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ispPAC®-POWR1208 Device Datasheet

September 2010

All Devices Discontinued!

Product Change Notification (PCN) #13-10 has been issued to discontinue all devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
ispPAC-POWR1208	ispPAC-POWR1208-01T44I	**Discontinued**	PCN#13-10
	ispPAC-POWR1208-01T44E		
	ispPAC-POWR1208-01TN44I		
	ispPAC-POWR1208-01TN44E		

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Internet: http://www.latticesemi.com

ispPAC®-POWR1208

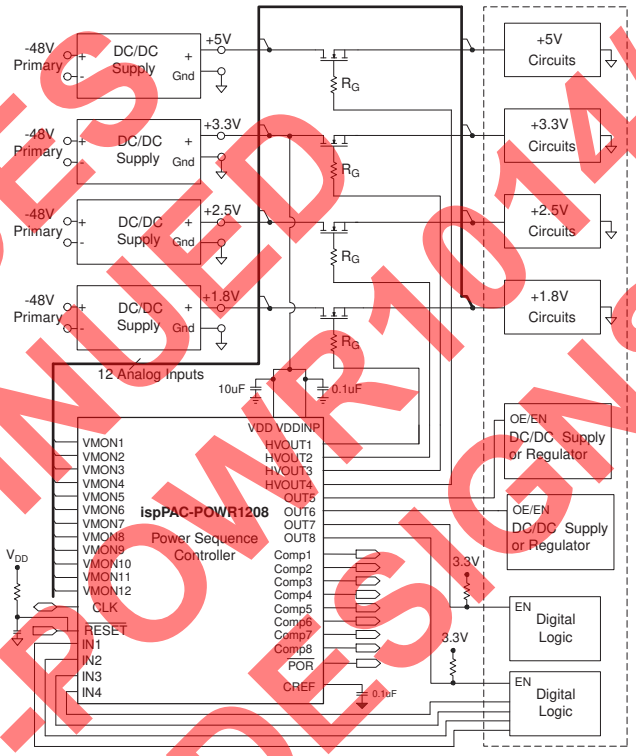
In-System Programmable Power Supply Sequencing Controller and Monitor

August 2004 **Data Sheet DS1031**

Features

- **Monitor and Control Multiple Power Supplies**
  - Simultaneously monitors up to 12 power supplies
  - Sequence controller for power-up conditions
  - Provides eight output control signals
  - Programmable digital and analog circuitry
- **Embedded PLD for Sequence Control**
  - Implements state machine and input conditional events
  - In-System Programmable (ISP™) through JTAG and on-chip E²CMOS®
- **Embedded Programmable Timers**
  - 4 Programmable 8-bit timers (32µs to 524ms)
  - Programmable time delay between multiple power supply ramp-up and wait statements
- **Analog Comparators for Monitoring**
  - 12 analog comparators for monitoring
  - 192 precise programmable threshold levels spanning 1.03V to 5.72V
  - Each comparator can be independently configured around standard logic supply voltages of 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V
  - Other user-defined voltages possible
  - Eight direct comparator outputs
- **Embedded Oscillator**
  - Built-in clock generator, 250kHz
  - Programmable clock frequency
  - Programmable timer pre-scaler
  - External clock support
- **Programmable Output Configurations**
  - Four digital outputs for logic and power supply control
  - Four fully programmable gate driver outputs for FET control, or programmable as four additional digital outputs
  - Expandable with ispMACH™ 4000 CPLD
- **2.25V to 5.5V Supply Range**
  - In-system programmable at 3.0V to 5.5V
  - Industrial temperature range: -40°C to +85°C
  - Automotive temperature range: -40°C to +125°C
  - 44-pin TQFP package
  - Lead-free package option

Application Block Diagram



Description

The Lattice ispPAC-POWR1208 incorporates both in-system programmable logic and in-system programmable analog circuits to perform special functions for power supply sequencing and monitoring. The ispPAC-POWR1208 device has the capability to be configured through software to control up to eight outputs for power supply sequencing and 12 comparators monitoring supply voltage limits, along with four digital inputs for interfacing to other control circuits or digital logic. Once configured, the design is downloaded into the device through a standard JTAG interface. The circuit configuration and routing are stored in non-volatile E²CMOS. PAC-Designer,® an easy-to-use Windows-compatible software package gives users the ability to design the logic and sequences that control the power supplies or FET driver circuits. The user has control over timing functions, programmable logic functions and comparator threshold values as well as I/O configurations.

Power Supply Sequence Controller and Monitor

The ispPAC-POWR1208 device is specifically designed as a fully-programmable power supply sequencing controller and monitor for managing up to eight separate power supplies, as well as monitoring up to 12 analog inputs or supplies. The ispPAC-POWR1208 device contains an internal PLD that is programmable by the user to implement digital logic functions and control state machines. The internal PLD connects to four programmable timers, special purpose I/O and the programmable monitoring circuit blocks. The internal PLD and timers can be clocked by either an internal programmable clock oscillator or an external clock source.

The voltage monitors are arranged as 12 independent comparators each with 192 programmable trip point settings. Monitoring levels are set around the following standard voltages: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V or 5.0V.

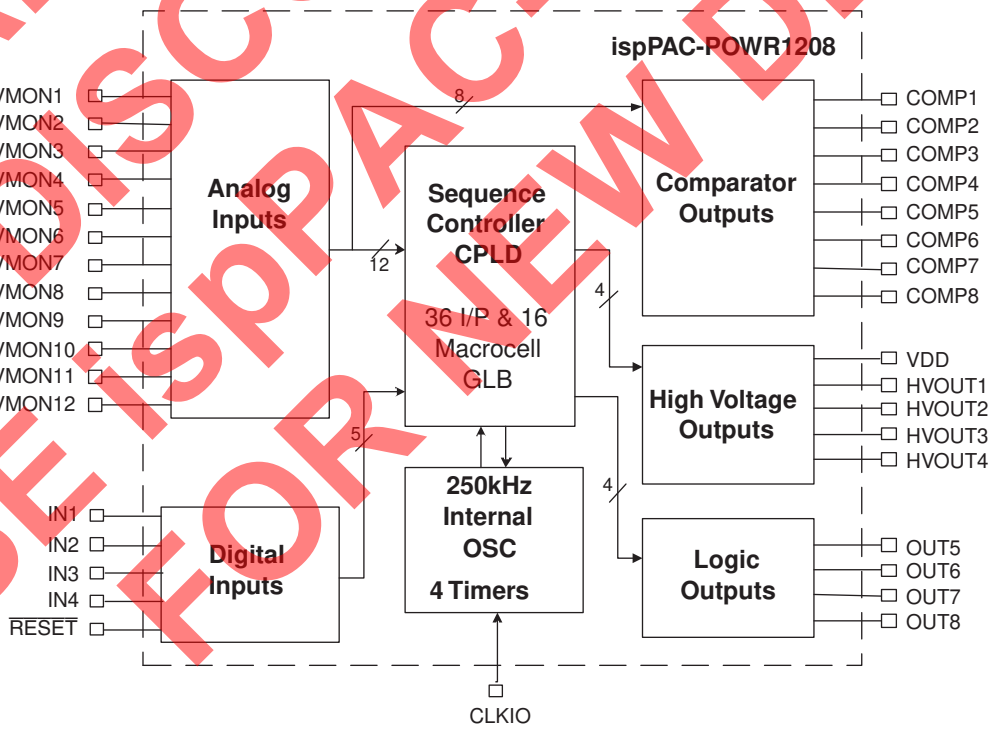
All 12 voltages can be monitored simultaneously (i.e., continuous-time operation). Other non-standard voltage levels can be accounted for using various scale factors.

For added robustness, the comparators feature a variable hysteresis that scales with the voltage they monitor. Generally, a larger hysteresis is better. However, as power supply voltages get smaller, that hysteresis increasingly affects trip-point accuracy. Therefore, the hysteresis is +/-16mV for 5V supplies and scales down to +/-3mV for 1.2V supplies, or about 0.3% of the trip point.

The programmable logic functions consist of a block of 36 inputs with 81 product terms and 16 macrocells. The architecture supports the sharing of product terms to enhance the overall usability.

Output pins are configurable in two different modes. There are eight outputs for controlling eight different power supplies. OUT5-OUT8 are open-drain outputs for interfacing to other circuits. The HVOUT1-HVOUT4 pins can be programmed individually as open-drain outputs or as high voltage FET gate drivers. As high voltage FET gate driver outputs, they can be used to drive an external N-Channel MOSFET as a switch to control the voltage ramp-up of the target board. The four HVOUT drivers have programmable current and voltage levels. Of the eight outputs, four can be configured in the FET gate driver mode or open-drain digital mode.

Figure 1-1. ispPAC-POWR1208 Block Diagram



Pin Descriptions

Number	Name	Pin Type	Voltage Range	Description
1	HVOUT4	O/D Output	2.25V-5.5V[2]	Open-drain Output 4
		Current Source	8V-12V[3]	FET Gate Driver 4
2	HVOUT3	O/D Output	2.25V-5.5V[2]	Open-drain Output 3
		Current Source	8V-12V[3]	FET Gate Driver 3
3	HVOUT2	O/D Output	2.25V-5.5V[2]	Open-drain Output 2
		Current Source	8V-12V[3]	FET Gate Driver 2
4	HVOUT1	O/D Output	2.25V-5.5V[2]	Open-drain Output 1
		Current Source	8V-12V[3]	FET Gate Driver 1
5	VDD	Power	2.25V-5.5V	Main Power Supply
6	IN1	CMOS Input	VDDINP[1]	Input 1
7	IN2	CMOS Input	VDDINP[1]	Input 2
8	IN3	CMOS Input	VDDINP[1]	Input 3
9	IN4	CMOS Input	VDDINP[1]	Input 4
10	$\overline{\text{RESET}}$	CMOS input	VDD[7]	PLD Reset Input, Active Low
11	VDDINP	Power	2.25V-5.5V[4]	Digital Inputs Power Supply
12	OUT5	O/D Output	2.25V-5.5V[2]	Open-Drain Output
13	OUT6	O/D Output	2.25V-5.5V[2]	Open-Drain Output
14	OUT7	O/D Output	2.25V-5.5V[2]	Open-Drain Output
15	OUT8	O/D Output	2.25V-5.5V[2]	Open-Drain Output
16	COMP8	O/D Output	2.25V-5.5V[2]	VMON8 Comparator Output (Open-Drain)
17	COMP7	O/D Output	2.25V-5.5V[2]	VMON7 Comparator Output (Open-Drain)
18	COMP6	O/D Output	2.25V-5.5V[2]	VMON6 Comparator Output (Open-Drain)
19	COMP5	O/D Output	2.25V-5.5V[2]	VMON5 Comparator Output (Open-Drain)
20	COMP4	O/D Output	2.25V-5.5V[2]	VMON4 Comparator Output (Open-Drain)
21	COMP3	O/D Output	2.25V-5.5V[2]	VMON3 Comparator Output (Open-Drain)
22	COMP2	O/D Output	2.25V-5.5V[2]	VMON2 Comparator Output (Open-Drain)
23	COMP1	O/D Output	2.25V-5.5V[2]	VMON1 Comparator Output (Open-Drain)
24	TCK	TTL/LVCMOS Input	VDD[6]	Test Clock (JTAG Pin)
25	$\overline{\text{POR}}$	O/D Output	2.25V-5.5V	Power-On-Reset Output
26	CLK	Bi-directional I/O	VDD	Clock Output (Open-Drain) or Clock Input
27	GND	Ground		Ground
28	TDO	TTL/LVCMOS Output	VDD	Test Data Out (JTAG Pin)
29	$\overline{\text{TRST}}$	TTL/LVCMOS Input	VDD	Test Reset, Active Low, 50k Ohm Internal Pull-up (JTAG Pin, Optional Use)
30	TDI	TTL/LVCMOS Input	VDD	Test Data In, 50k Ohm Internal Pull-up (JTAG Pin)
31	TMS	TTL/LVCMOS Input	VDD	Test Mode Select, 50k Ohm Internal pull-up (JTAG Pin)
32	VMON1	Analog Input	0V-5.72V[5]	Voltage Monitor Input 1
33	VMON2	Analog Input	0V-5.72V[5]	Voltage Monitor Input 2
34	VMON3	Analog Input	0V-5.72V[5]	Voltage Monitor Input 3
35	VMON4	Analog Input	0V-5.72V[5]	Voltage Monitor Input 4
36	VMON5	Analog Input	0V-5.72V[5]	Voltage Monitor Input 5
37	VMON6	Analog Input	0V-5.72V[5]	Voltage Monitor Input 6
38	VMON7	Analog Input	0V-5.72V[5]	Voltage Monitor Input 7

Pin Descriptions (Continued)

Number	Name	Pin Type	Voltage Range	Description
39	CREF	Reference	1.17V[8]	Reference for Internal Use, Decoupling Capacitor (.1uf Required, CREF to GND)
40	VMON8	Analog Input	0V-5.72V[5]	Voltage Monitor Input 8
41	VMON9	Analog Input	0V-5.72V[5]	Voltage Monitor Input 9
42	VMON10	Analog Input	0V-5.72V[5]	Voltage Monitor Input 10
43	VMON11	Analog Input	0V-5.72V[5]	Voltage Monitor Input 11
44	VMON12	Analog Input	0V-5.72V[5]	Voltage Monitor Input 12

1. IN1...IN4 are digital inputs to the PLD. The thresholds for these pins are referenced by the voltage on V_{DDINP}
2. The 18 open-drain outputs can be powered independently of V_{DD}, the open-drain outputs can be pulled up as high as +6.0V (referenced to ground). Exception, CLK pin 26 can only be pulled as high as V_{DD}.
3. The four FET driver outputs (when this mode is activated, the corresponding 4 open-drain outputs are disabled) are internally powered and can source up to 7.5V above V_{DD}.
4. V_{DDINP} can be chosen independent of V_{DD}. It applies only to the four logic inputs IN1-IN4.
5. The 12 VMON inputs can be biased independently of V_{DD}. The 12 VMON inputs can be as high as 7.0V Max (referenced to ground).
6. CLK is the PLD clock output in master mode. It is re-routed as an input in slave mode. The clock mode is set in software during design time. In output mode it is an open-drain type pin and requires an external pull-up resistor (pull-up voltage must be ≤ V_{DD}). Multiple ispPAC-POWR1208 devices can be tied together with one acting as the master, the master can use the internal clock and the slave can be clocked by the master. The slave needs to be set up using the clock as an input.
7. $\overline{RESET}$ is an active low INPUT pin, external pull-up resistor to V_{DD} is required. When driven low it resets all internal PLD flip-flops to zero or one, and may turn "ON" or "OFF" the output pins, including the HVOUT pins depending on the polarity configuration of the outputs in the PLD. If a reset function is needed for the other devices on the board, the PLD inputs and outputs can be used to generate these signals. The $\overline{RESET}$ connected to the $\overline{POR}$ pin can be used if multiple ispPAC-POWR1208 devices are cascaded together in expansion mode or if a manual reset button is needed to reset the PLD logic to the initial state. While using the ispPAC-POWR1208 in hot-swap applications it is recommended that either the $\overline{RESET}$ pin be connected to the $\overline{POR}$ pin, or connect a capacitor to ground (such that the time constant is 10 ms with the pull-up resistor) from the $\overline{RESET}$ pin.
8. The CREF pin requires a 0.1µF capacitor to ground, near the device pin. This reference is used internally by the device. No additional external circuitry should be connected to this pin.

Absolute Maximum Ratings

Absolute maximum ratings are shown in the table below. Stresses above those listed values may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{DD}	Core supply voltage at pin	—	-0.5	6.0	V
V_{DDINP}[1]	Digital input supply voltage for IN1-IN4	—	-0.5	6.0	V
HVOUTmax	HVOUT pin voltage, max = V_{DD} + 9V	—	-0.5	15	V
V_{IN}[2]	Input voltage applied, digital inputs	—	-0.5	6.0	V
VMON	Input voltage applied, V_{MON} voltage monitor inputs	—	-0.5	7.0	V
V_{TRI}	Tristated or open drain output, external voltage applied (CLK pin 26 pullup ≤ V_{DD}).	—	-0.5	6.0	V
T_S	Storage temperature	—	-65	150	°C
T_A	Ambient temperature with power applied	—	-55	125	°C
T_{SOL}	Maximum soldering temperature (10 sec. at 1/16 in.)	—	—	260	°C

1. V_{DDINP} is the supply pin that controls logic inputs IN1-IN4 only. Place 0.1µF capacitor to ground and supply the V_{DDINP} pin with appropriate supply voltage for the given input logic range.
2. Digital inputs are tolerant up to 5.5V, independent of the V_{DDINP} voltage.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{DD}	Core supply voltage at pin		2.25	5.5	V
V_{DDPROG}[1]	Core supply voltage at pin	During E^2 cell programming	3.0	5.5	V
V_{DDINP}[2]	Digital input supply voltage for IN1-IN4		2.25	5.5	V
V_{IN}[3]	Input voltage digital inputs		0	5.5	V
V_{MON}	Voltage monitor inputs V_{MON1} - V_{MON12}		0	6.0	V
Erase/Program Cycles		EEPROM, programmed at V_{DD} = 3.0V to 5.5V -40°C to +85°C	1000	—	Cycles
T_{APROG}	Ambient temperature during programming		-40	+85	°C
T_A	Ambient temperature	Power applied - Industrial	-40	+85	°C
		Power applied - Automotive	-40	+125	°C

1. The ispPAC-POWR1208 device must be powered from 3.0V to 5.5V during programming of the E^2CMOS memory.
2. V_{DDINP} is the supply pin that controls logic inputs IN1-IN4 only. Place 0.1µF capacitor to ground and supply the V_{DDINP} pin with appropriate supply voltage for the given input logic range.
3. Digital inputs are tolerant up to 5.5V, independent of the V_{DDINP} voltage.

Analog Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Supply Current	Internal Clock = 250kHz	—	7	15	mA

Reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{REF}[1]	Reference voltage at CREF pin	T = 25°C	—	1.17	—	V

1. CREF pin requires a 0.1µF capacitor to ground.

Voltage Monitors

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input impedance		70	100	130	kΩ
V_{MON} Range	Programmable voltage monitor trip point (192 steps)		1.03		5.72	V
V_{MON} Accuracy	Absolute accuracy of any trip point	T = 25 °C, V_{DD} = 3.3V	-0.9		+0.9	%
V_{MON} Tempco[1]	Temperature drift of any trip point	-40°C to +85°C		50		ppm/ °C
		-40°C to +125°C		76		ppm/ °C
HYST	Hysteresis of V_{MON} input, V_{HYST} = HYST*V_{MON} (+/-3 to +/-13mV)	V_{DD} = 3.3V		+/- 0.3% of trip point setting		%
PSR	Trip point sensitivity to V_{DD}	V_{DD} = 3.3V		0.06		%/V

1. See typical performance curves.

High Voltage FET Drivers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PP} Range	Programmable gate driver voltage (eight steps)	(Note 1)	8	—	12	V
V_{PP} Accuracy	Absolute accuracy of V_{PP} output voltage	25°C	-10	—	10	%
V_{PP} Step	Gate driver voltage step	(Note 2)	—	0.5	—	V
I_{SOURCE} Range	Programmable I_{SOURCE} current (32 steps)	FET Driver mode -40°C to +85°C	0.5	—	50	µA
	Programmable I_{SOURCE} current (16 steps)	FET Driver mode +85°C to +125°C (Note 3)	5.45	—	50	µA
I_{SOURCE} Accuracy	Absolute accuracy of I_{SOURCE} current	-40°C to +125°C I_{SOURCE} > 0.5µA	—	10	—	%
I_{STEP}	Relative current value, from any I_{SOURCE} setting to the next		—	15	—	%
R_{SINK}	Gate driver sink/discharge resistor when setting FET driver to a LOW state	FET Driver in OFF state V_{DD} = 2.25V	—	8	—	kΩ

1. Maximum voltage of V_{PP} is not to exceed 7.5V over V_{DD}.
2. The high voltage driver outputs are set in software, HVOUT voltage range is between 8V and 12V. V_{DD} values determine the maximum V_{PP}.
3. For high temperature operation from +85°C to +125°C, the lower HVOUT source current selections (0.5µA to 4.62µA) should not be used to drive MOSFETs due to increased leakage current to GND. Select gate currents from 5.45µA to 50µA for high temperature use.

Power-On-Reset

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{LPOR}	V_{DD} supply threshold beyond which $\overline{POR}$ output is guaranteed to be driven low	V_{DD} ramping up[1]	—	—	1.15	V
V_{HPOR}	V_{DD} supply threshold above which $\overline{POR}$ output is guaranteed driven high, and device initializes	V_{DD} ramping up[1]	—	—	2.1	V

1. POR tests run with 10kΩ resistor pulled up to V_{DD}.

AC/Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
Voltage Monitors						
t_{PD5}	Propagation Delay. Output transitions after a step input.	Glitch filter set to 5µs.[1] Input V_{TRIP} + 100mV to V_{TRIP} - 100mV	—	5	—	µs
t_{PD20}	Propagation Delay. Output transitions after a step input.	Glitch filter set to 20us.[1] Input V_{TRIP} + 100mV to V_{TRIP} - 100mV	—	20	—	µs
Oscillators						
f_{CLK}	Internal Master Clock frequency	(Note 2)	230	—	330	kHz
PLDCLK Range	Programmable frequency range of PLD clock (8 binary steps)	Internal Osc 250kHz	1.95	—	250	kHz
PLDCLKext	Max frequency of applied external clock source	External clock applied	—	—	1	MHz
Timers						
Timeout Range	Range of programmable time-out duration (15 steps)	Internal Osc 250kHz	0.03	—	524	ms

1. See Typical Performance Graphs.
2. f_{CLK} frequency sensitivity with respect to V_{DD}, 0.4%/Volt, typical.

Digital Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}	Input or I/O leakage current, no pull-up	0V ≤ V_{IN} ≤ V_{DDINP} or V_{DD} 25 °C			+/-10	µA
I_{PU}	Input pull-up current (TMS, TDI, $\overline{TRST}$)	25 °C		70		µA
V_{OL}	[OUT5-OUT8] [COMP1-COMP8] [HVOUT1-HVOUT4]	$I_{SINKOUT}$ = 4mA			0.4	V
$I_{SINKHVOUT}$	Maximum sink current for HVOUT pins in open-drain mode [HVOUT1-HVOUT4]	(Note 1)			4	mA
$I_{SINKOUT}$	Maximum sink current for logic outputs [OUT5-OUT8], [COMP1-COMP8]	(Note 1)			20	mA
$I_{SINKTOTAL}$	Total combined sink currents from all outputs [OUT, HVOUT, COMP]	(Note 1)			80	mA

1. [OUT5-OUT8] and [COMP1-COMP8] can sink up to 20mA max. per pin for LEDs, etc. However, output voltage levels may exceed V_{OL}. Total combined sink currents from all outputs (OUT, HVOUT, COMP) should not exceed $I_{SINKTOTAL}$.

DC Input Levels: IN1-IN4

Standard	V_{IL} (V)		V_{IH} (V)	
	Min.	Max.	Min.	Max.
CMOS, LVCMOS3.3, LVTTL, TTL	-0.3	0.8	2.0	5.5
LVCMOS2.5	-0.3	0.7	1.7	5.5

Note: V_{DDINP} is the input supply pin for IN1-IN4 digital logic input pins. The logic threshold trip point of IN1-IN4 is dependent on the voltage at V_{DDINP}.

Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PLD Timing						
Digital Glitch Filter	Minimum pulse width to transition through glitch filter.	Applied to IN1-IN4	20			µs
t_{CO}	Clock to Out Delay. Rising edge of clock to output transition.	Stable input before clock edge (Note 1)			300	ns
t_{SU}	Time that input needs to be present when using a registered function with the clock.	Data valid before clock (Note 1)	20			µs
t_{H}	Time that input needs to be held valid after the clock edge when using a registered function with the clock.	Hold data after clock	0			µs
t_{PD}	Propagation delay internal to the embedded PLD				90	ns
t_{RST}	$\overline{\text{RESET}}$ pulse width		25			µs

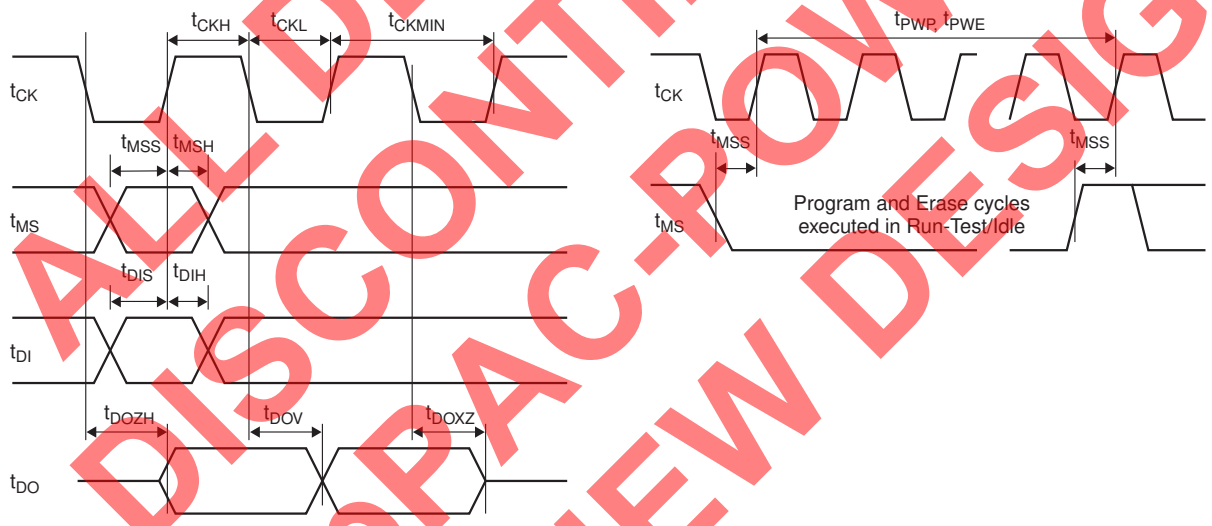
1. External clock 1MHz. Open drain outputs with 2k pull-up resistor to V_{DD}.

Note: All the above parameters apply to signal paths from the digital inputs [IN1-IN4].

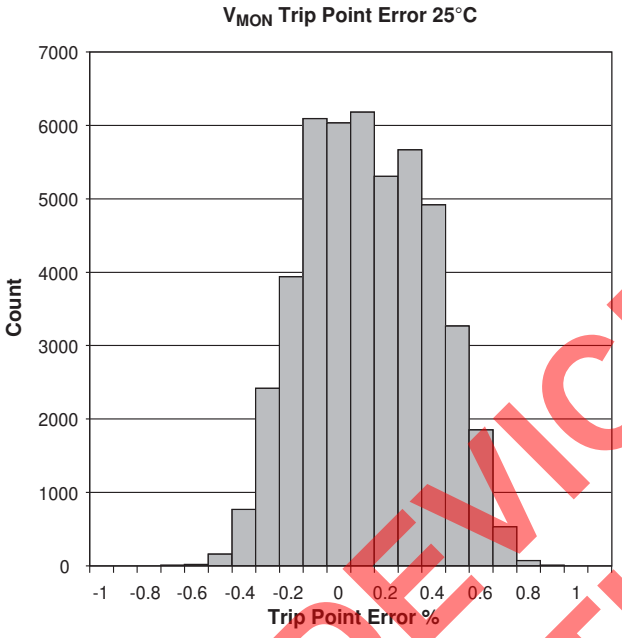
Timing for JTAG Operations

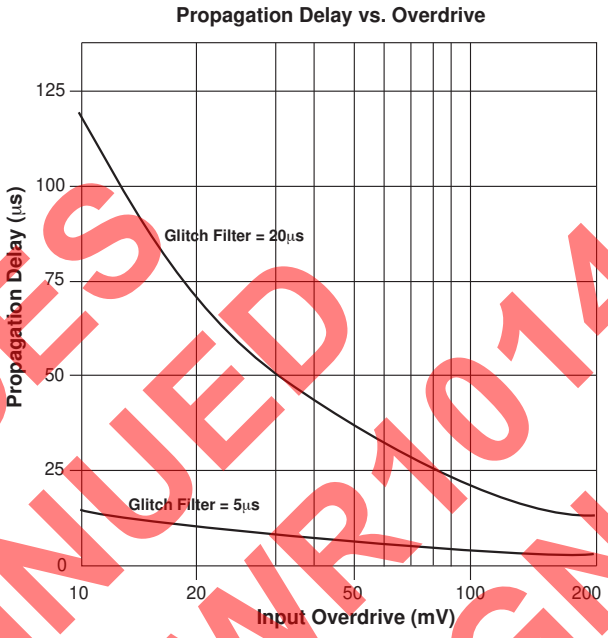
Symbol	Parameter	Conditions	Min	Typ.	Max	Units
t_{CKMIN}	Minimum clock period		1			µs
t_{CKH}	TCK high time		200			ns
t_{CKL}	TCK low time		200			ns
t_{MSS}	TMS setup time		15			ns
t_{MSH}	TMS hold time		50			ns
t_{DIS}	TDI setup time		15			ns
t_{DIH}	TDI hold time		50			ns
t_{DOZX}	TDO float to valid delay				200	ns
t_{DOV}	TDO valid delay				200	ns
t_{DOXZ}	TDO valid to float delay				200	ns
t_{RSTMIN}	Minimum reset pulse width		40			ns
t_{PWP}	Time for a programming operation[1]		40		100	ms
t_{PWE}	Time for an erase operation		40		100	ms

1. t_{PWP} represents programming pulse width for a single row of E^2CMOS cells.



Typical Performance Graphs





Note: Typical propagation delay of V_{MON} inputs to outputs as a function of overdrive beyond selected trip point.

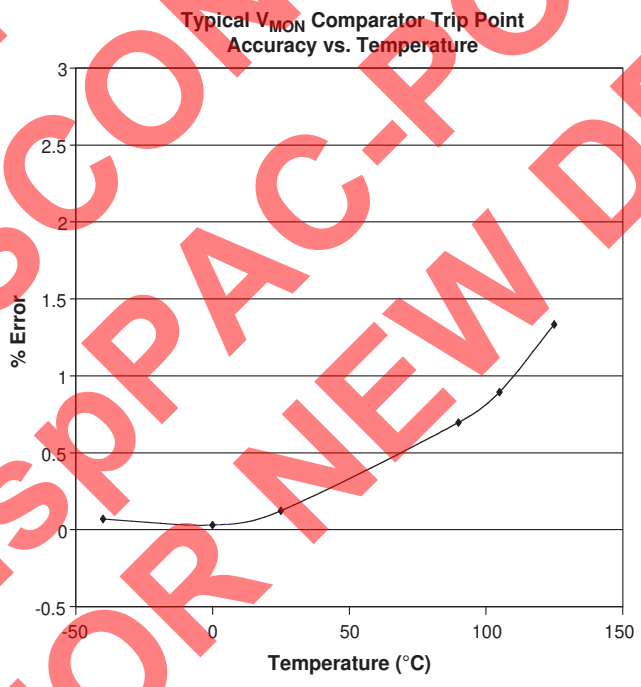


Table1-1. V_{MON} Trip Point Table[1]

1.2 low	1.2 high	1.5 low	1.5 high	1.8 low	1.8 high	2.5 low	2.5 high	3.3 low	3.3 high	5.0 low	5.0 high
1.036	1.202	1.291	1.502	1.549	1.801	2.153	2.500	2.842	3.297	4.299	4.991
1.046	1.213	1.303	1.516	1.564	1.818	2.173	2.524	2.869	3.328	4.340	5.038
1.056	1.225	1.316	1.531	1.579	1.836	2.195	2.549	2.897	3.361	4.383	5.088
1.066	1.237	1.329	1.546	1.595	1.854	2.216	2.574	2.926	3.394	4.426	5.138
1.076	1.249	1.341	1.560	1.609	1.871	2.237	2.597	2.952	3.425	4.466	5.185
1.087	1.261	1.354	1.575	1.625	1.889	2.258	2.622	2.981	3.458	4.509	5.235
1.096	1.272	1.366	1.590	1.639	1.906	2.279	2.646	3.008	3.489	4.550	5.282
1.107	1.284	1.379	1.605	1.655	1.924	2.300	2.671	3.036	3.522	4.593	5.332
1.117	1.295	1.391	1.619	1.669	1.941	2.320	2.694	3.063	3.553	4.633	5.379
1.127	1.307	1.404	1.634	1.685	1.959	2.342	2.719	3.091	3.586	4.676	5.429
1.137	1.319	1.417	1.649	1.700	1.977	2.363	2.744	3.120	3.619	4.719	5.479
1.147	1.331	1.429	1.663	1.715	1.994	2.384	2.768	3.147	3.650	4.760	5.526
1.157	1.343	1.442	1.678	1.730	2.012	2.405	2.793	3.175	3.683	4.803	5.576
1.168	1.355	1.455	1.693	1.746	2.030	2.427	2.818	3.203	3.716	4.846	5.626
1.178	1.366	1.467	1.707	1.761	2.047	2.447	2.841	3.230	3.747	4.886	5.673
1.188	1.378	1.480	1.722	1.776	2.065	2.469	2.866	3.259	3.780	4.929	5.723

1.All possible comparator trip voltages using internal attenuation settings.

Table 1-1 shows all possible comparator trip point voltage settings. The internal resistive divider allows ranges for 1.2V, 1.8V, 2.5V, 3.3V and 5.0V. There are 192 available voltages, ranging from 1.036V to 5.723V. In addition to the 192 voltage monitor trip points, the user can add additional resistors outside the device to divide down the voltage and achieve virtually any voltage trip point. This allows the capability to monitor higher voltages such and 12V, 15V, 24V, etc. Voltage monitor trip points are set in the graphical user interface of PAC-Designer software by simple pull-down menus. The user simply selects the given range and corresponding trip point value. Attenuation and reference values are set internally using E^2CMOS configuration bits internal to the device.

Figure 1-2 shows a single comparator, the attenuation network and reference used to program the monitor trip points. Each of the twelve comparators are independently set in the same way.

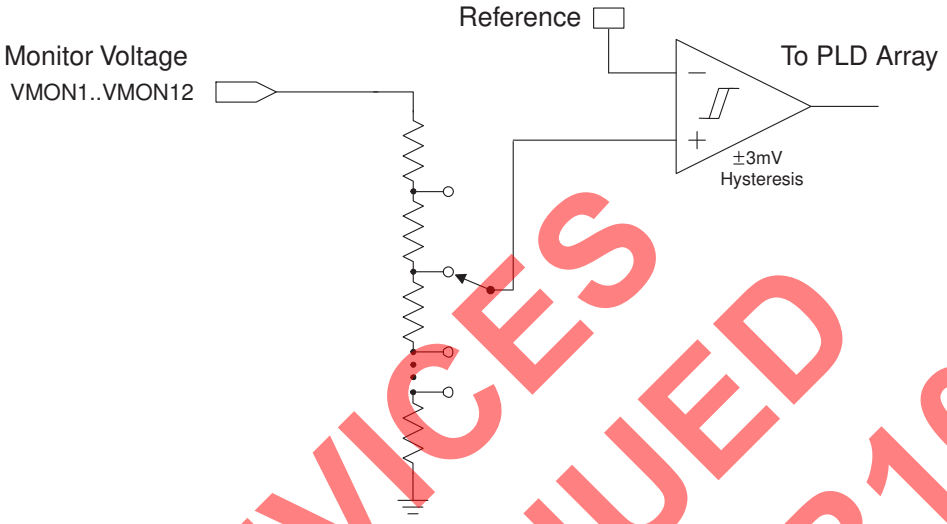
Theory Of Operation

The ispPAC-POWR1208 incorporates programmable voltage monitors along with digital inputs and outputs as well as high voltage FET gate drivers to control MOSFETs for ramping up power supply rails. The 16 macrocell PLD inputs are from the 12 voltage monitors and four digital inputs. There are four embedded programmable timers that interface with the PLD, along with an internal programmable oscillator.

The 12 independently programmable voltage monitors each have 192 programmable trip points.

Figure 1-2 shows a simplified schematic representation of one of these monitors.

Figure 1-2. Voltage Monitors



Each monitor consists of three major subsystems. The core of the monitor is a voltage comparator. This comparator outputs a HIGH signal to the PLD array if the voltage at its positive terminal is greater than that at its negative terminal, otherwise it outputs a LOW signal. A small amount of hysteresis is provided by the comparator to reduce the effects of input noise.

The input signal is attenuated by a programmable resistive divider before it is fed into the comparator. This feature is used to determine the coarse range in which the comparator should trip (e.g. 1.8V, 3.3V, 5V). Twelve possible ranges are available from the input divider network. The comparator's negative terminal is obtained from a programmable reference source (Reference), which may be set to one of 16 possible values scaled in approximately 1% increments from each other, allowing for fine tuning of the voltage monitor's trip points. This combination of coarse and fine adjustment supports 192 possible trip-point voltages for a given monitor circuit. Because each monitor's reference and input divider settings are completely independent of those of the other monitor circuits', the user can set any input monitor to any of the 192 available settings.

Comparator Hysteresis

V_{MON} Range Setting[1]	Typical Hysteresis on Over Voltage Range	Typical Hysteresis on Under Voltage Range	Units
5.0V	+/- 16.2	+/- 14.0	mV
3.3V	+/- 10.7	+/- 9.2	mV
2.5V	+/- 8.1	+/- 7.0	mV
1.8V	+/- 5.8	+/- 5.0	mV
1.5V	+/- 4.9	+/- 4.2	mV
1.2V	+/- 3.9	+/- 3.4	mV

1. The hysteresis scales depending on the voltage monitor range that is selected. The values shown are typical and are centered around the nominal voltage trip point for a given range selection.

PLD Architecture

The ispPAC-POWR1208 digital logic is composed of an internal PLD that is programmed to perform the sequencing functions. The PLD architecture allows flexibility in designing various state machines and control logic used for monitoring. The macrocell shown in Figure 1-3 is the heart of the PLD. There are 16 macrocells that can be used to control the functional states of the sequencer state machine or other control or monitoring logic. The PLD AND array shown in Figure 1-4 has 36 inputs, and 81 product terms (PTs). The resources from the AND array feed the 16 macrocells. The resources within the macrocells share routing and contain a product-term allocation array. The

product term allocation array greatly expands the PLD's ability to implement complex logical functions by allowing logic to be shared between adjacent blocks and distributing the product terms to allow for wider decode functions.

The basic macrocell has five product terms that feed the OR gate and the flip-flop. The flip-flop in each macrocell is independently configured. It can be programmed to function as a D-Type or T-Type flip-flop. The combinatorial functions are achieved through the bypass MUX function shown. By having the polarity control XOR, the logic reduction can be best fit to minimize the number of product terms. The flip-flop's clock is driven from a common clock that can be generated from a pre-scaled, on-board clock source or from an external clock. The macrocell also supports asynchronous reset and preset functions, derived from either product terms, the global reset input or the power-on reset signal.

Figure 1-3. ispPAC-POWR1208 Macrocell Block Diagram

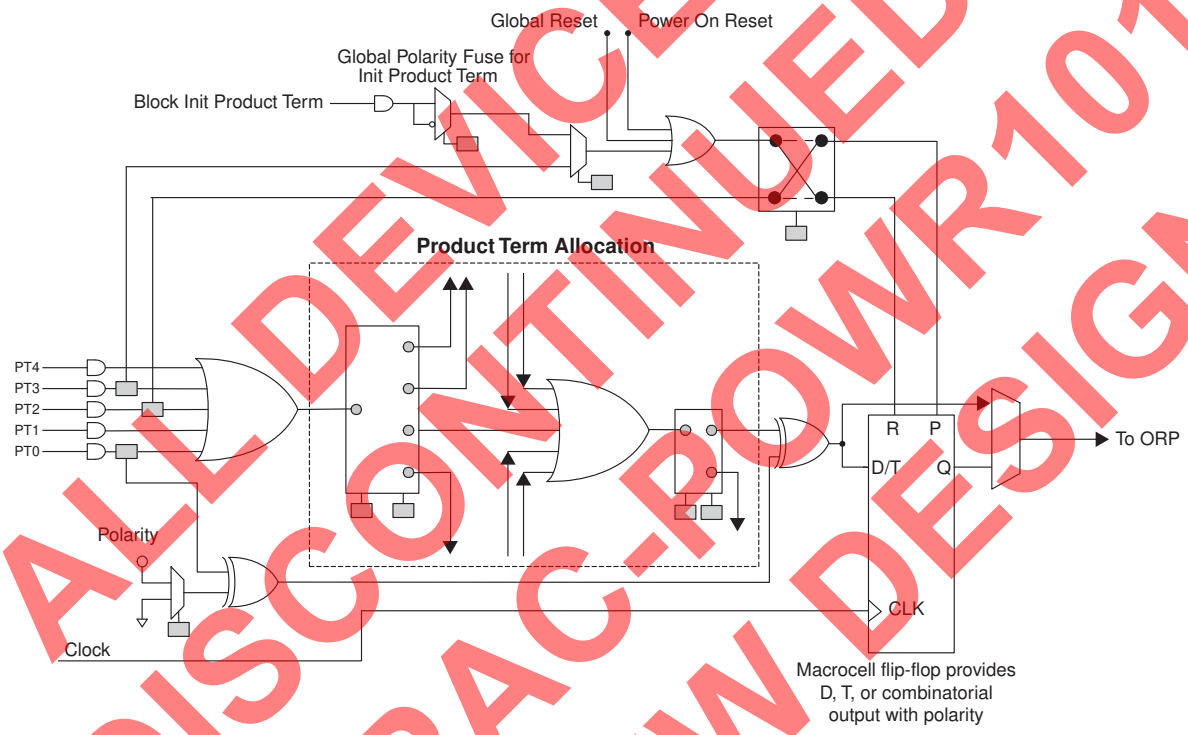
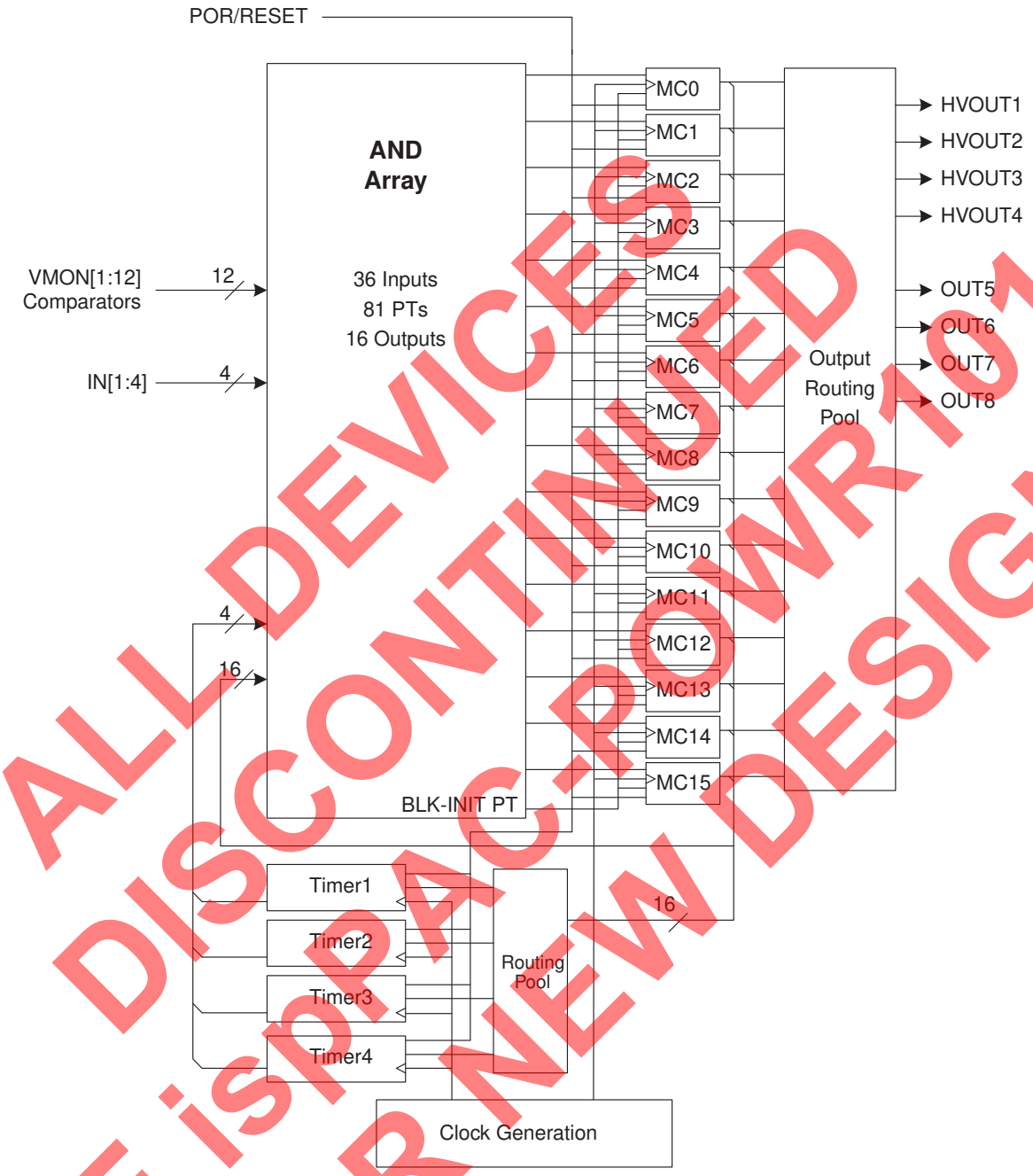


Figure 1-4. PLD and Timer Functional Block Diagram



Clock and Timer Systems

Figure 1-5 shows a block diagram of the ispPAC-POWR1208's internal clock and timer systems. The PLD clock can be programmed with eight different frequencies based on the internal oscillator frequency of 250kHz.

Figure 1-5. Clock and Timer Block

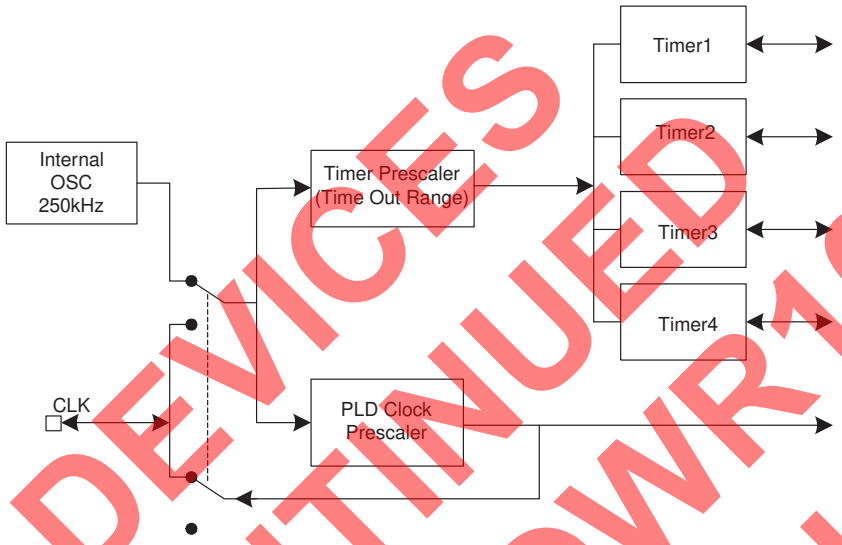


Table 1-2. PLD Clock Prescaler[1]

PLD Clock Frequency (kHz)	PLD Prescaler Divider
250	1
125	2
62.5	4
31.3	8
15.6	16
7.8	32
3.9	64
2	128

1. Values based on 250kHz clock.

The internal oscillator runs at a fixed frequency of 250kHz. This main signal is then fed to the PLD clock pre-scaler and also the Timer Clock pre-scaler (Figure 1-5). For the PLD Clock, the main 250kHz oscillator is divided down to eight selectable frequencies shown in the Table 1-2. The architecture of the clock network allows the PLD clock to be driven to the CLK pin. This enables the user access to the PLD clock as an output for expansion mode or other uses of the (CLK) clock pin.

Schematically, when the switch is in the upper position, the internal oscillator drives the PLD clock pre-scaler and the timer pre-scaler. In this mode, the CLK pin is an open-drain output and represents the same frequency as the PLD clock. This is used when operating other devices (such as "slave" sequencing devices) in a synchronized mode. When the switch is in the lower position, the CLK pin is an input and must be driven with an external clock source. When driven from an external source, the same PLD clock pre-scaler is available to this external clock. The frequencies available for the PLD clock will be the external clock frequency divided by 1, 2, 4, 8, 16, 32, 64 or 128, depending on the programmable value chosen.

The Timer Clock Pre-Scaler divides the internal 250kHz oscillator (or external clock, if selected) down before it generates the clock for the four programmable timers. The pre-scaler has eight different divider ratios: Divide by 4, 8,

16, 32, 64, 128, 256 and 512 (Table 1-3). After the clock for the timers is divided down, it is used to drive the programmable timers. The four timers share the same timer clock frequency but may have different end count values. The timers can cover a range from 32us to 524ms for the internal oscillator. Longer delays can be achieved by using the external clock as an input.

Table 1-3. Timer Values[1]

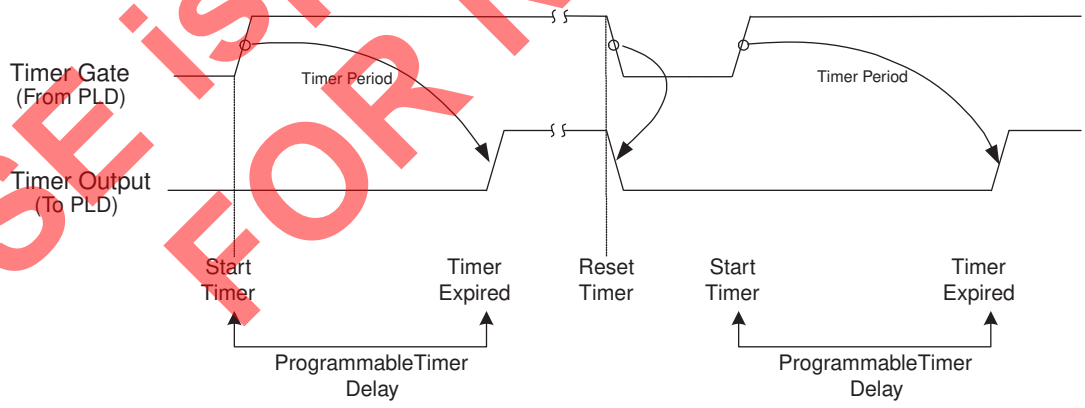
÷ 4 62 kHz	÷ 8 31.2 kHz	÷ 16 15.6 kHz	÷ 32 7.8 kHz	÷ 64 3.9 kHz	÷ 128 2 kHz	÷ 256 1 kHz	÷ 512 0.5 kHz
0.032 ms							
0.064 ms	0.064 ms						
0.128 ms	0.128 ms	0.128 ms					
0.256 ms	0.256 ms	0.256 ms	0.256 ms				
0.512 ms	0.512 ms	0.512 ms	0.512 ms	0.512 ms			
1.024 ms	1.024 ms	1.024 ms	1.024 ms	1.024 ms	1.024 ms		
2.048 ms	2.048ms	2.048ms	2.048ms	2.048ms	2.048ms	2.048ms	
4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms
	8.192 ms	8.192 ms	8.192 ms	8.192 ms	8.192 ms	8.192 ms	8.192 ms
		16.384 ms	16.384 ms	16.384 ms	16.384 ms	16.384 ms	16.384 ms
			32.768 ms	32.768 ms	32.768 ms	32.768 ms	32.768 ms
				65.536 ms	65.536 ms	65.536 ms	65.536 ms
					131.072 ms	131.072 ms	131.072 ms
						262.144 ms	262.144 ms
							524.288 ms

1. Timer values based on 250kHz clock.

For design entry, the user can select the source for the clock and the PAC-Designer software will calculate the appropriate delays in an easy-to-select menu format.

The control inputs for Timer1-Timer4 can be driven by any of the 16 PLD macrocell outputs. The reset for the timers is a function of the Global Reset pin ($\overline{\text{RESET}}$), a power-on reset or when the timer gate goes low. The waveforms in Figure 1-6 show the basic timer start and reset functions. Timer and clock divider values are entered in during the design phase using PAC-Designer software, simple pull-down menus allow the user to select the clocking mode and the values for the timers and the PLD clock.

Figure 1-6. Timer Waveforms



Note that if the clock module is configured as “slave” (i.e. the CLK is an input), the actual time-out of the four timers is determined by the external clock frequency.

Output Configuration Modes

The output pins for the ispPAC-POWR1208 device are programmable for different functional modes. The four outputs HVOUT1-HVOUT4, can be used as FET gate drivers or be programmed as open-drain digital outputs. Figure 1-7 explains the details of the gate driver mode.

Figure 1-7. Basic Function Diagram for an Output in Gate Driver Mode

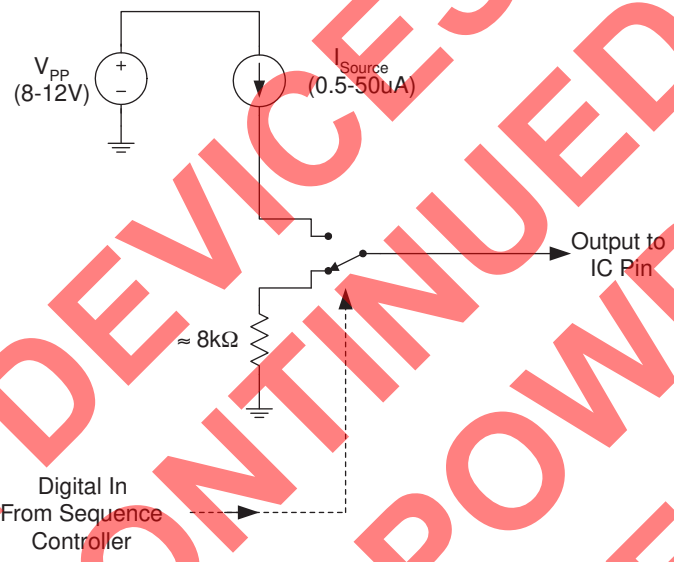
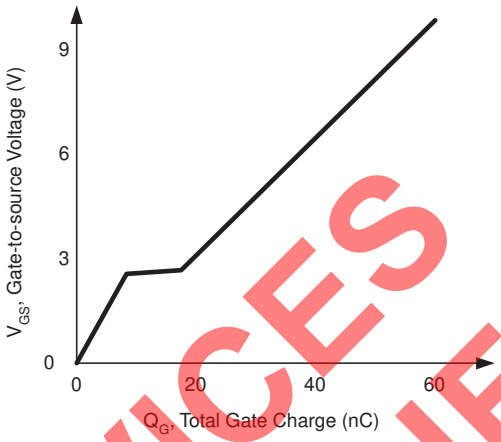


Figure 1-7 shows an output programmed for gate driver mode. In this mode the output is a current source that is programmable between 0.5µA to 50µA. The maximum voltage that the output level at the pin will rise is also programmable. The levels required depend on the gate-to-source threshold of the FET and the supply voltage. The maximum level needs to be sufficient to turn the gate-to-source threshold on and accommodate for the voltage of the board also, since the source pin of the FET is tied to the supply of the target board. When the HVOUT pin is sourcing current, charging a FET gate, the current is programmable between 0.5µA and 50µA. When the driver is turned to the off state, the driver will sink current. through the 8kΩ resistor.

Predicting MOSFET Turn-on Time

Because the ispPAC-POWR1208's MOSFET output drivers source a precise and well-defined output current, it becomes possible to predict MOSFET gate rise times if one knows the value of the load capacitance presented by the MOSFET being driven. The other method is by relating the total gate charge to the gate-to-source voltage.

Figure 1-8. MOSFET Gate Charge vs. Gate-Source Voltage



Using this method, it becomes straightforward to estimate the gate rise time for a given charging current. As an example a MOSFET's source voltage (V_S) will be 3.3V when the device is fully switched on, while the gate voltage (V_G) will be 10V in this condition. The device's gate-to-source voltage (V_{GS}) will therefore be 6.7V. Reading across and down the plot of Figure 1-8, a V_{GS} of 6.7V corresponds to ~40 nC of gate charge (Q_G). Because charge is equal to the product of current (I) and time ($t_{CHARGE-TIME}$) when current is constant, gate charging time can be expressed as:

$$i = \frac{dQ}{dt} \quad (1)$$

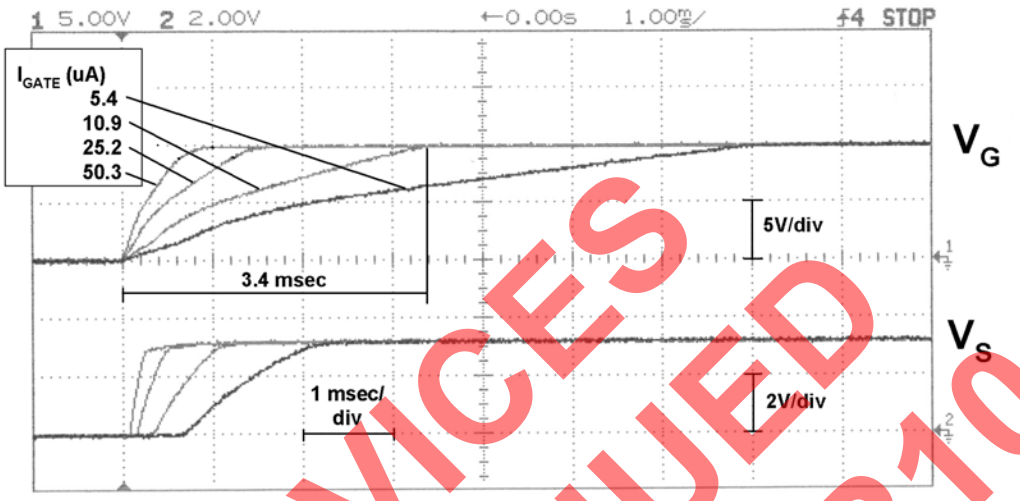
$$t_{CHARGE-TIME} = \frac{Q_G}{I} \quad (2)$$

For this example, let us assume a charging current of 10.9µA. Gate charging time is given by:

$$t_{CHARGE-TIME} = \frac{40 \times 10^{-9}C}{10.9 \times 10^{-6}A} = 3.7 \times 1 \quad (3)$$

Validation of this result can be seen in the scope plot shown in Figure 1-9. The top set of traces shows gate rise times for various (5.5µA to 50.3µA) gate drive currents. The trace labeled 10.9µA shows a 0-10V rise time of just over 3 milliseconds, which agrees to within 25% of our predicted value, well within the limits of device-to-device variation.

Figure 1-9. Gate and Source Voltage Responses for a 3.3V Supply



MOSFET gate capacitance ranges from hundreds to thousands of picoFarads. Refer to the MOSFET manufacturer's data sheet for values of Cgs (Capacitance gate-to-source). If slower ramps are required, an additional external low leakage capacitor (e.g. a polycarbonate or other poly type capacitor) can be added from the gate to ground. As a good design practice, it is recommended that a series resistor of 10-100Ω be placed in the gate drive signal near the FET gate pin.

Charge Pump

Four internal charge pumps are provided to fully support external N-channel FET devices. No external components are required for the charge pumps. The output voltage is programmable from 8 to 12V in 0.5V steps. The user must select a high voltage limit no greater than 7.5V above V_{DD} (the software assists this process). This voltage is controlled with an on-chip feedback loop, and is independent of the actual supply voltage.

Programmable Output Voltage Levels for HVOUT1- HVOUT4

There are eight selectable steps for the output voltage of the FET drivers when in FET driver mode. The output pins HVOUT1-4 are current source outputs, each with a programmable current. The current is programmable in 32 different steps ranging from .5µA to 50µA. The voltage that the pin is capable of driving to is listed in Table 1-4. For each supply range, the charge-pump range will be set by the software.

Table 1-4. HVOUT Gate Driver Voltage Range

V_{DD} = 2.5V	V_{DD} = 3.3V	V_{DD} = 5V
8	8	8
8.5	8.5	8.5
9	9	9
9.5	9.5	9.5
	10	10
		10.5
		11
		12

IEEE Standard 1149.1 Interface

Communication with the ispPAC-POWR1208 is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispPAC-POWR1208 as a serial programming interface, and not for boundary scan test purposes. There are no boundary scan logic registers in the ispPAC-POWR1208 architecture. This does not prevent the ispPAC-POWR1208 from functioning correctly, however, when placed in a valid serial chain with other IEEE 1149.1 compliant devices. Since the ispPAC-POWR1208 is used to powerup other devices, it should be programmed in a separate chain from PLDs, FPGAs or other JTAG devices.

A brief description of the ispPAC-POWR1208 serial interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990 (which now includes IEEE Std 1149.1a-1993).

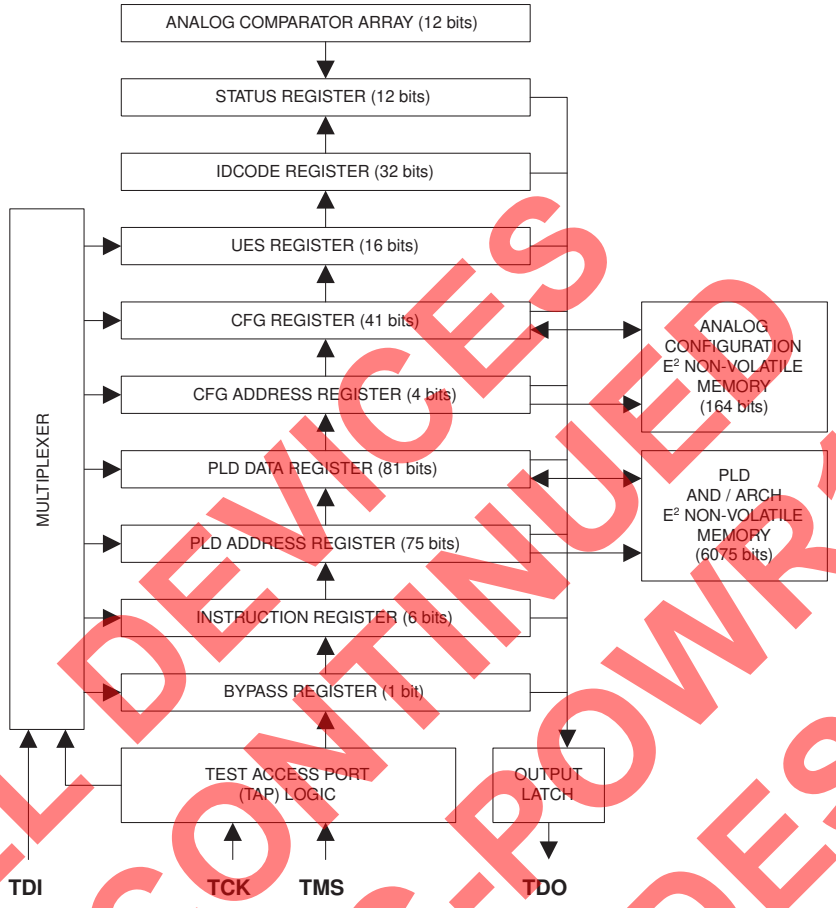
Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispPAC-POWR1208. The TAP controller is a state machine driven with mode and clock inputs. Under the correct protocol, instructions are shifted into an instruction register, which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing various registers, shifting data in, and then executing the respective program instruction. The programming instructions transfer the data into internal E^2CMOS memory. It is these non-volatile memory cells that determine the configuration of the ispPAC-POWR1208. By cycling the TAP controller through the necessary states, data can also be shifted out of the various registers to verify the current ispPAC-POWR1208 configuration. Instructions exist to access all data registers and perform internal control operations.

For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Other registers are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional user data registers that are defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. For ispPAC-POWR1208, the bypass register is a 1-bit shift register that provides a short path through the device when boundary testing or other operations are not being performed. The ispPAC-POWR1208, as mentioned earlier has no boundary-scan logic and therefore no boundary scan register. All instructions relating to boundary scan operations place the ispPAC-POWR1208 in the BYPASS mode to maintain compliance with the specification.

The optional identification (IDCODE) register described in IEEE 1149.1 is also included in the ispPAC-POWR1208. Six additional user data registers are included in the TAP of the ispPAC-POWR1208 as shown in Figure 1-10. Most of these additional registers are used to program and verify the analog configuration (CFG) and PLD bits. A status register is also provided to read the status of the twelve analog comparators.

Figure 1-10. TAP Registers

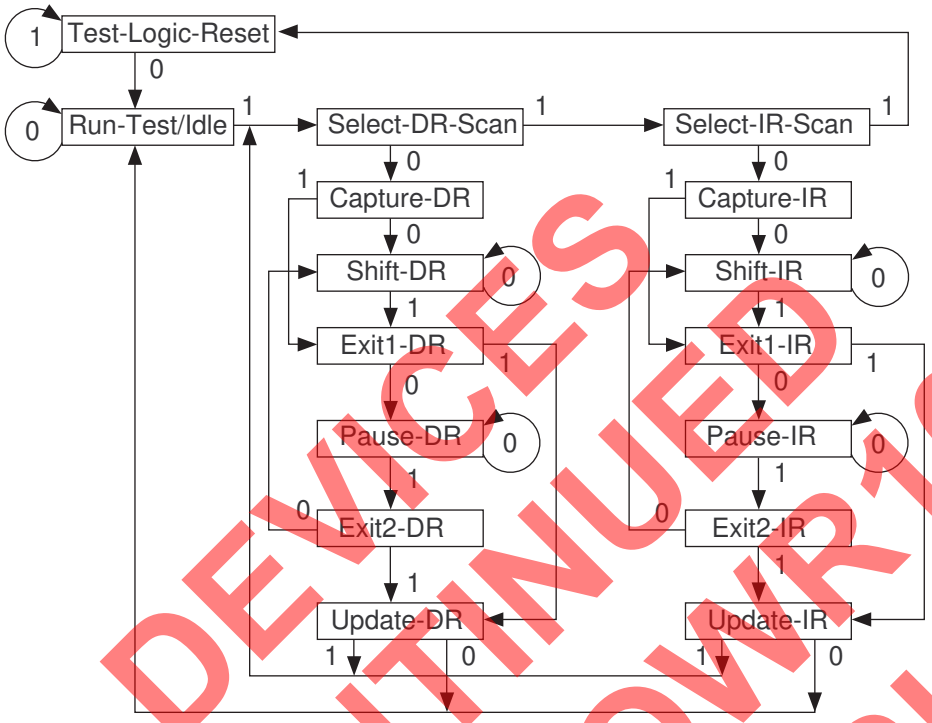


TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller. In a given state, the controller responds according to the level on the TMS input as shown in Figure 1-11. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run-Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register, and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction scan is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction scan is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple; it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain.

Figure 1-11. TAP States



Note: The value shown adjacent to each state transition represents the signal present at TMS at the time of a rising edge at TCK.

From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by re-entering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispPAC-POWR1208 contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured, verified, and monitored. For ispPAC-POWR1208, the instruction word length is 6-bits. All ispPAC-POWR1208 instructions available to users are shown in Table 1-5.

Table 1-5. ispPAC-POWR1208 TAP Instruction Table

Instruction	Code	Description
EXTEST	000000	External Test. Defaults to BYPASS.
ADDPLD[1]	000001	Address PLD address register (75 bits).
DATAPLD[1]	000010	Address PLD column data register (81 bits).
ERASEAND[1, 2]	000011	Bulk Erase AND array.
ERASEARCH[1, 2]	000100	Bulk Erase Architect array.
PROGPLD[1, 2]	000101	Program PLD column data register into E^2.
PROGESF[1, 2]	000110	Program the Electronic Security Fuse bit.
BYPASS	000111	Bypass (connect TDI to TDO).
READPLD[1]	001000	Reads PLD column data from E^2 to the register (81 bits).
DISCHARGE[1]	001001	Fast VPP discharge.
ADDCFG[1]	001010	Address CFG array address (4 bits).
DATACFG[1]	001011	Address CFG data (41 bits).
ERASECFG[1, 2]	001100	Bulk Erase CFG data.
PROGCFG[1, 2]	001101	Program CFG data register into E^2.
READCFG[1]	001110	Read CFG column data from E^2 to the register (41 bits).
CFGBE[1, 2]	010110	Bulk Erase all E^2 memory (CFG, PLD, USE, and ESF).
SAFESTATE[1]	010111	Digital outputs hiZ (FET pulled L)
PROGRAMEN[1]	011000	Enable program mode (SAFESTATE IO)
IDCODE	011001	Address Identification Code data register (32 bits).
PROGRAMDIS	011010	Disable Program mode (normal IO)
ADDSTATUS	011011	Address STATUS register (12 bits).
SAMPLE	011100	Sample/Preload. Default to Bypass.
ERASEUES[1, 2]	011101	Bulk Erase UES.
SHIFTUES	011110	Reads UES data from E^2 and selects the UES register (16 bits).
PROGUES[1, 2]	011111	Program UES data register into E^2.
BYPASS	1xxxxx	Bypass (connect TDI to TDO).

1. When these instructions are executed, the outputs are placed in the same mode as the instruction SAFESTATE (as described later) to prevent invalid and potentially destructive power supply sequencing.
2. Instructions that erase or program the E^2CMOS memory must be executed only when the supply to the device is maintained at 3.0V to 5.5V.

BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispPAC-POWR1208. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

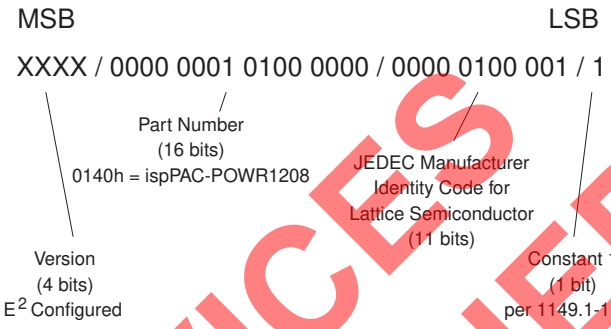
The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The ispPAC-POWR1208 has no boundary scan register, so for compatibility it defaults to the BYPASS mode whenever this instruction is received. The bit code for this instruction is defined by Lattice as shown in Table 1-5.

The **EXTEST** (external test) instruction is required and would normally place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. Again, since the ispPAC-POWR1208 has no boundary scan logic, the device is put in the BYPASS mode to ensure specification compatibility. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispPAC-POWR1208 and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer,

device type and version code (Figure 1-12). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 1-5.

Figure 1-12. ID Code



ispPAC-POWR1208 Specific Instructions

There are 21 unique instructions specified by Lattice for the ispPAC-POWR1208. These instructions are primarily used to interface to the various user registers and the E^{2}CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 1-5.

ADDPLD – This instruction is used to set the address of the PLD AND/ARCH arrays for subsequent program or read operations. This instruction also forces the outputs into the SAFESTATE.

DATAPLD – This instruction is used to shift PLD data into the register prior to programming or reading. This instruction also forces the outputs into the SAFESTATE.

ERASEAND – This instruction will bulk erase the PLD AND array. The action occurs at the second rising edge of TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

ERASEARCH – This instruction will bulk erase the PLD ARCH array. The action occurs at the second rising edge of TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

PROGPLD – This instruction programs the selected PLD AND/ARCH array column. The specific column is preselected by using ADDPLD instruction. The programming occurs at the second rising edge of the TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

PROGESF – This instruction is used to program the electronic security fuse (ESF) bit. Programming the ESF bit protects proprietary designs from being read out. The programming occurs at the second rising edge of the TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

READPLD – This instruction is used to read the content of the selected PLD AND/ARCH array column. This specific column is preselected by using ADDPLD instruction. This instruction also forces the outputs into the SAFESTATE.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispPAC-POWR1208 for a read cycle. This instruction also forces the outputs into the SAFESTATE.