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ispPAC®-POWR1220AT8

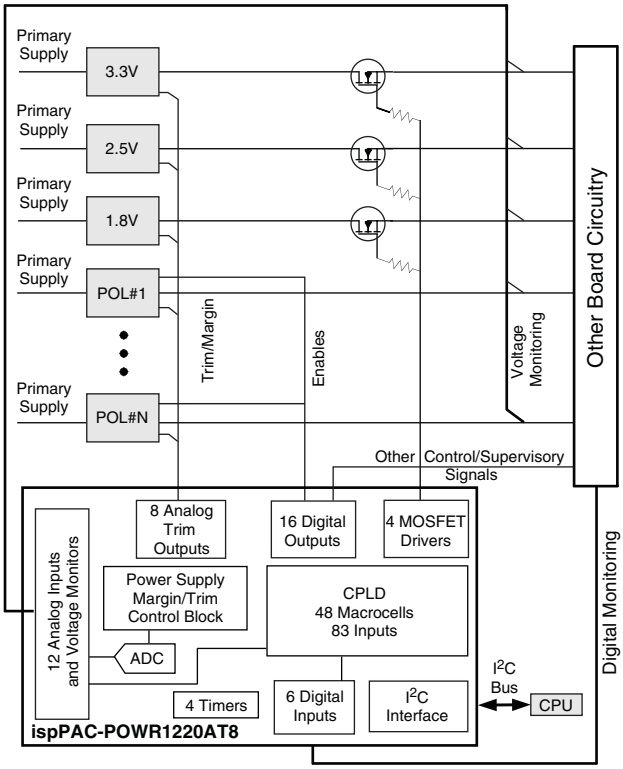
In-System Programmable Power Supply Monitoring, Sequencing and Margining Controller

September 2013 **Data Sheet DS1015**

Features

- **Monitor, Control, and Margin Multiple Power Supplies**
  - Simultaneously monitors up to 12 power supplies
  - Provides up to 20 output control signals
  - Provides up to eight analog outputs for margining/trimming power supply voltages
  - Programmable digital and analog circuitry
- **Power Supply Margin and Trim Functions**
  - Trim and margin up to eight power supplies
  - Dynamic voltage control through I^2C
  - Four hardware selectable voltage profiles
  - Independent Digital Closed-Loop Trim function for each output
- **Embedded PLD for Sequence Control**
  - 48-macrocell CPLD implements both state machines and combinatorial logic functions
- **Embedded Programmable Timers**
  - Four independent timers
  - 32µs to 2 second intervals for timing sequences
- **Analog Input Monitoring**
  - 12 independent analog monitor inputs
  - Differential inputs for remote ground sense
  - Two programmable threshold comparators per analog input
  - Hardware window comparison
  - 10-bit ADC for I^2C monitoring
- **High-Voltage FET Drivers**
  - Power supply ramp up/down control
  - Programmable current and voltage output
  - Independently configurable for FET control or digital output
- **2-Wire (I^2C/SMBus™ Compatible) Interface**
  - Comparator status monitor
  - ADC readout
  - Direct control of inputs and outputs
  - Power sequence control
  - Dynamic trimming/margining control
- **3.3V Operation, Wide Supply Range 2.8V to 3.96V**
  - In-system programmable through JTAG
  - Industrial temperature range: -40°C to +85°C
  - 100-pin TQFP package, lead-free option

Application Block Diagram



Description

The Lattice Power Manager II ispPAC-POWR1220AT8 is a general-purpose power-supply monitor, sequence and margin controller, incorporating both in-system programmable logic and in-system programmable analog functions implemented in non-volatile E^2CMOS® technology. The ispPAC-POWR1220AT8 device provides 12 independent analog input channels to monitor up to 12 power supply test points. Each of these input channels offers a differential input to support remote ground sensing, and has two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. Six general-purpose digital inputs are also provided for miscellaneous control functions.

The ispPAC-POWR1220AT8 provides 20 open-drain digital outputs that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for supervisory and general-purpose logic interface functions. Four of these outputs

(HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers. In high-voltage mode these outputs can provide up to 12V for driving the gates of n-channel MOSFETs so that they can be used as high-side power switches controlling the supplies with a programmable ramp rate for both ramp up and ramp down.

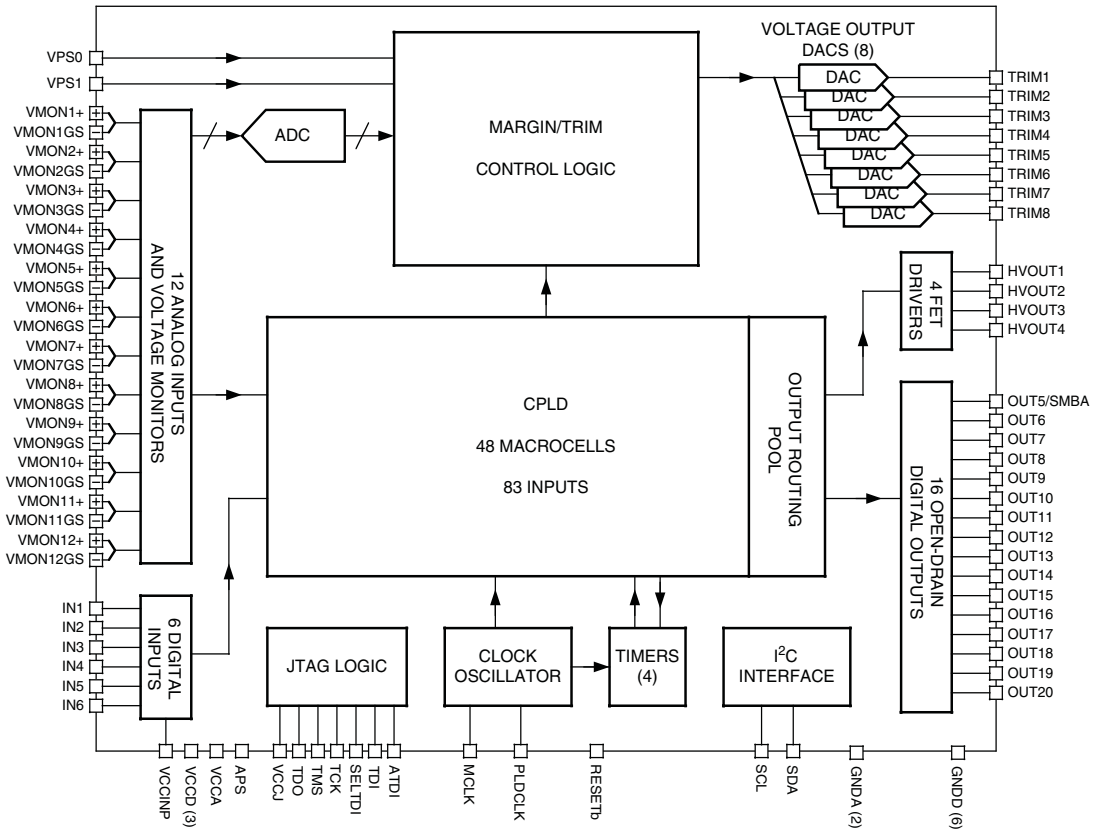
The ispPAC-POWR1220AT8 incorporates a 48-macrocell CPLD that can be used to implement complex state machine sequencing for the control of multiple power supplies as well as combinatorial logic functions. The status of all of the comparators on the analog input channels as well as the general purpose digital inputs are used as inputs by the CPLD array, and all digital outputs may be controlled by the CPLD. Four independently programmable timers can create delays and time-outs ranging from 32µs to 2 seconds. The CPLD is programmed using Logi-Builder™, an easy-to-learn language integrated into the PAC-Designer® software. Control sequences are written to monitor the status of any of the analog input channel comparators or the digital inputs.

In addition to the sequence control functions, the ispPAC-POWR1220AT8 incorporates eight DACs for generating trimming voltage to control the output voltage of a DC-DC converter. The trimming voltage can be set to four hardware selectable preset values (voltage profiles) or can be dynamically loaded in to the DAC through the I^2C bus. Additionally, each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode. The operating voltage profile can either be selected using external hardware pins or through the PLD outputs.

The on-chip 10-bit A/D converter can both be used to monitor the V_{MON} voltage through the I^2C bus as well as for implementing digital closed loop mode for maintaining the output voltage of all power supplies controlled by the monitoring and trimming section of the ispPAC-POWR1220AT8 device.

The I^2C bus/SMBus interface allows an external microcontroller to measure the voltages connected to the V_{MON} inputs, read back the status of each of the V_{MON} comparator and PLD outputs, control logic signals IN2 to IN5, control the output pins, and load the DACs for the generation of the trimming voltage of the external DC-DC converter.

Figure 1. ispPAC-POWR1220AT8 Block Diagram



Pin Descriptions

Number	Name	Pin Type	Voltage Range	Description
89	VPS0	Digital Input	VCCD	Trim Select Input 0 Registered by MCLK
90	VPS1	Digital Input	VCCD	Trim Select Input 1 Registered by MCLK
97	IN1[2]	Digital Input	VCCINP[1]	PLD Logic Input 1 Registered by MCLK
1	IN2[3]	Digital Input	VCCINP[1]	PLD Logic Input 2 Registered by MCLK
2	IN3[3]	Digital Input	VCCINP[1]	PLD Logic Input 3 Registered by MCLK
4	IN4[3]	Digital Input	VCCINP[1]	PLD Logic Input 4 Registered by MCLK
6	IN5[3]	Digital Input	VCCINP[1]	PLD Logic Input 5 Registered by MCLK
7	IN6[3]	Digital Input	VCCINP[1]	PLD Logic Input 6 Registered by MCLK
47	VMON1	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 1 Input
46	VMON1GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 1 Ground Sense
50	VMON2	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 2 Input
48	VMON2GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 2 Ground Sense
52	VMON3	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 3 Input
51	VMON3GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 3 Ground Sense
54	VMON4	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 4 Input
53	VMON4GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 4 Ground Sense
56	VMON5	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 5 Input
55	VMON5GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 5 Ground Sense
58	VMON6	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 6 Input
57	VMON6GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 6 Ground Sense
62	VMON7	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 7 Input
61	VMON7GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 7 Ground Sense
64	VMON8	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 8 Input
63	VMON8GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 8 Ground Sense
66	VMON9	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 9 Input
65	VMON9GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 9 Ground Sense
68	VMON10	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 10 Input
67	VMON10GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 10 Ground Sense
70	VMON11	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 11 Input
69	VMON11GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 11 Ground Sense
72	VMON12	Analog Input	-0.3V to 5.75V[4]	Voltage Monitor 12 Input
71	VMON12GS	Analog Input	-0.2V to 0.3V[5]	Voltage Monitor 12 Ground Sense
3, 22, 36, 43, 88, 98	GNDD[8]	Ground	Ground	Digital Ground
45, 87	GNDA[8]	Ground	Ground	Analog Ground
13, 38, 94	VCCD[7]	Power	2.8V to 3.96V	Core VCC, Main Power Supply
60	VCCA[7]	Power	2.8V to 3.96V	Analog Power Supply
5	VCCINP	Power	2.25V to 5.5V	VCC for IN[1:6] Inputs
33	VCCJ	Power	2.25V to 3.6V	VCC for JTAG Logic Interface Pins
39	APS[10]	Power	3.0V to 3.6V	VCC for E^2 Programming when the Device is **NOT** Powered by V_{CCD} or V_{CCA}
86	HVOUT1	Open Drain Output[6]	0V to 12V	Open-Drain Output 1
		Current Source/Sink	12.5µA to 100µA Source 100µA to 3000µA Sink	High-voltage FET Gate Driver 1

Pin Descriptions (Cont.)

Number	Name	Pin Type	Voltage Range	Description
85	HVOUT2	Open Drain Output[6]	0V to 12V	Open-Drain Output 2
		Current Source/Sink	12.5µA to 100µA Source 100µA to 3000µA Sink	High-voltage FET Gate Driver 2
42	HVOUT3	Open Drain Output[6]	0V to 12V	Open-Drain Output 3
		Current Source/Sink	12.5µA to 100µA Source 100µA to 3000µA Sink	High-voltage FET Gate Driver 3
40	HVOUT4	Open Drain Output[6]	0V to 12V	Open-Drain Output 4
		Current Source/Sink	12.5µA to 100µA Source 100µA to 3000µA Sink	High-voltage FET Gate Driver 4
8	OUT5_SMBA	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 5, (SMBUS Alert Active Low)
9	OUT6	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 6
10	OUT7	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 7
11	OUT8	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 8
12	OUT9	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 9
14	OUT10	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 10
15	OUT11	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 11
16	OUT12	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 12
17	OUT13	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 13
18	OUT14	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 14
19	OUT15	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 15
20	OUT16	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 16
21	OUT17	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 17
23	OUT18	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 18
24	OUT19	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 19
25	OUT20	Open Drain Output[6]	0V to 5.5V	Open-Drain Output 20
84	TRIM1	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 1
83	TRIM2	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 2
82	TRIM3	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 3
80	TRIM4	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 4
79	TRIM5	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 5
75	TRIM6	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 6
74	TRIM7	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 7

Pin Descriptions (Cont.)

Number	Name	Pin Type	Voltage Range	Description
73	TRIM8	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 8
91	RESETb[9]	Digital I/O	0V to 3.96V	Device Reset (Active Low)
95	PLDCLK	Digital Output	0V to 3.96V	250kHz PLD Clock Output (Tristate), CMOS Output
96	MCLK	Digital I/O	0V to 3.96V	8MHz Clock I/O (Tristate), CMOS Drive
34	TDO	Digital Output	0V to 5.5V	JTAG Test Data Out
37	TCK	Digital Input	0V to 5.5V	JTAG Test Clock Input
28	TMS	Digital Input	0V to 5.5V	JTAG Test Mode Select
31	TDI	Digital Input	0V to 5.5V	JTAG Test Data In, TDISEL pin = 1
30	ATDI	Digital Input	0V to 5.5V	JTAG Test Data In (Alternate), TDISEL Pin = 0
32	TDISEL	Digital Input	0V to 5.5V	Select TDI/ATDI Input
92	SCL	Digital Input	0V to 5.5V	I^2C Serial Clock Input
93	SDA	Digital I/O	0V to 5.5V	I^2C Serial Data, Bi-directional Pin
44, 59	RESERVED			Reserved - Do Not Connect
26, 27, 29, 35, 41, 49, 76, 77, 78, 81, 99, 100	NC			No Internal Connection

1. [IN1...IN6] are inputs to the PLD. The thresholds for these pins are referenced by the voltage on VCCINP.
2. IN1 pin can also be controlled through JTAG interface.
3. [IN2..IN6] can also be controlled through I^2C/SMBus interface.
4. The VMON inputs can be biased independently from VCCA. Unused VMONs should be tied to GNDD.
5. The VMONGS inputs are the ground sense line for each given VMON pin. The VMON input pins along with the VMONGS ground sense pins implement a differential pair for each voltage monitor to allow remote sense at the load. VMONGS lines must be connected and are not to exceed -0.2V - +0.3V in reference to the GNDA pin.
6. Open-drain outputs require an external pull-up resistor to a supply.
7. VCCD and VCCA pins must be connected together on the circuit board.
8. GNDA and GNDD pins must be connected together on the circuit board.
9. The RESETb pin should only be used for cascading two or more ispPAC-POWR1220AT8 devices.
10. The APS pin **MUST** be left floating when VCCD and VCCA are powered.

Absolute Maximum Ratings

Absolute maximum ratings are shown in the table below. Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions of this specification is not implied.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}	Core supply		-0.5	4.5	V
V_{CCA}	Analog supply		-0.5	4.5	V
V_{CCINP}	Digital input supply (IN[1:6])		-0.5	6	V
V_{CCJ}	JTAG logic supply		-0.5	6	V
APS[1]	Alternate E^2 programming supply[1]		-0.5	4	V
V_{IN}	Digital input voltage (all digital I/O pins)		-0.5	6	V
V_{MON+}	V_{MON} input voltage		-0.5	6	V
V_{MONGS}	V_{MON} input voltage ground sense		-0.5	6	V
V_{TRI}	Voltage applied to tri-stated pins	HVOUT[1:4]	-0.5	13.3	V
		OUT[5:20]	-0.5	6	V
$I_{SINKMAXTOTAL}$	Maximum sink current on any output			23	mA
T_S	Storage temperature		-65	150	°C
T_A	Ambient temperature		-65	125	°C

1. The APS pin **MUST** be left floating when VCCD and VCCA are powered.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}, V_{CCA}	Core supply voltage at pin		2.8	3.96	V
V_{CCINP}	Digital input supply for IN[1:6] at pin		2.25	5.5	V
V_{CCJ}	JTAG logic supply voltage at pin		2.25	3.6	V
APS	Alternate E^2 programming supply at pin	V_{CCD} and V_{CCA} powered	No Connect Must Be Left Floating		
		V_{CCD} and V_{CCA} not powered	3.0	3.6	V
V_{IN}	Input voltage at digital input pins		-0.3	5.5	V
V_{MON}	Input voltage at V_{MON} pins		-0.3	5.9	V
V_{MONGS}	Input voltage at V_{MONGS} pins		-0.2	0.3	V
V_{OUT}	Open-drain output voltage	OUT[5:20] pins	-0.3	5.5	V
		HVOUT[1:4] pins in open-drain mode	-0.3	13.0	V
T_{APROG}	Ambient temperature during programming		-40	85	°C
T_A	Ambient temperature	Power applied	-40	85	°C

ESD Performance

Pin Group	ESD Stress	Min.	Units
All pins	HBM	2000	V
	CDM	1000	V

Analog Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}[1]	Supply current				40	mA
I_{CCINP}	Supply current				5	mA
I_{CCJ}	Supply current				1	mA
I_{CCPROG}	Supply current	During programming cycle			40	mA

1. Includes currents on V_{CCD} and V_{CCA} supplies.

Voltage Monitors

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input resistance		55	65	75	kΩ
C_{IN}	Input capacitance			8		pF
V_{MON} Range	Programmable trip-point range		0.075		5.734	V
V_Z Sense	Near-ground sense threshold		70	75	80	mV
V_{MON} Accuracy	Absolute accuracy of any trip-point[1]			0.2	0.7	%
HYST	Hysteresis of any trip-point (relative to setting)			1		%
CMR	Common mode rejection			60		dB

1. Guaranteed by characterization across V_{CCA} range, operating temperature, process.

High Voltage FET Drivers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PP}	Gate driver output voltage	12V setting[1]	11.5	12	12.5	V
		10V setting	9.6	10	10.4	
		8V setting	7.7	8	8.3	
		6V setting	5.8	6	6.2	
I_{OUTSRC}	Gate driver source current (HIGH state)	Four settings in software		12.5		µA
				25		
				50		
				100		
$I_{OUTSINK}$	Gate driver sink current (LOW state)	FAST OFF mode	2000	3000		µA
		Controlled ramp settings		100		
				250		
				500		

1. 12V setting only available on the ispPAC-POWR1220AT8-02.

Margin/Trim DAC Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution			8(7+sign)		bits
FSR	Full scale range			+/-320		mV
LSB	LSB step size			2.5		mV
I_{OUT}	Output source/sink current		-200		200	µA
BPZ	Bipolar zero output voltage (code=80h)	Offset 1		0.6		V
		Offset 2		0.8		
		Offset 3		1.0		
		Offset 4		1.25		
TS	TrimCell output voltage settling time[1]	DAC code changed from 80H to FFH or 80H to 00H			2.5	ms
		Single DAC code change		256		µs
C_LOAD	Maximum load capacitance				50	pF
$T_{UPDATEM}$	Update time through I^2C port[2]	MCLK = 8MHz		260		µs
TOSE	Total open loop supply voltage error[3]	Full scale DAC corresponds to ±5% supply voltage variation	-1%		+1%	V/V

1. To 1% of set value with 50pf load connected to trim pins.
2. Total time required to update a single TRIMx output value by setting the associated DAC through the I^2C port.
3. This is the total resultant error in the trimmed power supply output voltage referred to any DAC code due to the DAC's INL, DNL, gain, output impedance, offset error and bipolar offset error across the industrial temperature range and the ispPAC-POWR1200AT8 operating V_{CCA} and V_{CCD} ranges.

ADC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	ADC Resolution			10		Bits
$T_{CONVERT}$	Conversion Time	Time from I^2C Request			200	µs
V_{IN}	Input range Full Scale	Programmable Attenuator = 1	0		2.048	V
		Programmable Attenuator = 3	0		5.9[1]	V
ADC Step Size	LSB	Programmable Attenuator = 1		2		mV
		Programmable Attenuator = 3		6		mV
Eattenuator	Error Due to Attenuator	Programmable Attenuator = 3		+/- 0.1		%

1. Maximum voltage is limited by V_{MONX} pin (theoretical maximum is 6.144V).

ADC Error Budget Across Entire Operating Temperature Range

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
TADC Error	Total Measurement Error at Any Voltage[1]	Measurement Range 600 mV - 2.048V, VMONxGS > -100mV, Attenuator =1	-8	+/-4	8	mV
		Measurement Range 600 mV - 2.048V, VMONxGS > -200mV, Attenuator =1		+/-6		mV
		Measurement Range 0 - 600 mV, VMONxGS > -200mV, Attenuator =1		+/-10		mV

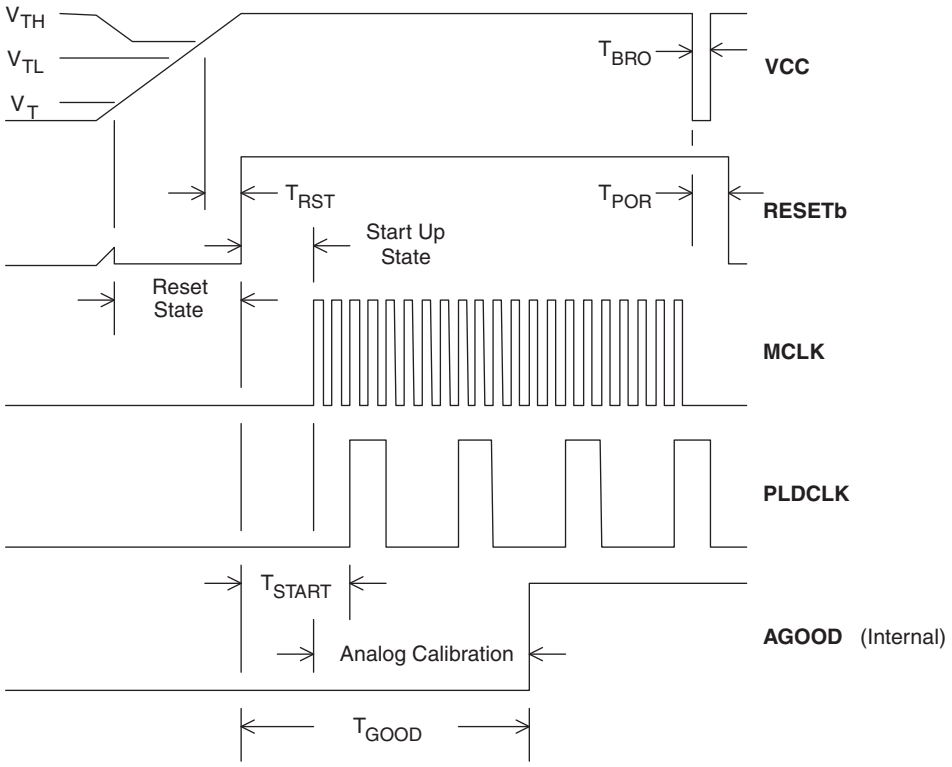
1. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specs of the ADC.

Power-On Reset

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{RST}	Delay from V_{TH} to start-up state				100	µs
T_{START}	Delay from RESETb HIGH to PLDCLK rising edge			5	10	µs
T_{GOOD}	Power-on reset to valid VMON comparator output and AGOOD is true				2.5	ms
T_{BRO}	Minimum duration brown out required to trigger RESETb		1		5	µs
T_{POR}	Delay from brown out to reset state.				13	µs
V_{TL}	Threshold below which RESETb is LOW[1]				2.3	V
V_{TH}	Threshold above which RESETb is HIGH[1]		2.7			V
V_T	Threshold above which RESETb is valid[1]		0.8			V
C_L	Capacitive load on RESETb for master/slave operation				200	pF

1. Corresponds to VCCA and VCCD supply voltages.

Figure 2. ispPAC-POWR1220ATE Power-On Reset



AC/Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Monitors						
t_{PD16}	Propagation delay input to output glitch filter OFF			16		µs
t_{PD64}	Propagation delay input to output glitch filter ON			64		µs
Oscillators						
f_{CLK}	Internal master clock frequency (MCLK)		7.6	8	8.4	MHz
f_{CLKEXT}	Externally applied master clock (MCLK)		7.2		8.8	MHz
f_{PLDCLK}	PLDCLK output frequency	f_{CLK} = 8MHz		250		kHz
Timers						
Timeout Range	Range of programmable timers (128 steps)	f_{CLK} = 8MHz	0.032		1966	ms
Resolution	Spacing between available adjacent timer intervals				13	%
Accuracy	Timer accuracy	f_{CLK} = 8MHz	-6.67		-12.5	%

Digital Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL},I_{IH}	Input leakage, no pull-up/pull-down				+/-10	µA
$I_{OH-HVOUT}$	Output leakage current	HVOUT[1:4] in open drain mode and pulled up to 12V		35	60	µA
I_{PU}	Input pull-up current (TMS, TDI, TDISEL, ATDI, MCLK)			70		µA
V_{IL}	Voltage input, logic low[1]	VPS[0:1], TDI, TMS, ATDI, TDISEL, 3.3V supply			0.8	V
		VPS[0:1], TDI, TMS, ATDI, TDISEL, 2.5V supply			0.7	
		SCL, SDA			30% V_{CCD}	
		IN[1:6]			30% V_{CCINP}	
V_{IH}	Voltage input, logic high[1]	VPS[0:1], TDI, TMS, ATDI, TDISEL, 3.3V supply	2.0			V
		VPS[0:1], TDI, TMS, ATDI, TDISEL, 2.5V supply	1.7			
		SCL, SDA	70% V_{CCD}		V_{CCD}	
		IN[1:6]	70% V_{CCINP}		V_{CCINP}	
V_{OL}	HVOUT[1:4] (open drain mode),	I_{SINK} = 10mA			0.8	V
	OUT[5:20]	I_{SINK} = 20mA			0.8	
	TDO, MCLK, PLDCLK, SDA	I_{SINK} = 4mA			0.4	
V_{OH}	TDO, MCLK, PLDCLK	I_{SRC} = 4mA			V_{CCD} - 0.4	V
$I_{SINKTOTAL}$	All digital outputs				130	mA

1. VPS[0:1], SCL, SDA referenced to V_{CCD}; IN[1:6] referenced to V_{CCINP}; TDO, TDI, TMS, ATDI, TDISEL referenced to V_{CCJ}.

I²C Port Characteristics

Symbol	Definition	100KHz		400KHz		Units
		Min.	Max.	Min.	Max.	
F_{I^2C}	I²C clock/data rate		100[1]		400[1]	KHz
$T_{SU;STA}$	After start	4.7		0.6		us
$T_{HD;STA}$	After start	4		0.6		us
$T_{SU;DAT}$	Data setup	250		100		ns
$T_{SU;STO}$	Stop setup	4		0.6		us
$T_{HD;DAT}$	Data hold; SCL= Vih_min = 2.1V	0.3	3.45	0.3	0.9	us
T_{LOW}	Clock low period	4.7		1.3		us
T_{HIGH}	Clock high period	4		0.6		us
T_F	Fall time; 2.25V to 0.65V		300		300	ns
T_R	Rise time; 0.65V to 2.25V		1000		300	ns
$T_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
T_{POR}	Device must be operational after power-on reset	500		500		ms
T_{BUF}	Bus free time between stop and start condition	4.7		1.3		us

1. If F_{I^2C} is less than 50kHz, then the ADC DONE status bit is not guaranteed to be set after a valid conversion request is completed. In this case, waiting for the $T_{CONVERT}$ minimum time after a convert request is made is the only way to guarantee a valid conversion is ready for readout. When F_{I2C} is greater than 50kHz, ADC conversion complete is ensured by waiting for the DONE status bit.

Timing for JTAG Operations

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{ISPEN}	Program enable delay time		10	—	—	µs
t_{ISPDIS}	Program disable delay time		30	—	—	µs
t_{HVDIS}	High voltage discharge time, program		30	—	—	µs
t_{HVDIS}	High voltage discharge time, erase		200	—	—	µs
t_{CEN}	Falling edge of TCK to TDO active		—	—	15	ns
t_{CDIS}	Falling edge of TCK to TDO disable		—	—	15	ns
t_{SU1}	Setup time		5	—	—	ns
t_H	Hold time		10	—	—	ns
t_{CKH}	TCK clock pulse width, high		20	—	—	ns
t_{CKL}	TCK clock pulse width, low		20	—	—	ns
f_{MAX}	Maximum TCK clock frequency		—	—	25	MHz
t_{CO}	Falling edge of TCK to valid output		—	—	15	ns
t_{PWV}	Verify pulse width		30	—	—	µs
t_{PWP}	Programming pulse width		20	—	—	ms

Figure 3. Erase (User Erase or Erase All) Timing Diagram

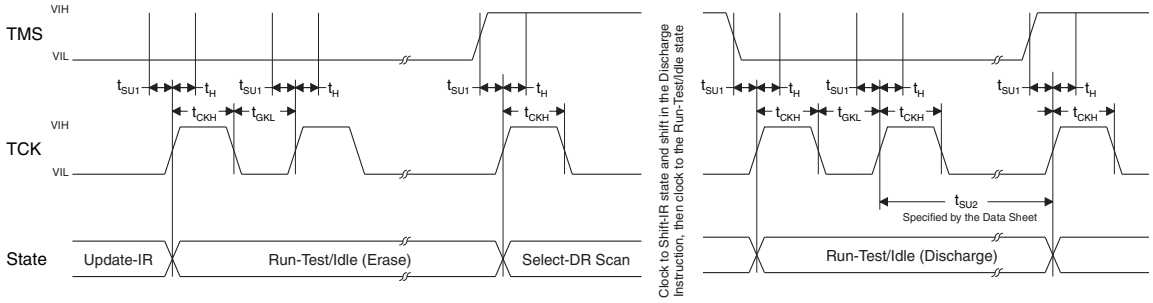


Figure 4. Programming Timing Diagram

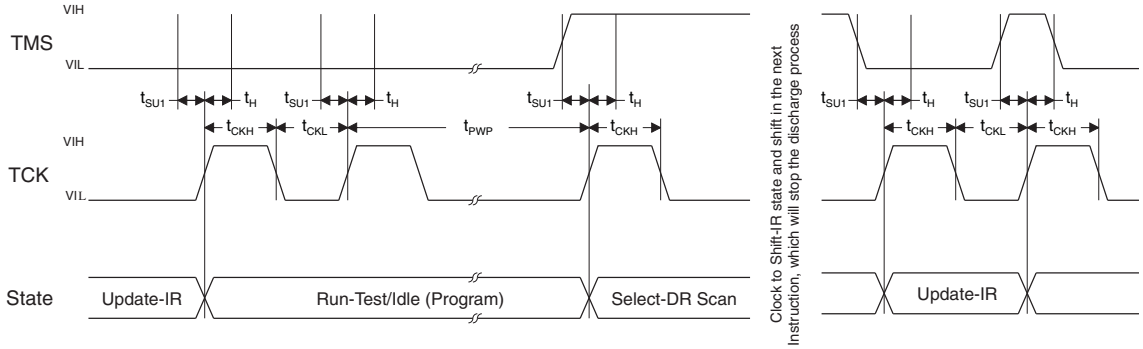


Figure 5. Verify Timing Diagram

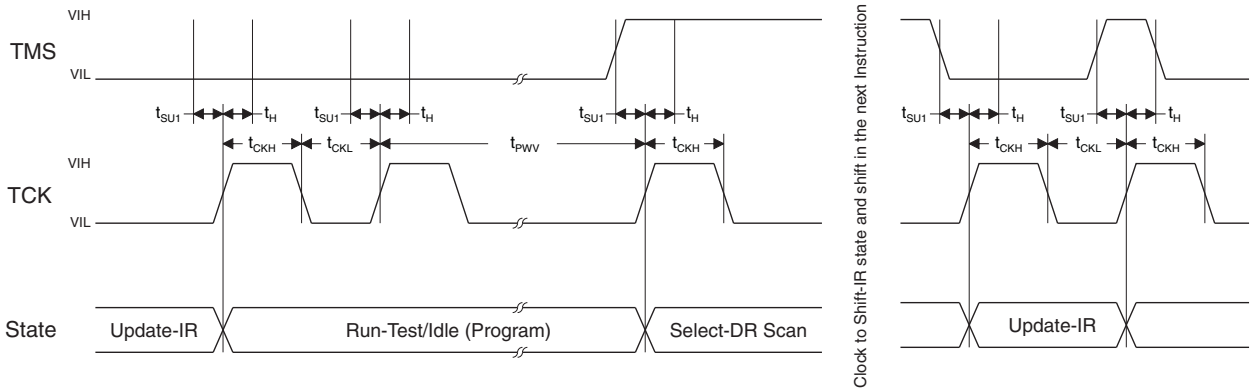
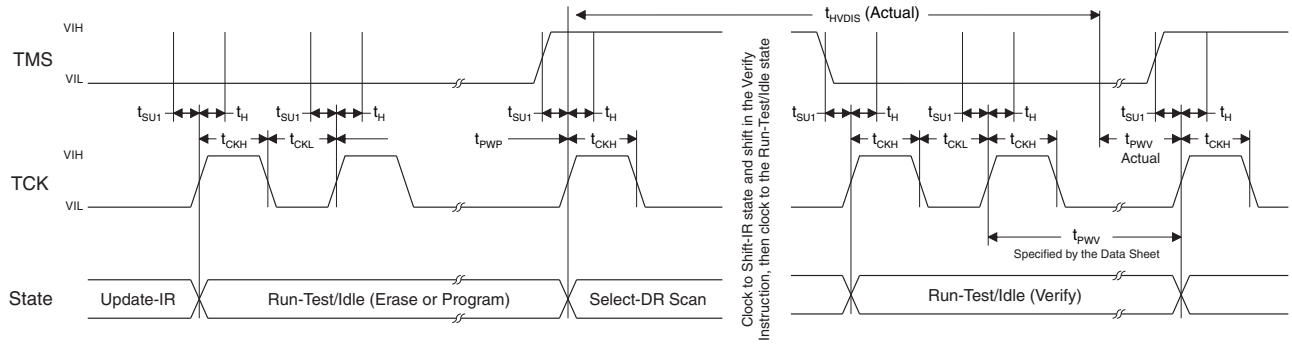


Figure 6. Discharge Timing Diagram



Theory of Operation

Analog Monitor Inputs

The ispPAC-POWR1220AT8 provides 12 independently programmable voltage monitor input circuits as shown in Figure 7. Two individually programmable trip-point comparators are connected to an analog monitoring input. Each comparator reference has 368 programmable trip points over the range of 0.664V to 5.734V. Additionally, a 75mV ‘zero-detect’ threshold is selectable which allows the voltage monitors to determine if a monitored signal has dropped to ground level. This feature is especially useful for determining if a power supply’s output has decayed to a substantially inactive condition after it has been switched off.

Figure 7. ispPAC-POWR1220AT8 Voltage Monitors

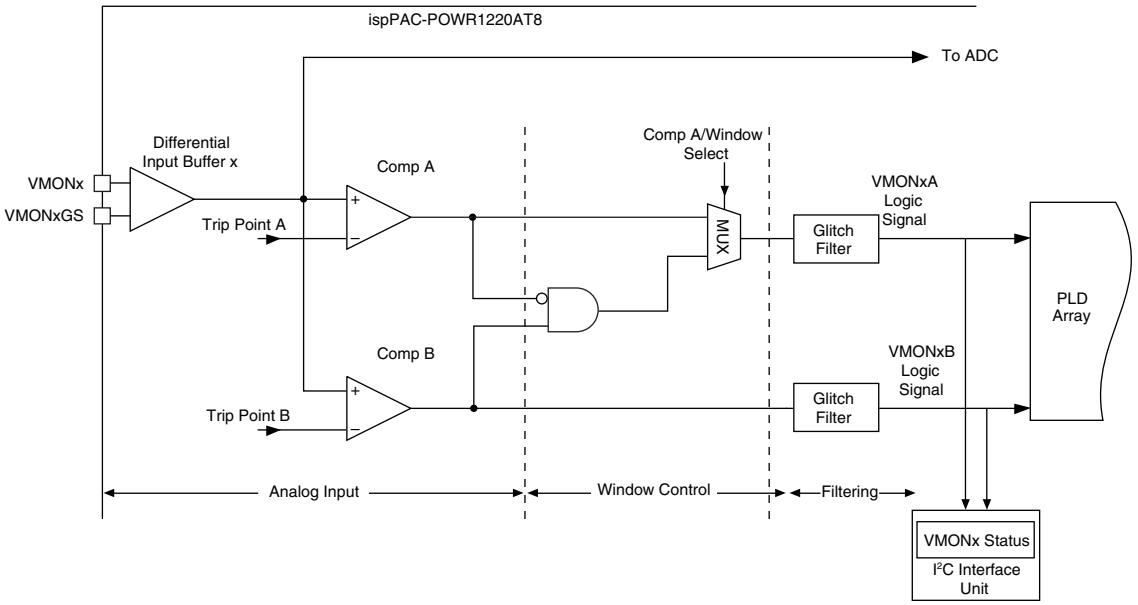


Figure 7 shows the functional block diagram of one of the 12 voltage monitor inputs - 'x' (where x = 1...12). Each voltage monitor can be divided into three sections: Analog Input, Window Control, and Filtering. The first section provides a differential input buffer to monitor the power supply voltage through VMONx+ (to sense the positive terminal of the supply) and VMONxGS (to sense the power supply ground). Differential voltage sensing minimizes inaccuracies in voltage measurement with ADC and monitor thresholds due to the potential difference between the ispPAC-POWR1220AT8 device ground and the ground potential at the sensed node on the circuit board.

The voltage output of the differential input buffer is monitored by two individually programmable trip-point comparators, shown as CompA and CompB. Table 1 shows all 368 trip points spanning the range 0.664V to 5.734V to which a comparator's threshold can be set.

Each comparator outputs a HIGH signal to the PLD array if the voltage at its positive terminal is greater than its programmed trip point setting, otherwise it outputs a LOW signal.

A hysteresis of approximately 1% of the setpoint is provided by the comparators to reduce false triggering as a result of input noise. The hysteresis provided by the voltage monitor is a function of the input divider setting. Table 3 lists the typical hysteresis versus voltage monitor trip-point.

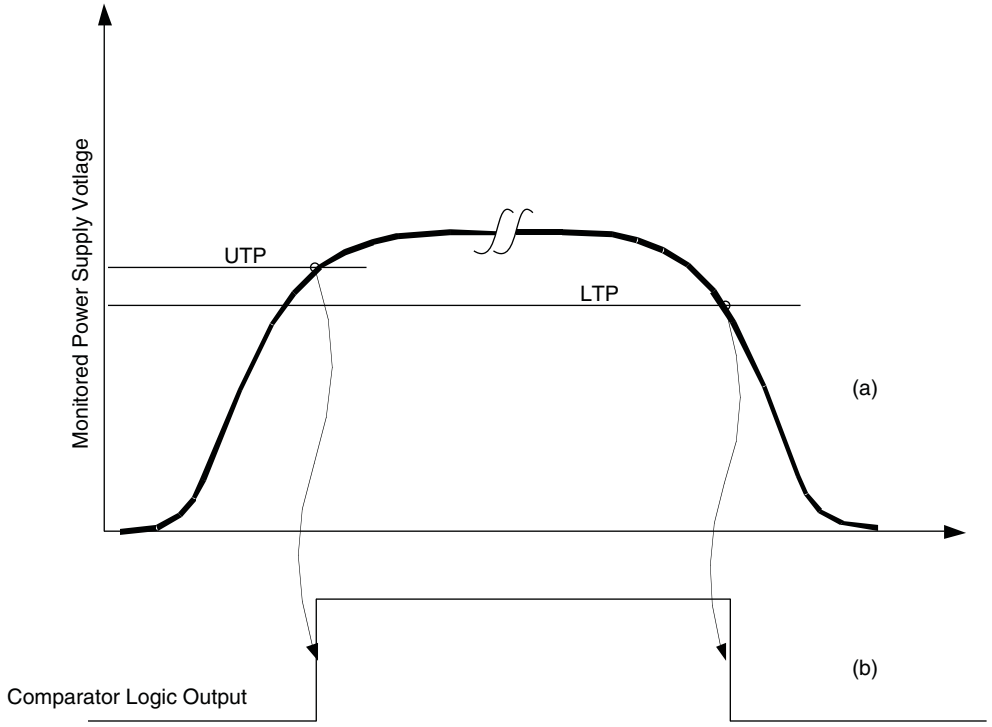
AGOOD Logic Signal

All the VMON comparators auto-calibrate immediately after a power-on reset event. During this time, the digital glitch filters are also initialized. This process completion is signalled by an internally generated logic signal: AGOOD. All logic using the VMON comparator logic signals must wait for the AGOOD signal to become active.

Programmable Over-Voltage and Under-Voltage Thresholds

Figure 8 (a) shows the power supply ramp-up and ramp-down voltage waveforms. Because of hysteresis, the comparator outputs change state at different thresholds depending on the direction of excursion of the monitored power supply.

Figure 8. (a) Power Supply Voltage Ramp-up and Ramp-down Waveform and the Resulting Comparator Output, (b) Corresponding to Upper and Lower Trip Points



During power supply ramp-up the comparator output changes from logic 0 to 1 when the power supply voltage crosses the upper trip point (UTP). During ramp down the comparator output changes from logic state 1 to 0 when the power supply voltage crosses the lower trip point (LTP). To monitor for over voltage fault conditions, the UTP should be used. To monitor under-voltage fault conditions, the LTP should be used.

Tables 1 and 2 show both the under-voltage and over-voltage trip points, which are automatically selected in software depending on whether the user is monitoring for an over-voltage condition or an under-voltage condition.

Table 1. Trip Point Table Used For Over-Voltage Detection

Fine Range Setting	Coarse Range Setting											
	1	2	3	4	5	6	7	8	9	10	11	12
1	0.790	0.941	1.120	1.333	1.580	1.885	2.244	2.665	3.156	3.758	4.818	5.734
2	0.786	0.936	1.114	1.326	1.571	1.874	2.232	2.650	3.139	3.738	4.792	5.703
3	0.782	0.930	1.108	1.319	1.563	1.864	2.220	2.636	3.123	3.718	4.766	5.674
4	0.778	0.926	1.102	1.312	1.554	1.854	2.209	2.622	3.106	3.698	4.741	5.643
5	0.773	0.921	1.096	1.305	1.546	1.844	2.197	2.607	3.089	3.678	4.715	5.612
6	0.769	0.916	1.090	1.298	1.537	1.834	2.185	2.593	3.072	3.657	4.689	5.581
7	0.765	0.911	1.084	1.290	1.529	1.825	2.173	2.579	3.056	3.637	4.663	5.550
8	0.761	0.906	1.078	1.283	1.520	1.815	2.161	2.565	3.039	3.618	4.638	5.520
9	0.756	0.901	1.072	1.276	1.512	1.805	2.149	2.550	3.022	3.598	4.612	5.489
10	0.752	0.896	1.066	1.269	1.503	1.795	2.137	2.536	3.005	3.578	4.586	5.459
11	0.748	0.891	1.060	1.262	1.495	1.785	2.125	2.522	2.988	3.558	4.561	5.428
12	0.744	0.886	1.054	1.255	1.486	1.774	2.113	2.507	2.971	3.537	4.535	5.397
13	0.739	0.881	1.048	1.248	1.478	1.764	2.101	2.493	2.954	3.517	4.509	5.366
14	0.735	0.876	1.042	1.240	1.470	1.754	2.089	2.479	2.937	3.497	4.483	5.336
15	0.731	0.871	1.036	1.233	1.461	1.744	2.077	2.465	2.920	3.477	4.457	5.305
16	0.727	0.866	1.030	1.226	1.453	1.734	2.064	2.450	2.903	3.457	4.431	5.274
17	0.723	0.861	1.024	1.219	1.444	1.724	2.052	2.436	2.886	3.437	4.406	5.244
18	0.718	0.856	1.018	1.212	1.436	1.714	2.040	2.422	2.869	3.416	4.380	5.213
19	0.714	0.851	1.012	1.205	1.427	1.704	2.028	2.407	2.852	3.396	4.355	5.183
20	0.710	0.846	1.006	1.198	1.419	1.694	2.016	2.393	2.836	3.376	4.329	5.152
21	0.706	0.841	1.000	1.190	1.410	1.684	2.004	2.379	2.819	3.356	4.303	5.121
22	0.701	0.836	0.994	1.183	1.402	1.673	1.992	2.365	2.802	3.336	4.277	5.090
23	0.697	0.831	0.988	1.176	1.393	1.663	1.980	2.350	2.785	3.316	4.251	5.059
24	0.693	0.826	0.982	1.169	1.385	1.653	1.968	2.337	2.768	3.296	4.225	5.030
25	0.689	0.821	0.976	1.162	1.376	1.643	1.956	2.323	2.752	3.276	4.199	4.999
26	0.684	0.816	0.970	1.155	1.369	1.633	1.944	2.309	2.735	3.256	4.174	4.968
27	0.680	0.810	0.964	1.148	1.361	1.623	1.932	2.294	2.718	3.236	4.149	4.937
28	0.676	0.805	0.958	1.140	1.352	1.613	1.920	2.280	2.701	3.216	4.123	4.906
29	0.672	0.800	0.952	1.133	1.344	1.603	1.908	2.266	2.684	3.196	4.097	4.876
30	0.668	0.795	0.946	1.126	—	1.593	1.896	2.251	—	3.176	4.071	4.845
Low-V Sense	75mV											

Table 2. Trip Point Table Used For Under-Voltage Detection

Fine Range Setting	Coarse Range Setting											
	1	2	3	4	5	6	7	8	9	10	11	12
1	0.786	0.936	1.114	1.326	1.571	1.874	2.232	2.650	3.139	3.738	4.792	5.703
2	0.782	0.930	1.108	1.319	1.563	1.864	2.220	2.636	3.123	3.718	4.766	5.674
3	0.778	0.926	1.102	1.312	1.554	1.854	2.209	2.622	3.106	3.698	4.741	5.643
4	0.773	0.921	1.096	1.305	1.546	1.844	2.197	2.607	3.089	3.678	4.715	5.612
5	0.769	0.916	1.090	1.298	1.537	1.834	2.185	2.593	3.072	3.657	4.689	5.581
6	0.765	0.911	1.084	1.290	1.529	1.825	2.173	2.579	3.056	3.637	4.663	5.550
7	0.761	0.906	1.078	1.283	1.520	1.815	2.161	2.565	3.039	3.618	4.638	5.520
8	0.756	0.901	1.072	1.276	1.512	1.805	2.149	2.550	3.022	3.598	4.612	5.489
9	0.752	0.896	1.066	1.269	1.503	1.795	2.137	2.536	3.005	3.578	4.586	5.459
10	0.748	0.891	1.060	1.262	1.495	1.785	2.125	2.522	2.988	3.558	4.561	5.428
11	0.744	0.886	1.054	1.255	1.486	1.774	2.113	2.507	2.971	3.537	4.535	5.397
12	0.739	0.881	1.048	1.248	1.478	1.764	2.101	2.493	2.954	3.517	4.509	5.366
13	0.735	0.876	1.042	1.240	1.470	1.754	2.089	2.479	2.937	3.497	4.483	5.336
14	0.731	0.871	1.036	1.233	1.461	1.744	2.077	2.465	2.920	3.477	4.457	5.305
15	0.727	0.866	1.030	1.226	1.453	1.734	2.064	2.450	2.903	3.457	4.431	5.274
16	0.723	0.861	1.024	1.219	1.444	1.724	2.052	2.436	2.886	3.437	4.406	5.244
17	0.718	0.856	1.018	1.212	1.436	1.714	2.040	2.422	2.869	3.416	4.380	5.213
18	0.714	0.851	1.012	1.205	1.427	1.704	2.028	2.407	2.852	3.396	4.355	5.183
19	0.710	0.846	1.006	1.198	1.419	1.694	2.016	2.393	2.836	3.376	4.329	5.152
20	0.706	0.841	1.000	1.190	1.410	1.684	2.004	2.379	2.819	3.356	4.303	5.121
21	0.701	0.836	0.994	1.183	1.402	1.673	1.992	2.365	2.802	3.336	4.277	5.090
22	0.697	0.831	0.988	1.176	1.393	1.663	1.980	2.350	2.785	3.316	4.251	5.059
23	0.693	0.826	0.982	1.169	1.385	1.653	1.968	2.337	2.768	3.296	4.225	5.030
24	0.689	0.821	0.976	1.162	1.376	1.643	1.956	2.323	2.752	3.276	4.199	4.999
25	0.684	0.816	0.970	1.155	1.369	1.633	1.944	2.309	2.735	3.256	4.174	4.968
26	0.680	0.810	0.964	1.148	1.361	1.623	1.932	2.294	2.718	3.236	4.149	4.937
27	0.676	0.805	0.958	1.140	1.352	1.613	1.920	2.280	2.701	3.216	4.123	4.906
28	0.672	0.800	0.952	1.133	1.344	1.603	1.908	2.266	2.684	3.196	4.097	4.876
29	0.668	0.795	0.946	1.126	1.335	1.593	1.896	2.251	2.667	3.176	4.071	4.845
30	0.664	0.790	0.940	1.119	—	1.583	1.884	2.236	—	3.156	4.045	4.815
Low-V Sense	75mV											

Table 3. Comparator Hysteresis vs. Trip-Point

Trip-point Range (V)		Hysteresis (mV)
Low Limit	High Limit	
0.664	0.79	8
0.79	0.941	10
0.94	1.12	12
1.119	1.333	14
1.326	1.58	17
1.583	1.885	20
1.884	2.244	24
2.236	2.665	28
2.65	3.156	34
3.156	3.758	40
4.045	4.818	51
4.815	5.734	61
75 mV		0 (Disabled)

The window control section of the voltage monitor circuit is an AND gate (with inputs: an inverted COMPA "ANDed" with COMPB signal) and a multiplexer that supports the ability to develop a 'window' function without using any of the PLD's resources. Through the use of the multiplexer, voltage monitor's 'A' output may be set to report either the status of the 'A' comparator, or the window function of both comparator outputs. The voltage monitor's 'A' output indicates whether the input signal is between or outside the two comparator thresholds. **Important:** This windowing function is only valid in cases where the threshold of the 'A' comparator is set to a value higher than that of the 'B' comparator. Table 4 shows the operation of window function logic.

Table 4. Voltage Monitor Windowing Logic

Input Voltage	Comp A	Comp B	Window (B and Not A)	Comment
V_{IN} < Trip-point B < Trip-point A	0	0	0	Outside window, low
Trip-point B < V_{IN} < Trip-point A	0	1	1	Inside window
Trip-point B < Trip-point A < V_{IN}	1	1	0	Outside window, high

Note that when the 'A' output of the voltage monitor circuit is set to windowing mode, the 'B' output continues to monitor the output of the 'B' comparator. This can be useful in that the 'B' output can be used to augment the windowing function by determining if the input is above or below the windowing range.

The third section in the ispPAC-POWR1220AT8's input voltage monitor is a digital filter. When enabled, the comparator output will be delayed by a filter time constant of 64 µS, and is especially useful for reducing the possibility of false triggering from noise that may be present on the voltages being monitored. When the filter is disabled, the comparator output will be delayed by 16µS. In both cases, enabled or disabled, the filters also provide synchronization of the input signals to the PLD clock. This synchronous sampling feature effectively eliminates the possibility of race conditions from occurring in any subsequent logic that is implemented in the ispPAC-POWR1220AT8's internal PLD logic.

The comparator status can be read from the I^2C interface. For details on the I^2C interface, please refer to the I^2C/SMBUS Interface section of this data sheet.

VMON Voltage Measurement with the On-chip Analog to Digital Converter (ADC)

The ispPAC-POWR1220 has an on-chip analog to digital converter that can be used for measuring the voltages at the VMON inputs. The ADC is also used in closed loop trimming of DC-DC converters. Close loop trimming is covered later in this document.

Figure 9. ADC Monitoring VMON1 to VMON12

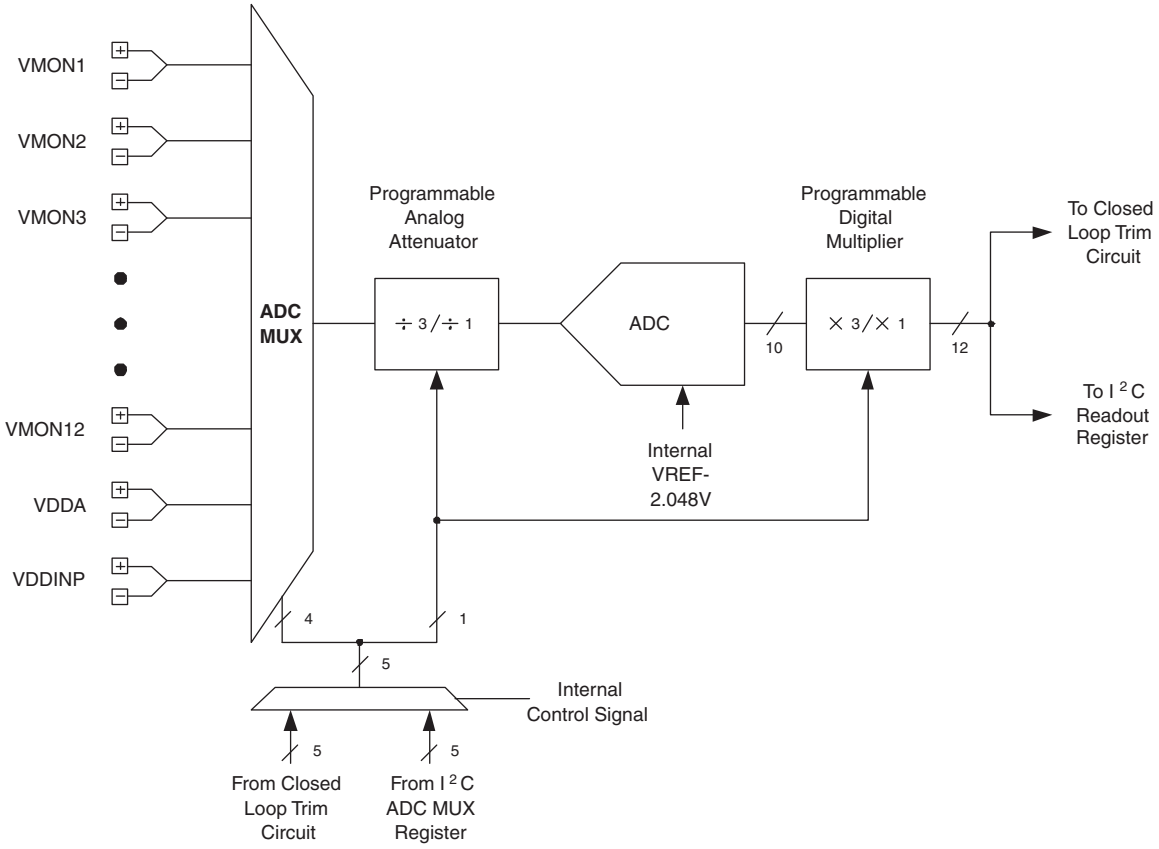


Figure 9 shows the ADC circuit arrangement within the ispPAC-POWR1220AT8 device. The ADC can measure all analog input voltages through the multiplexer, ADC MUX. The programmable attenuator between the ADC mux and the ADC can be configured as divided-by-3 or divided-by-1 (no attenuation). The divided-by-3 setting is used to measure voltages from 0V to 6V range and divided-by-1 setting is used to measure the voltages from 0V to 2V range.

A microcontroller can place a request for any VMON voltage measurement at any time through the I^2C bus. Upon the receipt of an I^2C command, the ADC will be connected to the I^2C selected VMON through the ADC MUX. The ADC output is then latched into the I^2C readout registers.

Calculation

The algorithm to convert the ADC code to the corresponding voltage takes into consideration the attenuation bit value. In other words, if the attenuation bit is set, then the 10-bit ADC result is automatically multiplied by 3 to calculate the actual voltage at that V_{MON} input. Thus, the I^2C readout register is 12 bits instead of 10 bits. The following formula can always be used to calculate the actual voltage from the ADC code.

Voltage at the VMONx Pins

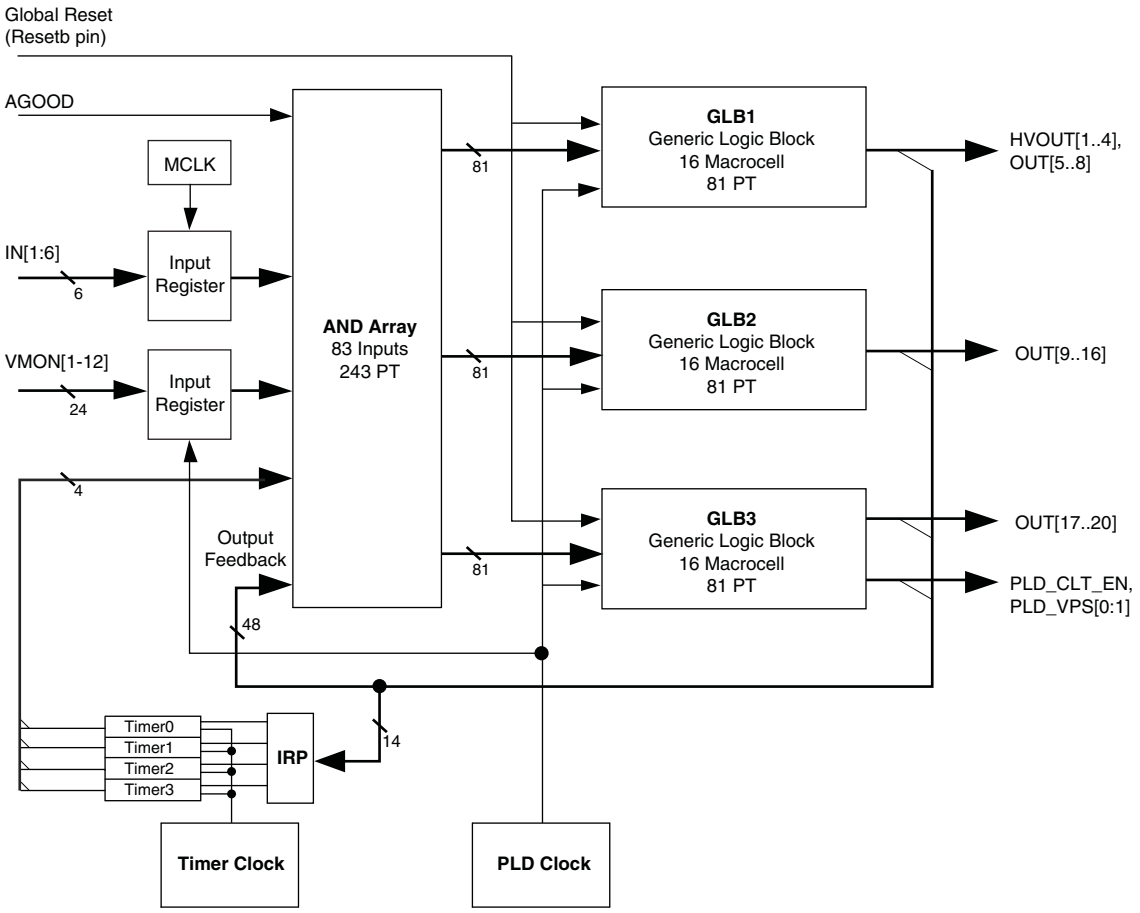
VMON = ADC code (12 bits[1], converted to decimal) * 2mV

[1]Note: ADC_VALUE_HIGH (8 bits), ADC_VALUE_LOW (4 bits) read from I^2C/SMBUS interface

PLD Block

Figure 10 shows the ispPAC-POWR1220AT8 PLD architecture, which is derived from the Lattice's ispMACH™ 4000 CPLD. The PLD architecture allows the flexibility in designing various state machines and control functions used for power supply management. The AND array has 83 inputs and generates 243 product terms. These 243 product terms are divided into three groups of 81 for each of the generic logic blocks, GLB1, GLB2, and GLB3. Each GLB is made up of 16 macrocells. In total, there are 48 macrocells in the ispPAC-POWR1220AT8 device. The output signals of the ispPAC-POWR1220AT8 device are derived from GLBs as shown in Figure 10. Additionally, the GLB3 generates the timer control and trimming block controls.

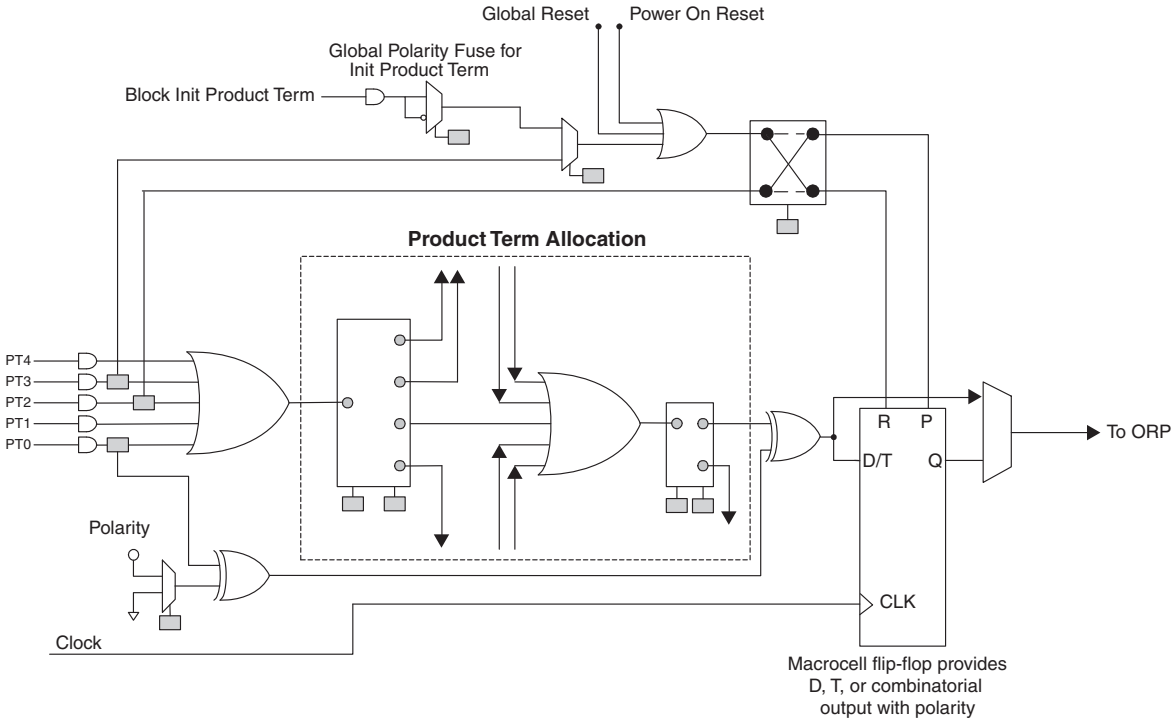
Figure 10. ispPAC-POWR1220AT8 PLD Architecture



Macrocell Architecture

The macrocell shown in Figure 11 is the heart of the PLD. The basic macrocell has five product terms that feed the OR gate and the flip-flop. The flip-flop in each macrocell is independently configured. It can be programmed to function as a D-Type or T-Type flip-flop. Combinatorial functions are realized by bypassing the flip-flop. The polarity control and XOR gates provide additional flexibility for logic synthesis. The flip-flop's clock is driven from the common PLD clock that is generated by dividing the 8 MHz master clock (MCLK) by 32. The macrocell also supports asynchronous reset and preset functions, derived from either product terms, the global reset input, or the power-on reset signal. The resources within the macrocells share routing and contain a product term allocation array. The product term allocation array greatly expands the PLD's ability to implement complex logical functions by allowing logic to be shared between adjacent blocks and distributing the product terms to allow for wider decode functions. All the digital inputs are registered by MCLK and the VMON comparator outputs are registered by the PLD Clock to synchronize them to the PLD logic.

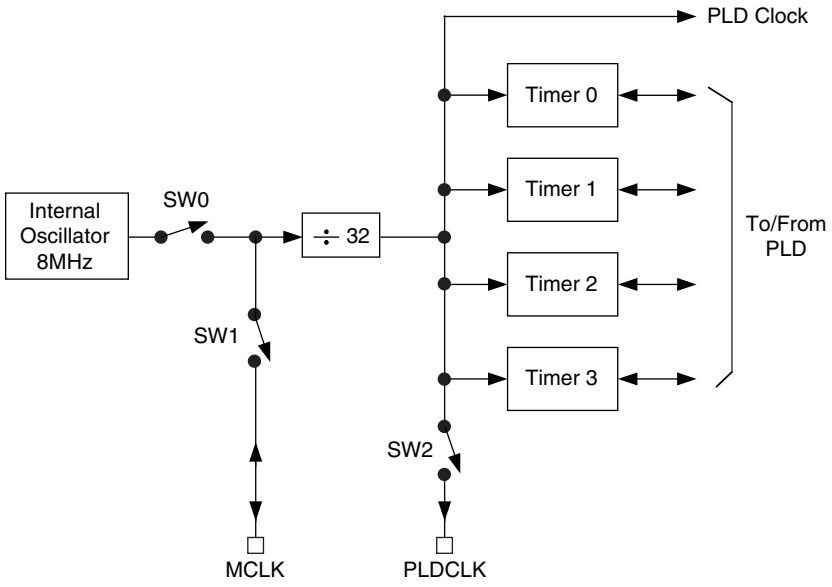
Figure 11. ispPAC-POWR1220AT8 Macrocell Block Diagram



Clock and Timer Functions

Figure 12 shows a block diagram of the ispPAC-POWR1220AT8's internal clock and timer systems. The master clock operates at a fixed frequency of 8MHz, from which a fixed 250kHz PLD clock is derived.

Figure 12. Clock and Timer System



The internal oscillator runs at a fixed frequency of 8 MHz. This signal is used as a source for the PLD and timer clocks. It is also used for clocking the comparator outputs and clocking the digital filters in the voltage monitor circuits, ADC and trim circuits. The ispPAC-POWR1220AT8 can be programmed to operate in three modes: Master

mode, Standalone mode and Slave mode. Table 5 summarizes the operating modes of ispPAC-POWR1220AT8.

Table 5. ispPAC-POWR1220AT8 Operating Modes

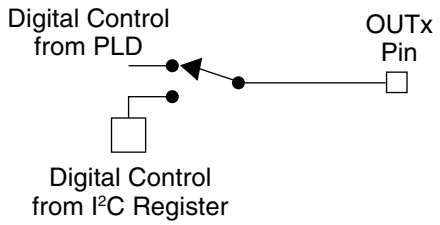
Timer Operating Mode	SW0	SW1	Condition	Comments
Standalone	Closed	Open	When only one ispPAC-POWR1220AT8 is used.	MCLK pin tristated
Master	Closed	Closed	When more than one ispPAC-POWR1220AT8 is used in a board, one of them should be configured to operate in this mode.	MCLK pin outputs 8MHz clock
Slave	Open	Closed	When more than one ispPAC-POWR1220AT8s is used in a board. Other than the master, the rest of the ispPAC-POWR1220AT8s should be programmed as slaves.	MCLK pin is input

A divide-by-32 prescaler divides the internal 8MHz oscillator (or external clock, if selected) down to 250kHz for the PLD clock and for the programmable timers. This PLD clock may be made available on the PLDCLK pin by closing SW2. Each of the four timers provides independent timeout intervals ranging from 32µs to 1.96 seconds in 128 steps.

Digital Outputs

The ispPAC-POWR1220AT8 provides 20 digital outputs, HVOUT[1:4] and OUT[5:20]. Outputs OUT[5:20] are permanently configured as open drain to provide a high degree of flexibility when interfacing to logic signals, LEDs, opto-couplers, and power supply control inputs. The HVOUT[1:4] pins can be configured as either high voltage FET drivers or open drain outputs. Each of these outputs may be controlled either from the PLD or from the I^2C bus. The determination whether a given output is under PLD or I^2C control may be made on a pin-by-pin basis (see Figure 13). For further details on controlling the outputs through I^2C, please see the I^2C/SMBUS Interface section of this data sheet.

Figure 13. Digital Output Pin Configuration



High-Voltage Outputs

In addition to being usable as digital open-drain outputs, the ispPAC-POWR1220AT8's HVOUT1-HVOUT4 output pins can be programmed to operate as high-voltage FET drivers. Figure 14 shows the details of the HVOUT gate drivers. Each of these outputs may be controlled from the PLD or from the I^2C bus (see Figure 14). For further details on controlling the outputs through I^2C, please see the I^2C/SMBUS Interface section of this data sheet.

Figure 14. Basic Function Diagram for an Output in High Voltage MOSFET Gate Driver Mode

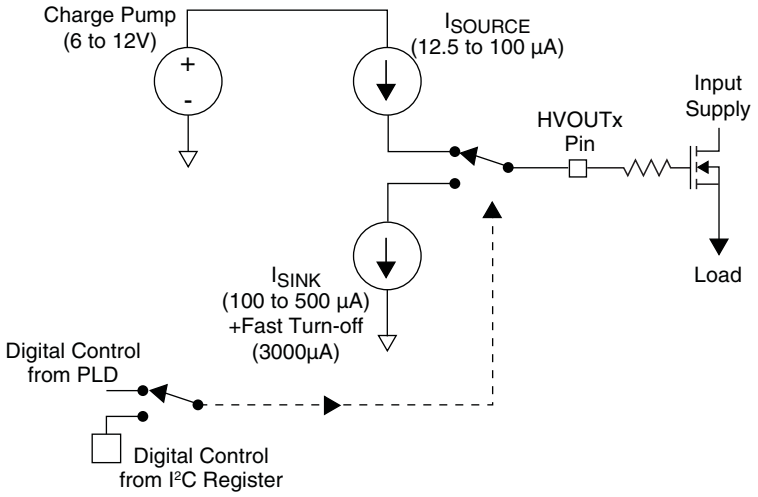


Figure 14 shows the HVOUT circuitry when programmed as a FET driver. In this mode the output either sources current from a charge pump or sinks current. The maximum voltage that the output level at the pin will rise to is also programmable between 6V and 12V. The maximum voltage levels that are required depend on the gate-to-source threshold of the FET being driven and the power supply voltage being switched. The maximum voltage level needs to be sufficient to bias the gate-to-source threshold on and also accommodate the load voltage at the FET's source, since the source pin of the FET to provide a wide range of ramp rates is tied to the supply of the target board. When the HVOUT pin is sourcing current, charging a FET gate, the source current is programmable between 12.5µA and 100µA. When the driver is turned to the off state, the driver will sink current to ground, and this sink current is also programmable between 3000µA and 100µA to control the turn-off rate.

Programmable Output Voltage Levels for HVOUT1- HVOUT4

There are three selectable steps for the output voltage of the FET drivers when in FET driver mode. The voltage that the pin is capable of driving to can be programmed from 6V to 12V in 2V steps.

Controlling Power Supply Output Voltage by Margin/ Trim Block

One of the key features of the ispPAC-POWR1220AT8 is its ability to make adjustments to the power supplies that it may also be monitoring and/or sequencing. This is accomplished through the Trim and Margin Block of the device. The Trim and Margin Block can adjust voltages of up to eight different power supplies through TrimCells as shown in Figure 15. The DC-DC blocks in the figure represent virtually any type of DC power supply that has a trim or voltage adjustment input. This can be an off-the-shelf unit or custom circuit designed around a switching regulator IC.

The interface between the ispPAC-POWR1220AT8 and the DC power supply is represented by a single resistor (R1 to R8) to simplify the diagram. Each of these resistors represents a resistor network.

Other control signals driving the Margin/Trim Block are:

- VPS [1:0] – Control signals from device pins common to all eight TrimCells, which are used to select the active voltage profile for all TrimCells together.
- PLD_VPS[1:0] – Voltage profile selection signals generated by the PLD. These signals can be used instead of the VPS signals from the pins.
- ADC input – Used to determine the trimmed DC-DC converter voltage.
- PLD_CLT_EN – Only from PLD, used to enable closed loop trimming of all TrimCells together.

Next to each DC-DC converter, four voltages are shown. These voltages correspond to the operating voltage profile of the Margin/Trim Block.

When the VPS[1:0] = 00, representing Voltage Profile 0: (Voltage Profile 0 is recommended to be used for the normal circuit operation)

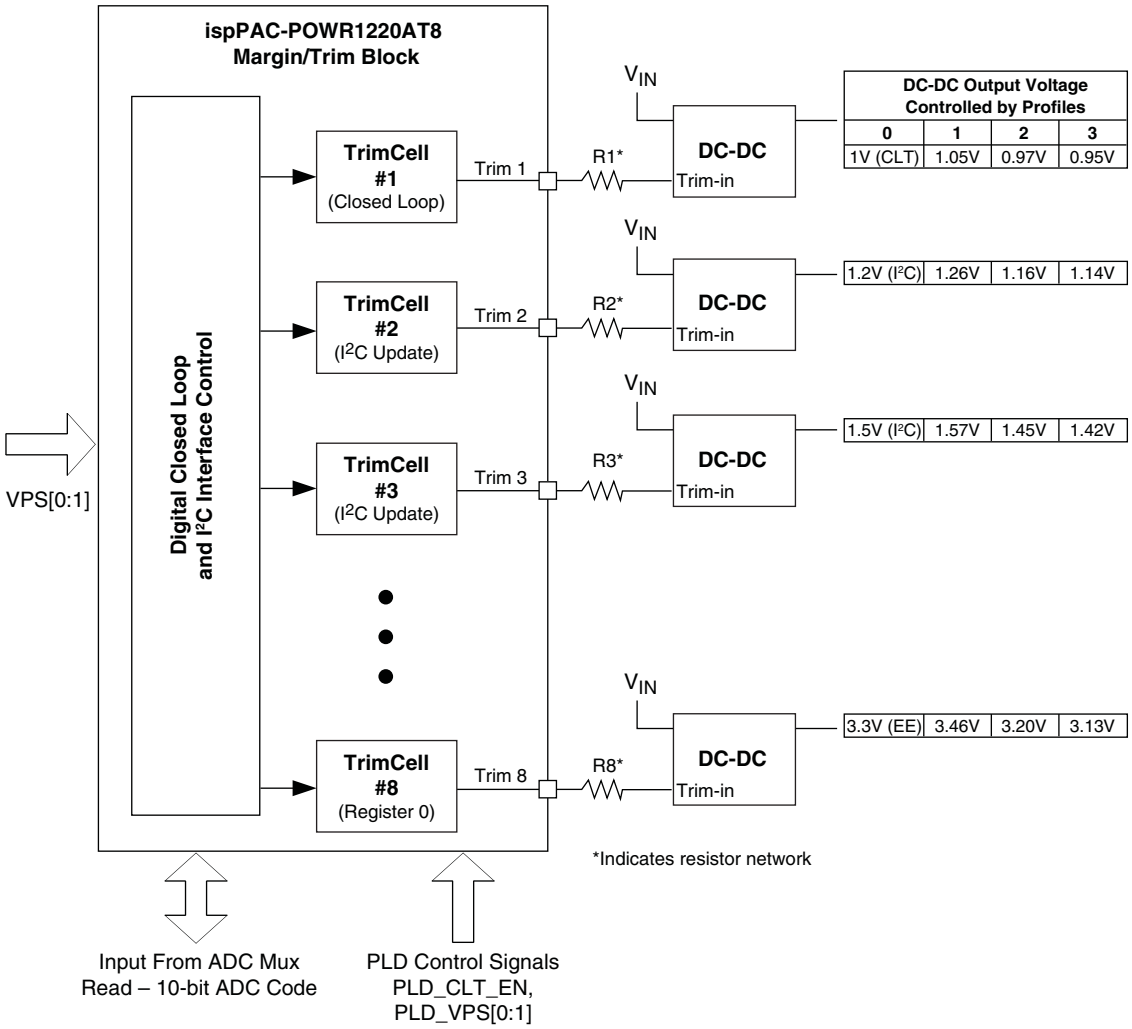
The output voltage of the DC-DC converter controlled by the Trim 1 pin of the ispPAC-POWR1220AT8 will be 1V and that TrimCell is operating in closed loop trim mode. At the same time, the DC-DC converters controlled by Trim 2, Trim 3 and Trim 8 pins output 1.2V, 1.5V and 3.3V respectively.

When the VPS[1:0] = 01, representing Voltage Profile 1 being active:

The DC-DC output voltage controlled by Trim 1, 2, 3, and 8 pins will be 1.05V, 1.26V, 1.57V, and 3.46V. These supply voltages correspond to 5% above their respective normal operating voltage (also called as margin high).

Similarly, when VPS[1:0] = 11, all DC-DC converters are margined low by 5%.

Figure 15. ispPAC-POWR1220AT8 Trim and Margin Block



There are eight TrimCells in the ispPAC-POWR1220AT8 device, enabling simultaneous control of up to eight individual power supplies. Each TrimCell can generate up to four trimming voltages to control the output voltage of the DC-DC converter.