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ispPAC®-POWR6AT6

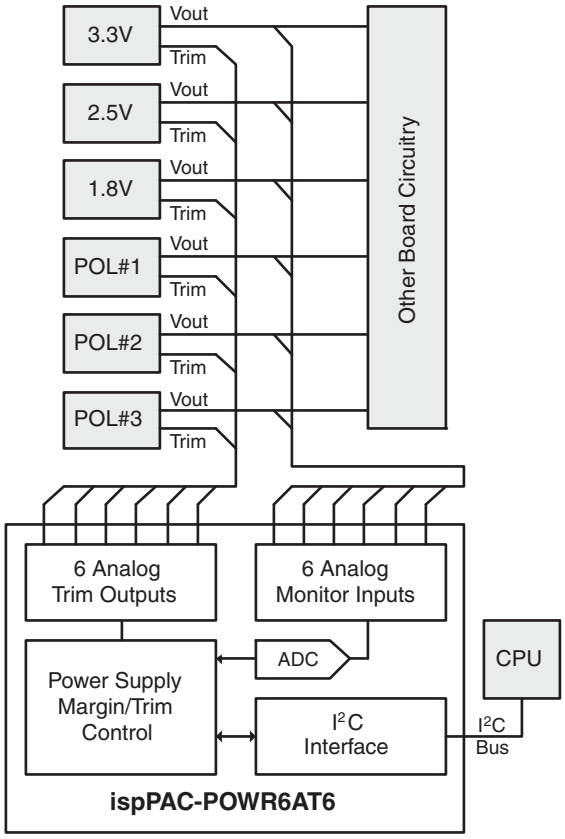
In-System Programmable Power Supply Monitoring and Margining Controller

November 2013 Data Sheet DS1016

Features

- **Power Supply Margin and Trim Functions**
  - Trim and margin up to six power supplies
  - Dynamic voltage control through I^2C
  - Four hardware selectable voltage profiles
  - Independent Digital Closed-Loop Trim function for each output
- **Analog Input Monitoring**
  - Six analog monitor inputs
  - Differential input architecture for accurate remote ground sensing
  - 10-bit ADC for direct voltage measurements
- **2-Wire (I^2C/SMBus™ Compatible) Interface**
  - Readout of the ADC
  - Dynamic trimming/margining control
- **Other Features**
  - Programmable analog circuitry
  - Wide supply range, 2.8V to 3.96V
  - In-system programmable through JTAG
  - Industrial temperature range: -40°C to +85°C
  - 32-pin QFNS (Quad Flat-pack, No lead, Saw-singulated) package[1], only 5mm x 5mm, lead-free option

Application Block Diagram



Description

Lattice's Power Manager II ispPAC-POWR6AT6 is a general-purpose power-supply monitoring and margining controller, incorporating in-system programmable analog functions implemented in non-volatile E^2CMOS® technology. The ispPAC-POWR6AT6 device provides six independent analog input channels to monitor up to six power supply test points. Each of these input channels offers a differential input to support remote ground sensing.

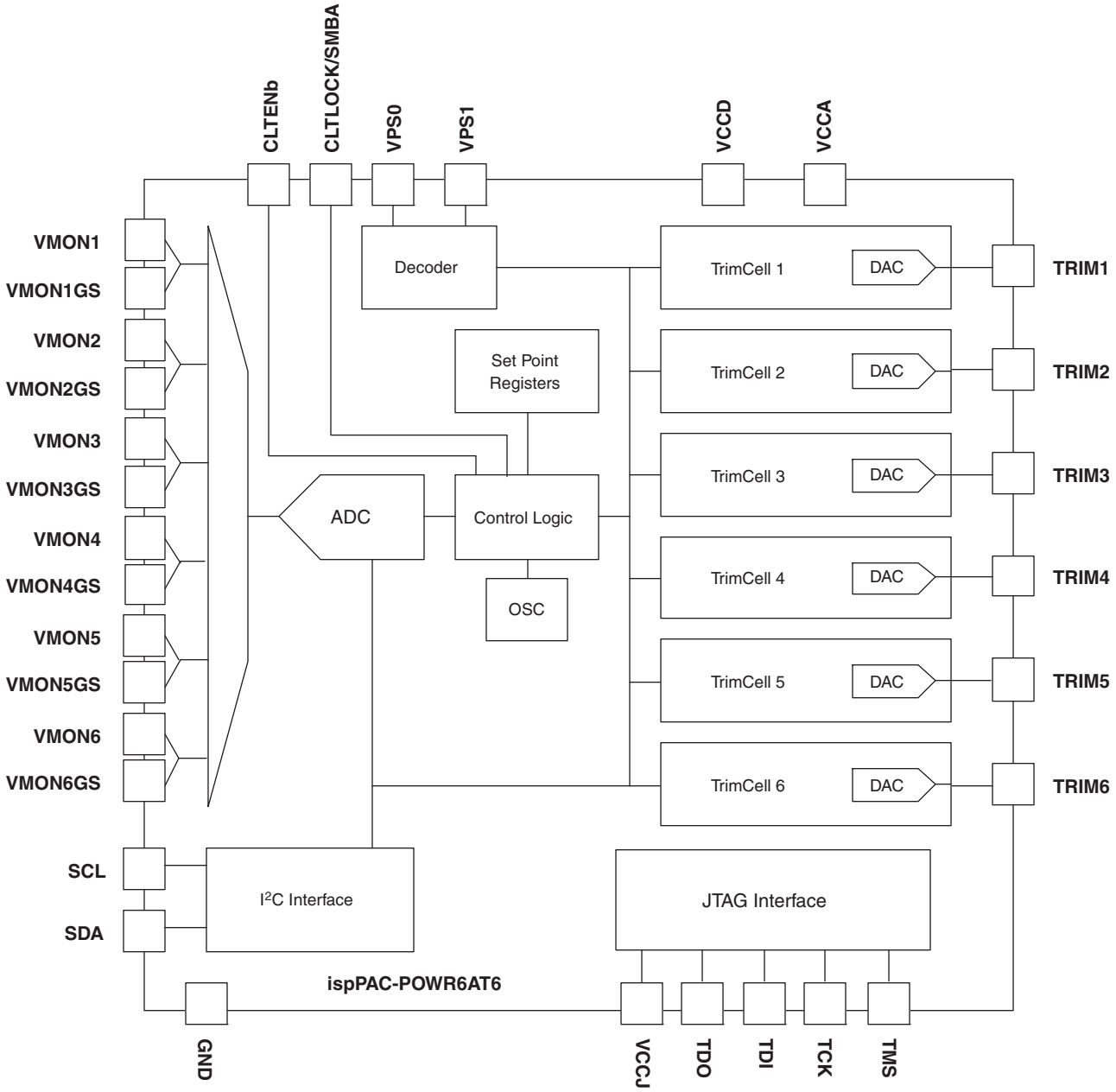
The ispPAC-POWR6AT6 incorporates six DACs for generating a trimming voltage to control the output voltage of a power supply. The trimming voltage can be set to four hardware selectable preset values (voltage profiles) or can be dynamically loaded in to the DAC through the I^2C bus. Additionally, each power supply output voltage can be maintained within 1% tolerance across various load conditions using the Digital Closed Loop Control mode. The operating voltage profile can be selected using external hardware pins.

The on-chip 10-bit A/D converter can both be used to monitor the V_{MON} voltage through the I^2C bus as well as for implementing digital closed loop mode for maintaining the output voltage of all power supplies controlled by the monitoring and trimming section of the ispPAC-POWR6AT6 device.

The I^2C bus/SMBus interface allows an external microcontroller to measure the voltages connected to the V_{MON} analog monitor inputs and load the DACs for the generation of the trimming voltages of the external DC-DC converters.

1. Use 32-pin QFNS package for all new designs. Refer to PCN #13A-08 for 32-pin QFN package discontinuance.

Figure 3-1. ispPAC-POWR6AT6 Block Diagram



Pin Descriptions

Number	Name	Pin Type	Voltage Range	Description
7	VPS0	Digital Input	VCCD	Trim Select Input 0
8	VPS1	Digital Input	VCCD	Trim Select Input 1
6	CLTENb	Digital Input	VCCD	Enables closed loop trim process (asserted low)
9	CLTLOCK/ SMBA	Open Drain Output[1]	0V to 5.5V	Signals that all TrimCells selected for closed-loop trim have reached a trim locked condition. Can be configured to be compliant with SMBus Alert protocol.[2]
15	VMON1	Analog Input	-0.3V to 5.75V	Voltage Monitor 1 Input
14	VMON1GS	Analog Input	-0.3V to 0.3V[3]	Voltage Monitor 1 Ground Sense
17	VMON2	Analog Input	-0.3V to 5.75V	Voltage Monitor 2 Input
16	VMON2GS	Analog Input	-0.3V to 0.3V[3]	Voltage Monitor 2 Ground Sense
19	VMON3	Analog Input	-0.3V to 5.75V	Voltage Monitor 3 Input
18	VMON3GS	Analog Input	-0.3V to 0.3V[3]	Voltage Monitor 3 Ground Sense
21	VMON4	Analog Input	-0.3V to 5.75V	Voltage Monitor 4 Input
20	VMON4GS	Analog Input	-0.3V to 0.3V[3]	Voltage Monitor 4 Ground Sense
23	VMON5	Analog Input	-0.3V to 5.75V	Voltage Monitor 5 Input
22	VMON5GS	Analog Input	-0.3V to 0.3V[3]	Voltage Monitor 5 Ground Sense
25	VMON6	Analog Input	-0.3V to 5.75V	Voltage Monitor 6 Input
24	VMON6GS	Analog Input	-0.3V to 0.3V[3]	Voltage Monitor 6 Ground Sense
32	GND	Ground	Ground	Ground
12	VCCD[4]	Power	2.8V to 3.96V	Core VCC, Main Power Supply
13	VCCA[4]	Power	2.8V to 3.96V	Analog Power Supply
2	VCCJ	Power	2.25V to 3.6V	VCC for JTAG Logic Interface Pins
31	TRIM1	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 1
30	TRIM2	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 2
29	TRIM3	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 3
28	TRIM4	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 4
27	TRIM5	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 5
26	TRIM6	Analog Output	-320mV to +320mV from Programmable DAC Offset	Trim DAC Output 6

Pin Descriptions (Cont.)

Number	Name	Pin Type	Voltage Range	Description
1	TDO	Digital Output		JTAG Test Data Out
3	TCK	Digital Input		JTAG Test Clock Input
5	TMS	Digital Input		JTAG Test Mode Select; Internal Pullup
4	TDI	Digital Input		JTAG Test Data In; Internal Pullup
10	SCL	Digital Input		I^2C Serial Clock Input
11	SDA	Digital I/O		I^2C Serial Data, Bi-directional Pin
Die Pad	NC	No Connection		No Internal Connection

1. Open-drain outputs require an external pull-up resistor to a supply.
2. Normally asserted low, but can be programmed to assert high (open) if desired.
3. The VMONxGS inputs are the ground sense line for each given VMON pin. The VMON input pins along with the VMONxGS ground sense pins implement a differential pair for each voltage monitor to allow remote sense at the load. VMONxGS lines must be connected and are not to exceed -0.3V to +0.3V in reference to the GND pin.
4. VCCA and VCCD pins must be connected together on the circuit board.

Absolute Maximum Ratings

Absolute maximum ratings are shown in the table below. Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions of this specification is not implied.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}	Core supply		-0.5	4.5	V
V_{CCA}	Analog supply		-0.5	4.5	V
V_{CCJ}	JTAG logic supply		-0.5	6	V
V_{IN}	Digital input voltage (all digital I/O pins)		-0.5	6	V
V_{MON+}	V_{MON} input voltage		-0.5	6	V
V_{MONGS}	V_{MON} input voltage ground sense		-0.5	6	V
T_S	Storage temperature		-65	150	°C
T_A	Ambient temperature		-65	125	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}, V_{CCA}	Core supply voltage at pin		2.8	3.96	V
V_{CCJ}	JTAG logic supply voltage at pin		2.25	3.6	V
V_{IN}	Input voltage at digital input pins		-0.3	5.5	V
V_{MON}	Input voltage at V_{MON} pins		-0.3	5.9	V
V_{MONGS}	Input voltage at V_{MONGS} pins		-0.3	0.3	V
V_{OUT}	Open-drain output voltage	CLTLOCK/SMBA	-0.3	5.5	V
T_{APROG}	Ambient temperature during programming	(Note 1)	-40	85	°C
T_A	Ambient temperature	Power applied[1]	-40	85	°C

1. The die pad on the bottom of the QFN/QFNS package does not need to be electrically or thermally connected to ground.

Analog Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}[1]	Supply current				10	mA
I_{CCJ}	Supply current				1	mA

1. Includes currents on V_{CCD} and V_{CCA} supplies.

Analog Voltage Monitor Inputs (V_{MON})

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input resistance	Input mode = Attenuated[1]	50	65	80	k¾
		Input mode = Unattenuated		10		M¾
C_{IN}	Input capacitance			12		pF

1. True for Vmon input voltage from 600mV to 2.048V. Values less than 600mV will see higher input impedance values.

Margin/Trim DAC Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution			8(7+sign)		bits
FSR	Full scale range			+/-320		mV
LSB	LSB step size			2.5		mV
I_{OUT}	Output source/sink current		-200		200	µA
V_{BPZ}	Bipolar zero output voltage (code=80h)	Offset 1		0.6		V
		Offset 2		0.8		
		Offset 3		1.0		
		Offset 4		1.25		
TS	TrimCell output voltage settling time[1]	DAC code changed from 80H to FFH or 80H to 00H			2.5	ms
		Single DAC code change		256		µs
C_LOAD	Maximum load capacitance				50	pF
$T_{UPDATEM}$	Update time through I^2C port[2]			260		µs
TOSE	Total open loop supply voltage error[3]	Full scale DAC corresponds to ±5% supply voltage variation	-1		+1	%

1. To 1% of set value with 50pf load connected to trim pins.
2. Total time required to update a single TRIMx output value by setting the associated DAC through the I^2C port.
3. This is the total resultant error in the trimmed power supply output voltage referred to any DAC code due to the DAC's INL, DNL, gain, output impedance, offset error and bipolar offset error across the industrial temperature range and the ispPAC-POWR6AT6 operating V_{CCA} and V_{CCD} ranges.

ADC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	ADC resolution			10		Bits
VIN	Input range full scale	Programmable attenuator = 1	0		2.048	V
		Programmable attenuator = 3	0		5.75[1]	V
$T_{CONVERT}$	Conversion complete time	Time from I^2C request to complete one conversion cycle			200[2]	µs
ADC Step Size	LSB	Programmable attenuator = 1		2		mV
		Programmable attenuator = 3		6		mV
Eattenuator	Error due to attenuator	Programmable attenuator = 3		+/- 0.1		%

1. Maximum voltage is limited by V_{MONX} pin (theoretical maximum is 6.144V).
2. Minimum time to wait for valid ADC result. Applies when not reading the DONE status bit (via I^2C) to determine ADC.

ADC Error Budget Across Entire Operating Temperature Range

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
TADC Error	Total Measurement Error at Any Voltage[1]	Measurement Range 600 mV to 2.048V, VMONxGS > -100mV, Attenuator =1	-8	+/-4	8	mV
		Measurement Range 600 mV to 2.048V, VMONxGS > -200mV, Attenuator =1		+/-6		mV
		Measurement Range 0 to 600 mV, VMONxGS > -200mV, Attenuator =1		+/-10		mV

1. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specs of the ADC.

Digital Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL},I_{IH}	Input leakage, no pull-up/pull-down				+/-10	µA
I_{PU}	Input pull-up current (TMS, TDI)			70		µA
V_{IL}	Voltage input, logic low[1]	VPS[0:1], TDI, TMS, CLTENb, V_{CCD} = V_{CCJ} = 3.3V			0.8	V
		SCL, SDA			30% V_{CCD}	
		TDI, TMS, V_{CCJ} = 2.5V			0.7	
V_{IH}	Voltage input, logic high[1]	VPS[0:1], TDI, TMS, CLTENb, V_{CCD} = V_{CCJ} = 3.3V	2.0			V
		SCL, SDA	70% V_{CCD}		V_{CCD}	
		TDI, TMS, V_{CCJ} = 2.5V	1.7			
V_{OL}	CLTLOCK/SMBA	I_{SINK} = 20mA			0.8	V

1. CLTENb, VPS[0:1], SCL, SDA referenced to V_{CCD}; TDO, TDI, TMS referenced to V_{CCJ}.

I²C Port Characteristics

Symbol	Definition	100KHz		400KHz		Units
		Min.	Max.	Min.	Max.	
F_{I2C}	I²C clock/data rate		100[1]		400[1]	KHz
$T_{SU;STA}$	After start	4.7		0.6		us
$T_{HD;STA}$	After start	4		0.6		us
$T_{SU;DAT}$	Data setup	250		100		ns
$T_{SU;STO}$	Stop setup	4		0.6		us
$T_{HD;DAT}$	Data hold; SCL= Vih_min = 2.1V	0.3	3.45	0.3	0.9	us
T_{LOW}	Clock low period	4.7		1.3		us
T_{HIGH}	Clock high period	4		0.6		us
T_F	Fall time; 2.25V to 0.65V		300		300	ns
T_R	Rise time; 0.65V to 2.25V		1000		300	ns
$T_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
T_{POR}	Device must be operational after power-on reset	500		500		ms
T_{BUF}	Bus free time between stop and start condition	4.7		1.3		us

1. If F_{I2C} is less than 50kHz, then the ADC DONE status bit is not guaranteed to be set after a valid conversion request is completed. In this case, waiting for the $T_{CONVERT}$ minimum time after a convert request is made is the only way to guarantee a valid conversion is ready for readout. When F_{I2C} is greater than 50kHz, ADC conversion complete is ensured by waiting for the DONE status bit.

Timing for JTAG Operations

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{ISPEN}	Program enable delay time		10	—	—	µs
t_{ISPDIS}	Program disable delay time		30	—	—	µs
t_{HVDIS}	High voltage discharge time, program		30	—	—	µs
t_{HVDIS}	High voltage discharge time, erase		200	—	—	µs
t_{CEN}	Falling edge of TCK to TDO active		—	—	10	ns
t_{CDIS}	Falling edge of TCK to TDO disable		—	—	10	ns
t_{SU1}	Setup time		5	—	—	ns
t_H	Hold time		10	—	—	ns
t_{CKH}	TCK clock pulse width, high		20	—	—	ns
t_{CKL}	TCK clock pulse width, low		20	—	—	ns
f_{MAX}	Maximum TCK clock frequency		—	—	25	MHz
t_{CO}	Falling edge of TCK to valid output		—	—	10	ns
t_{PWV}	Verify pulse width		30	—	—	µs
t_{PWP}	Programming pulse width		20	—	—	ms

Figure 3-2. Erase (User Erase or Erase All) Timing Diagram

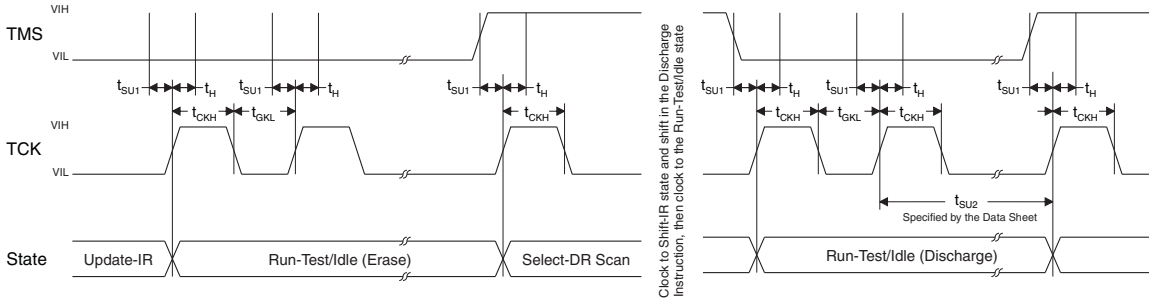


Figure 3-3. Programming Timing Diagram

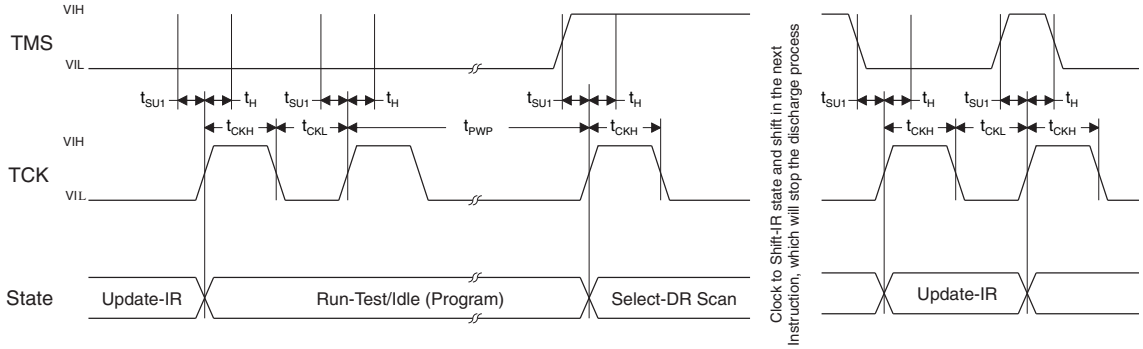


Figure 3-4. Verify Timing Diagram

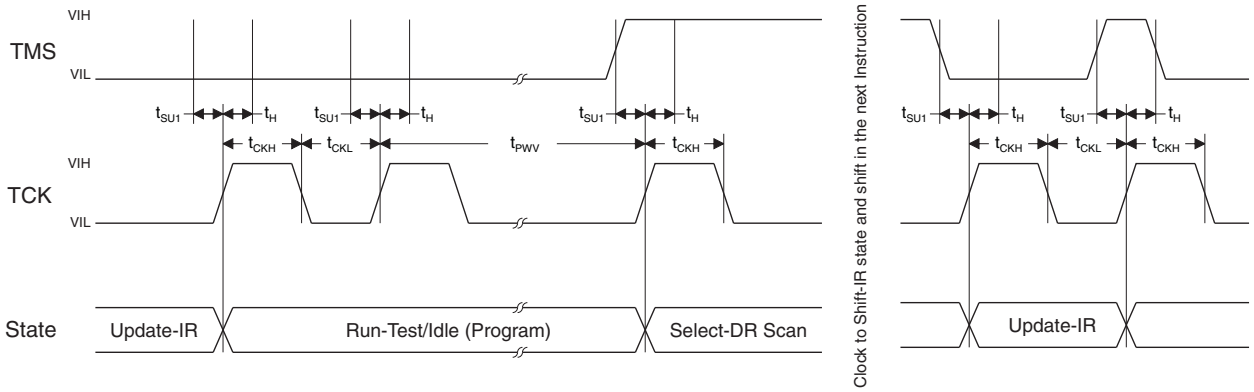
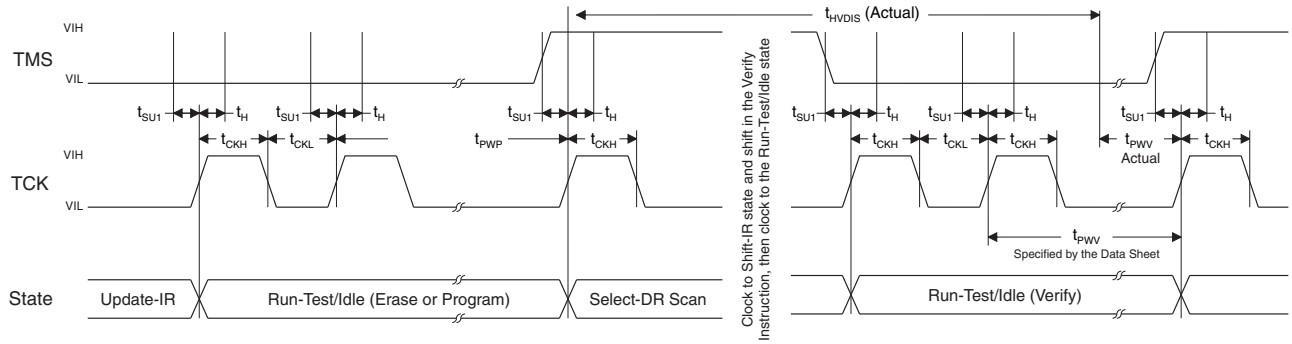


Figure 3-5. Discharge Timing Diagram



Theory of Operation

Voltage Measurement with the On-chip Analog to Digital Converter (ADC)

The ispPAC-POWR6AT6 has an on-chip analog to digital converter that can be used for measuring the voltages at the VMON inputs. The ADC is also used in closed loop trimming of DC-DC converters. Close loop trimming is covered later in this document.

Figure 3-6. ADC Monitoring VMON1 to VMON6

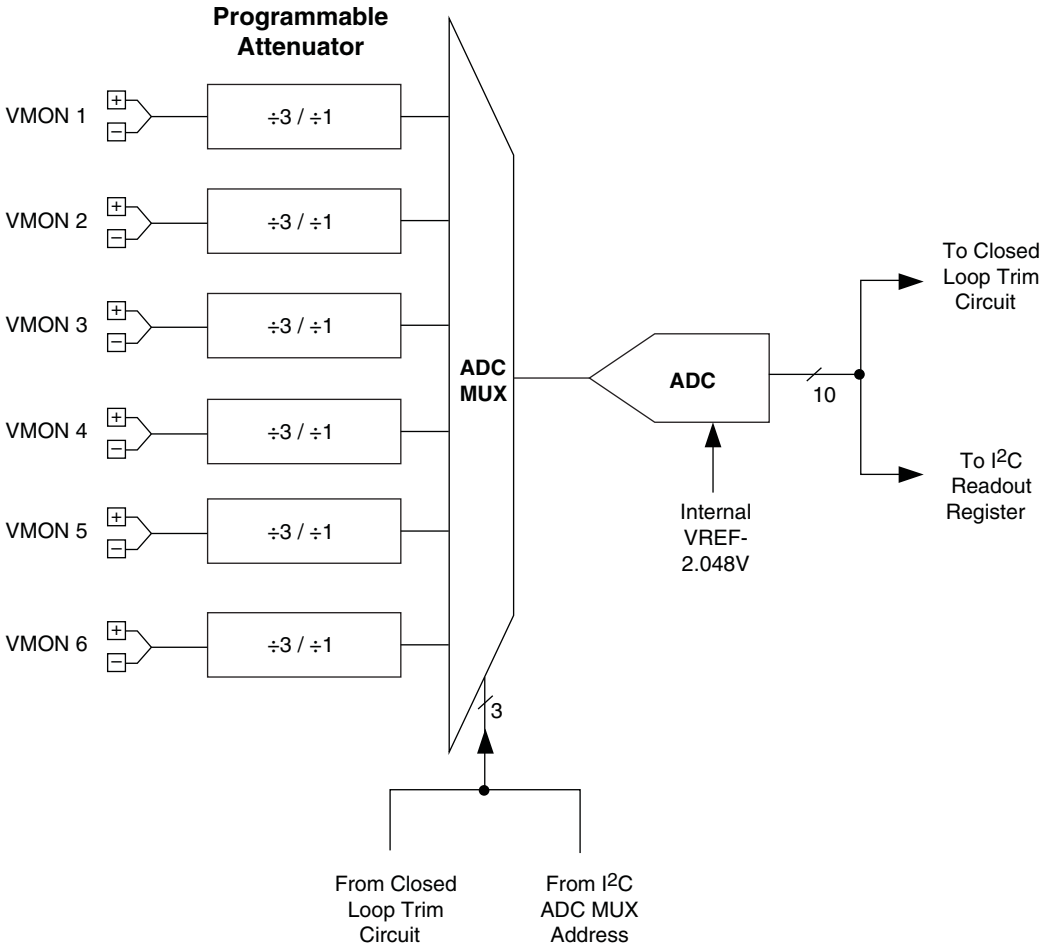


Figure 3-6 shows the ADC circuit arrangement within the ispPAC-POWR6AT6 device. The ADC can measure all analog input voltages through the multiplexer, ADC MUX. The programmable attenuator between the ADC mux and VMON pins can be configured as divided-by-3 or divided-by-1 (no attenuation). The divided-by-3 setting is used to measure voltages from 0V to 6V range and divided-by-1 setting is used to measure the voltages from 0V to 2V range.

A microcontroller can place a request for any VMON voltage measurement at any time through the I^2C bus. Upon the receipt of an I^2C command, the ADC will be connected to the I^2C selected VMON through the ADC MUX. The ADC output is then latched into the I^2C readout registers.

Calculation

The algorithm to convert the ADC code to the corresponding voltage takes into consideration the attenuation bit value. In other words, if the attenuation bit is set, then ADC output logic multiplies the 10-bit ADC code by 3 to calculate the actual voltage at that VMON input. The following formula can always be used to calculate the actual voltage from the ADC code.

Voltage at the VMONx Pins

VMONx = ADC code (12 bits[1], converted to decimal) * 2mV

[1]Note: ADC_VALUE_HIGH (8 bits), ADC_VALUE_LOW (4 bits) read from I^2C/SMBUS interface

Controlling Power Supply Output Voltage with the Margin/ Trim Block

One of the key features of the ispPAC-POWR6AT6 is its ability to make adjustments to the power supplies that it may also be monitoring. This is accomplished through the Trim and Margin Block of the device. The Trim and Margin Block can adjust voltages of up to six different power supplies through TrimCells as shown in Figure 3-7. The DC-DC blocks in the figure represent virtually any type of DC power supply that has a trim or voltage adjustment input. This can be an off-the-shelf unit or custom circuit designed around a switching regulator IC.

The interface between the ispPAC-POWR6AT6 and the DC power supply is represented by a single resistor (R1 to R6) to simplify the diagram. Each of these resistors represents a resistor network.

Other control signals driving the Margin/Trim Block are:

- VPS [1:0] – Control signals from device pins common to all six TrimCells, which are used to select the active voltage profile for all TrimCells together.
- ADC input – Used to determine the trimmed DC-DC converter voltage.
- CLTENb – Used to enable closed loop trimming of all TrimCells together.

Next to each DC-DC converter, four voltages are shown. These voltages correspond to the operating voltage profile of the Margin/Trim Block.

When the VPS[1:0] = 00, representing Voltage Profile 0: (Voltage Profile 0 is recommended to be used for the normal circuit operation)

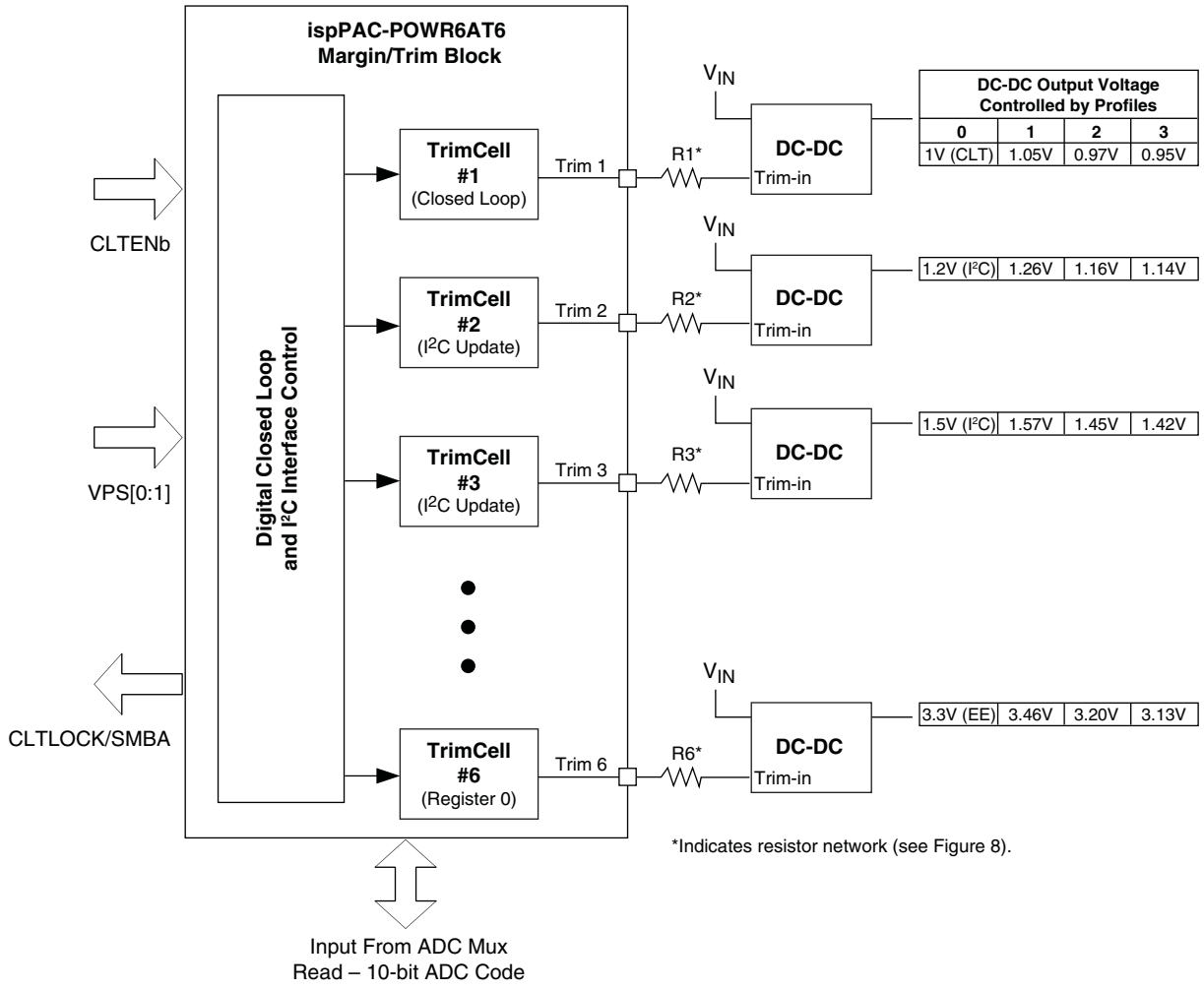
The output voltage of the DC-DC converter controlled by the Trim 1 pin of the ispPAC-POWR6AT6 will be 1V and that TrimCell is operating in closed loop trim mode. At the same time, the DC-DC converters controlled by Trim 2, Trim 3 and Trim 6 pins output 1.2V, 1.5V and 3.3V respectively.

When the VPS[1:0] = 01, representing Voltage Profile 1 being active:

The DC-DC output voltage controlled by Trim 1, 2, 3, and 6 pins will be 1.05V, 1.26V, 1.57V, and 3.46V. These supply voltages correspond to 5% above their respective normal operating voltage (also called as margin high).

Similarly, when VPS[1:0] = 11, all DC-DC converters are margined low by 5%.

Figure 3-7. ispPAC-POWR6AT6 Trim and Margin Block



There are six TrimCells in the ispPAC-POWR6AT6 device, enabling simultaneous control of up to six individual power supplies. Each TrimCell can generate up to four trimming voltages to control the output voltage of the DC-DC converter.

Figure 3-8. TrimCell Driving a Typical DC-DC Converter

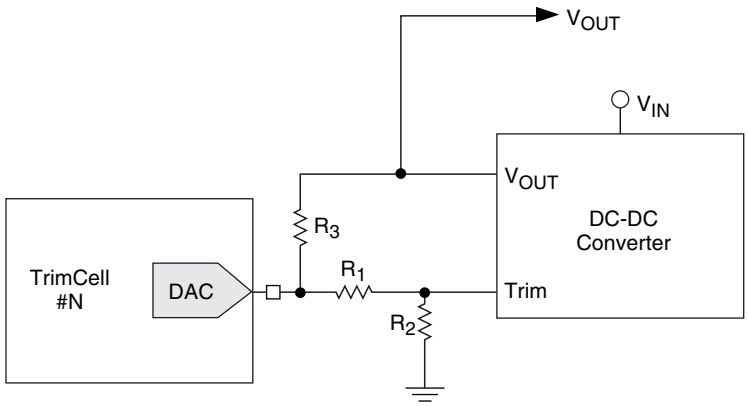


Figure 3-8 shows the resistor network between the TrimCell #N in the ispPAC-POWR6AT6 and the DC-DC converter. The values of these resistors depend on the type of DC-DC converter used and its operating voltage range. The method to calculate the values of the resistors R1, R2, and R3 are described in a separate application note.

Voltage Profile Control

The Margin / Trim Block of ispPAC-POWR6AT6 consists of six TrimCells. Because all six TrimCells in the Margin / Trim Block are controlled by a common voltage profile control signals, they all operate at the same voltage profile. The voltage profile control input comes from a pair of device pins: VPS0, VPS1.

TrimCell Architecture

The TrimCell block diagram is shown in Figure 3-9. The 8-bit DAC at the output provides the trimming voltage required to set the output voltage of a programmable supply. Each TrimCell can be operated in any one of the four voltage profiles. In each voltage profile the output trimming voltage can be set to a preset value. There are six 8-bit registers in each TrimCell that, depending on the operational mode, set the DAC value. Of these, four DAC values (DAC Register 0 to DAC Register 3) are stored in the E^2CMOS memory while the remaining register contents are stored in volatile registers. Two multiplexers (Mode Mux and Profile Mux) control the routing of the code to the DAC. The Profile Mux can be controlled by common TrimCell voltage profile control signals.

Figure 3-9. ispPAC-POWR6AT6 Output TrimCell

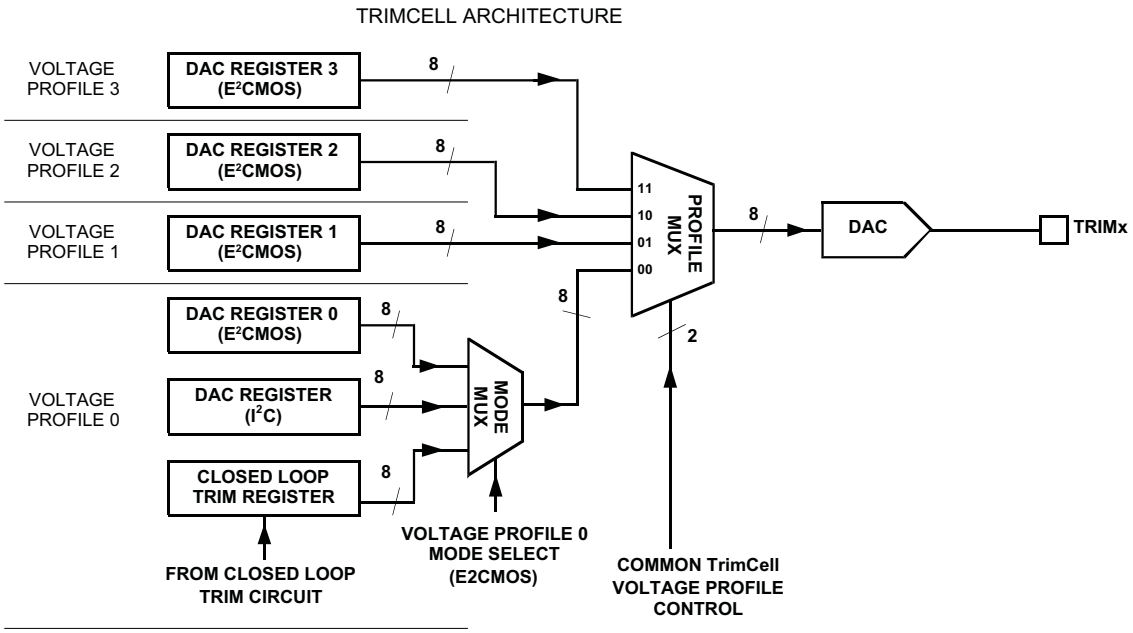


Figure 3-7 shows four power supply voltages next to each DC-DC converter. When the Profile MUX is set to Voltage Profile 3, the DC supply controlled by Trim 1 will be at 0.95V, the DC supply controlled by Trim 2 will be at 1.14V, 1.42V for Trim 3 and 3.13V for Trim 8. When Voltage Profile 0 is selected, Trim 1 will set the supply to 1V, Trim 2 and Trim 3 will be set by the values that have been loaded using I^2C at 1.2 and 1.5V, and Trim 6 will be set to 3.3V.

The following table summarizes the voltage profile selection and the corresponding DAC output trimming voltage. The voltage profile selection is common to all six TrimCells.

Table 3-1. TrimCell Voltage Profile and Operating Modes

VPS[1:0]	Selected Voltage Profile	Selected Mode	Trimming Voltage is Controlled by
11	Voltage Profile 3	—	DAC Register 3 (E^2CMOS)
10	Voltage Profile 2	—	DAC Register 2 (E^2CMOS)
01	Voltage Profile 1	—	DAC Register 1 (E^2CMOS)
00	Voltage Profile 0	DAC Register 0 Select	DAC Register 0 (E^2CMOS)
		DAC Register I^2C Select	DAC Register (I^2C)
		Digital Closed Loop Trim	Closed Loop Trim Register

TrimCell Operation in Voltage Profiles 1, 2 and 3: The output trimming voltage is determined by the code stored in the DAC Registers 1, 2, and 3 corresponding to the selected Voltage Profile.

TrimCell Operation in Voltage Profile 0: The Voltage Profile 0 has three operating modes. They are DAC Register 0 Select mode, DAC Register I^2C Select mode and Closed Loop Trim mode. The mode selection is stored in the E^2CMOS configuration memory. Each of the six TrimCells can be independently set to different operating modes during Voltage Profile 0 mode of operation.

DAC Register 0 Select Mode: The contents of DAC register 0 are stored in the on-chip E^2CMOS memory. When Voltage Profile 0 is selected, the DAC will be loaded with the value stored in DAC Register 0.

DAC Register I^2C Select Mode: This mode is used if the power management arrangement requires an external microcontroller to control the DC-DC converter output voltage. The microcontroller updates the contents of the DAC Register I^2C on the fly to set the trimming voltage to a desired value. The DAC Register I^2C is a volatile register and is reset to 80H (DAC at Bipolar zero) upon power-on. The external microcontroller writes the correct DAC code in this DAC Register I^2C before enabling the programmable power supply.

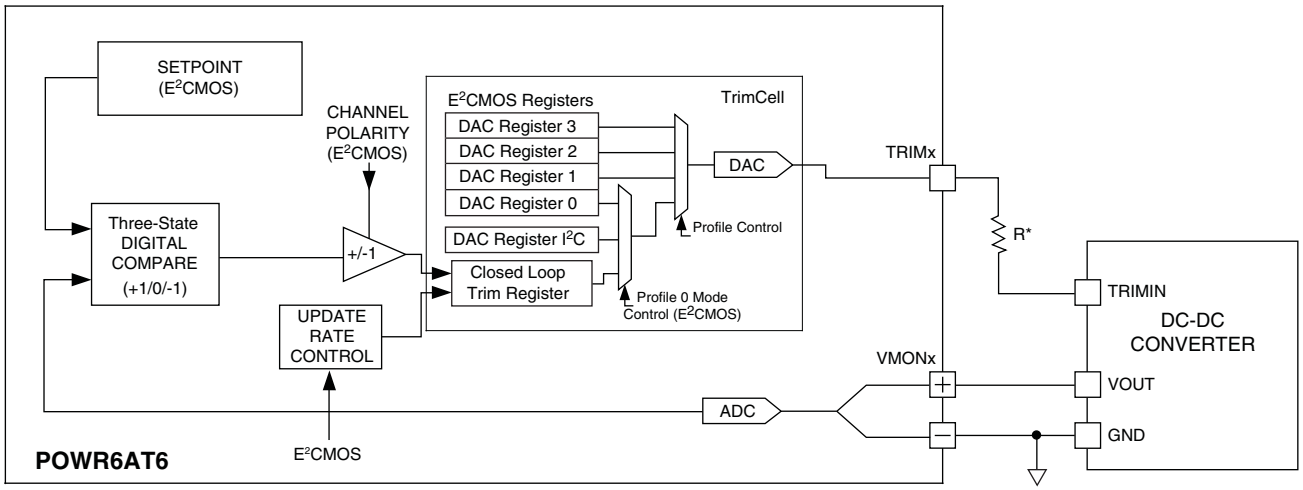
Digital Closed Loop Trim Mode

Closed loop trim mode operation can be used when tight control over the DC-DC converter output voltage at a desired value is required. The closed loop trim mechanism operates by comparing the measured output voltage of the DC-DC converter with the internally stored voltage setpoint. The difference between the setpoint and the actual DC-DC converter voltage generates an error voltage. This error voltage adjusts the DC-DC converter output voltage toward the setpoint. This operation iterates until the setpoint and the DC-DC converter voltage are equal.

Figure 3-10 shows the closed loop trim operation of a TrimCell. At regular intervals (as determined by the Update Rate Control register) the ispPAC-POWR6AT6 device initiates the closed loop power supply voltage correction cycle through the following blocks:

- Non-volatile **Setpoint** register stores the desired output voltage
- On-chip **ADC** is used to measure the voltage of the DC-DC converter
- **Three-state comparator** is used to compare the measured voltage from the ADC with the **Setpoint** register contents. The output of the three state comparator can be one of the following:
  - +1 if the setpoint voltage is greater than the DC-DC converter voltage
  - -1 if the setpoint voltage is less than the DC-DC converter voltage
  - 0 if the setpoint voltage is equal to the DC-DC converter voltage
- **Channel polarity control** determines the polarity of the error signal
- **Closed loop trim register** is used to compute and store the DAC code corresponding to the error voltage. The contents of the Closed Loop Trim will be incremented or decremented depending on the channel polarity and the three-state comparator output. If the three-state comparator output is 0, the closed loop trim register contents are left unchanged.
- The **DAC** in the **TrimCell** is used to generate the analog error voltage that adjusts the attached DC-DC converter output voltage.

Figure 3-10. Digital Closed Loop Trim Operation



*Indicates resistor network (see Figure 8).

The closed loop trim cycle interval is programmable and is set by the update rate control register. The following table lists the programmable update interval that can be selected by the update rate register.

Table 3-2. Output DAC Update Rate in Digital Closed Loop Mode

Update Rate Control Value	Update Interval
00	432 µs
01	1.06 ms
10	8.74 ms
11	16.9 ms

Closed Loop Trim Control Using the CLTENb Pin

There is a one-to-one relationship between the selected TrimCell and the corresponding VMON input for the closed loop operation. For example, if TrimCell 3 is used to control the power supply in the closed loop trim mode, VMON3 must be used to monitor its output power supply voltage.

The CLTENb enable pin (active low) simultaneously starts the closed loop trimming process for all ispPAC-POWR6AT6 trim outputs so configured. Behavior of individual trim output pins is defined using Lattice PAC-Designer design software and stored in the ispPAC-POWR6AT6's non-volatile E^{2}CMOS memory. In addition to a closed-loop trim control option, two other configuration alternatives are available. The first stores a fixed, or static, value for a given trim output in E^{2}CMOS memory. The second enables dynamic trim adjustments to be made using an external microcontroller via the ispPAC-POWR6AT6's I^{2}C interface bus. Neither of these options is affected by the CLTENb pin, however.

When the ispPAC-POWR6AT6's CLTENb pin goes low, closed-loop trimming is enabled. When CLTENb subsequently goes high, there is a brief delay after which closed-loop trimming is suspended. The delay is the time required for ispPAC-POWR6AT6 control logic to complete a trim update cycle. Table 3-2 shows typical times for update cycles based on which of four trim rates is initially chosen in PAC-Designer. When the trim process is halted, it should also be noted the trim output DACs have constant voltage output levels (corresponding to their last input code setting). This condition can be safely maintained indefinitely, but resuming closed-loop trimming (by taking CLTENb low) better insures power supplies remain precisely adjusted under all possible conditions. When re-enabled, closed-loop trimming restarts where it left off. In this sense, the CLTENb pin can be thought of as a “pause” control for closed-loop trim.

It should also be noted that whenever the VPS0 and VPS1 pins are not both low, they effectively stop closed-loop trim the same way the CLTENb pin does when it goes high. That is, whenever an alternate trim mode (other than VPS0=0 and VPS1=0) is selected, the trim process is suspended as described above. Assuming the CLTENb pin is asserted, when both VPS0 and VPS1 are low again, closed-loop trimming will resume where it left off.

It is recommended that the CLTENb pin not be activated until after any necessary power supply sequencing is completed to prevent an “open loop” condition from occurring. Otherwise, if control of when closed-loop trimming begins is not critical, the CLTENb pin can be tied to ground. This will cause closed-loop trim to begin immediately after the initial power on of the ispPAC-POWR6AT6 is completed.

Closed Loop Trim Start-up Behavior

The contents of the closed loop register, upon power-up, will contain a value 80h (Bipolar-zero) value. The DAC output voltage will be equal to the programmed Offset voltage. Usually under this condition, the power supply output will be close to its nominal voltage. If the power supply trimming should start after reaching its desired output voltage, the corresponding DAC code can be loaded into the closed loop trim register through I^2C (same address as the DAC register I^2C mode) before activating the CLTENb pin.

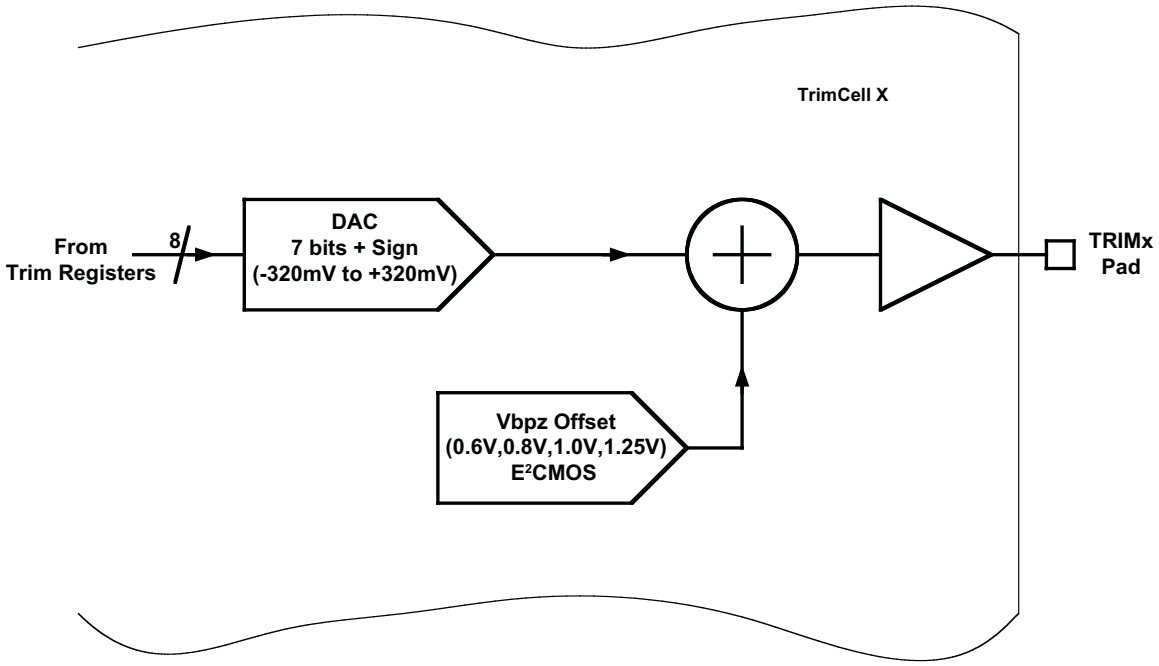
Details of the Digital to Analog Converter (DAC)

Each TrimCell has an 8-bit bipolar DAC to set the trimming voltage (Figure 3-11). The full-scale output voltage of the DAC is +/- 320 mV. A code of 80H results in the DAC output set at its bi-polar zero value.

The voltage output from the DAC is added to a programmable offset value and the resultant voltage is then applied to the trim output pin. The offset voltage is typically selected to be approximately equal to the DC-DC converter open circuit trim node voltage. This results in maximizing the DC-DC converter output voltage range.

The programmed offset value can be set to 0.6V, 0.8V, 1.0V or 1.25V. This value selection is stored in E^2CMOS memory and cannot be changed dynamically.

Figure 3-11. Vbpz Offset Voltage is Added to DAC Output Voltage to Derive Trim Pad Voltage



RESET Command via JTAG or I^2C

Issuing a reset instruction via JTAG or I^2C will force all trim outputs selected for digital closed-loop trim control back to their initial output level (code 80h + Vbpz). After that, assuming the CLTENb is still asserted, digital closed loop

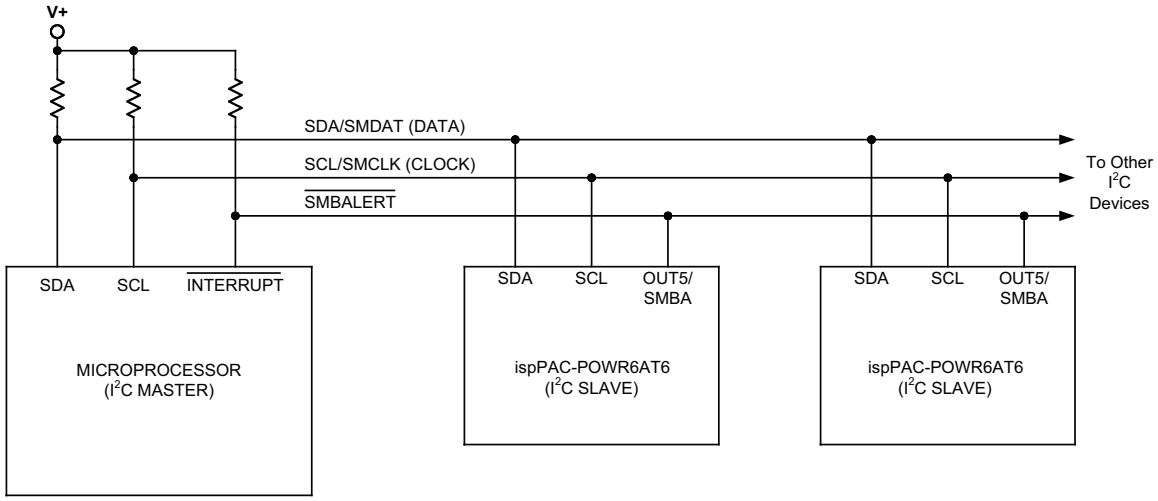
trim will begin and CLTLOCK/SMBA will only reassert when the trim process is complete. Contents of the I²C cltlock_status register (0x00), however are not fully reset to initial conditions until the CLTLOCK/SMBA pin achieves a reasserted state.

CAUTION: Issuing a RESET command through I²C or JTAG during the ispPAC-POWR6AT6 device operation, results in the device aborting all operations and returning to the power-on reset state except for the one condition mentioned above.

I²C/SMBUS Interface

I²C and SMBus are low-speed serial interface protocols designed to enable communications among a number of devices on a circuit board. The ispPAC-POWR6AT6 supports a 7-bit addressing of the I²C communications protocol, as well as SMBTimeout and SMBAlert features of the SMBus, enabling it to easily integrated into many types of modern power management systems. Figure 3-12 shows a typical I²C configuration, in which one or more ispPAC-POWR6AT6s are slaved to a supervisory microcontroller. SDA is used to carry data signals, while SCL provides a synchronous clock signal. The SMBAlert line is only present in SMBus systems. The 7-bit I²C address of the POWR6AT6 is fully programmable through the JTAG port.

Figure 3-12. ispPAC-POWR6AT6 in I²C/SMBUS System



In both the I²C and SMBus protocols, the bus is controlled by a single MASTER device at any given time. This master device generates the SCL clock signal and coordinates all data transfers to and from a number of slave devices. The ispPAC-POWR6AT6 is configured as a slave device, and cannot independently coordinate data transfers. Each slave device on a given I²C bus is assigned a unique address. The ispPAC-POWR6AT6 implements the 7-bit addressing portion of the standard. Any 7-bit address can be assigned to the ispPAC-POWR6AT6 device by programming through JTAG. When selecting a device address, one should note that several addresses are reserved by the I²C and/or SMBus standards, and should not be assigned to ispPAC-POWR6AT6 devices to assure bus compatibility. Table 3-3 lists these reserved addresses.

Table 3-3. I²C/SMBus Reserved Slave Device Addresses

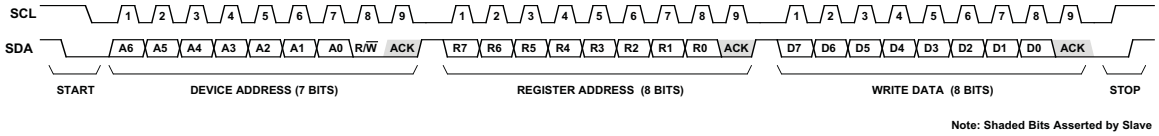
Address	R/W bit	I²C function Description	SMBus Function
0000 000	0	General Call Address	General Call Address
0000 000	1	Start Byte	Start Byte
0000 001	x	CBUS Address	CBUS Address
0000 010	x	Reserved	Reserved
0000 011	x	Reserved	Reserved
0000 1xx	x	HS-mode master code	HS-mode master code
0001 000	x	NA	SMBus Host
0001 100	x	NA	SMBus Alert Response Address
0101 000	x	NA	Reserved for ACCESS.bus
0110 111	x	NA	Reserved for ACCESS.bus
1100 001	x	NA	SMBus Device Default Address
1111 0xx	x	10-bit addressing	10-bit addressing
1111 1xx	x	Reserved	Reserved

The ispPAC-POWR6AT6's I²C/SMBus interface allows data to be both written to and read from the device. A data write transaction (Figure 3-13) consists of the following operations:

1. Start the bus transaction
2. Transmit the device address (7 bits) along with a low write bit
3. Transmit the address of the register to be written to (8 bits)
4. Transmit the data to be written (8 bits)
5. Stop the bus transaction

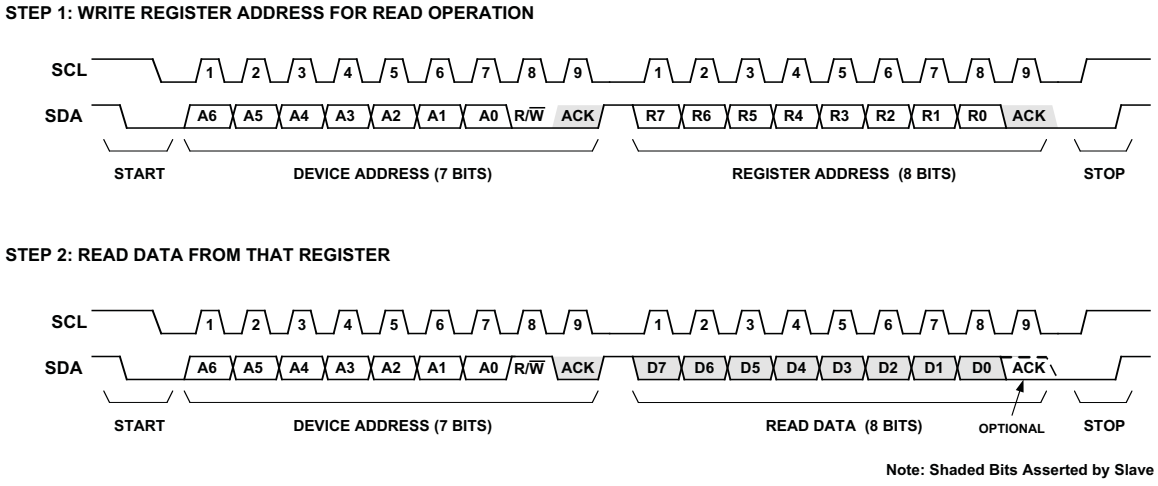
To start the transaction, the master device holds the SCL line high while pulling SDA low. Address and data bits are then transferred on each successive SCL pulse, in three consecutive byte frames of 9 SCL pulses. Address and data are transferred on the first 8 SCL clocks in each frame, while an acknowledge signal is asserted by the slave device on the 9th clock in each frame. Both data and addresses are transferred in a most-significant-bit-first format. The first frame contains the 7-bit device address, with bit 8 held low to indicate a write operation. The second frame contains the register address to which data will be written, and the final frame contains the actual data to be written. Note that the SDA signal is only allowed to change when the SCL is low, as raising SDA when SCL is high signals the end of the transaction.

Figure 3-13. I²C Write Operation



Reading a data byte from the ispPAC-POWR6AT6 requires two separate bus transactions (Figure 3-14). The first transaction writes the register address from which a data byte is to be read. Note that since no data is being written to the device, the transaction is concluded after the second byte frame. The second transaction performs the actual read. The first frame contains the 7-bit device address with the R/W bit held High. In the second frame the ispPAC-POWR6AT6 asserts data out on the bus in response to the SCL signal. Note that the acknowledge signal in the second frame is asserted by the master device and not the ispPAC-POWR6AT6.

Figure 3-14. I²C Read Operation



The ispPAC-POWR6AT6 provides 15 registers that can be accessed through its I²C interface. These registers provide the user with the ability to monitor and control the device's inputs and outputs, and transfer data to and from the device. Table 3-4 provides a summary of these registers.

Table 3-4. I²C Control Registers

Register Address	Register Name	Read/Write	Description	Value on POR, RESET
0x00	cltlock_status	R/W	Closed-loop trim status *bit-6 is RW, all others R only	1100 0000
0x01	adc_value_low	R	ADC D[3:0] and status	0000 1110
0x02	adc_value_high	R	ADC D[11:4]	0000 0000
0x03	adc_mux	R/W	ADC Attenuator and MUX[3:0]	1110 1000
0x04	UES_byte0	R	UES[7:0]	EEEE EEEE
0x05	UES_byte1	R	UES[15:8]	EEEE EEEE
0x06	UES_byte2	R	UES[23:16]	EEEE EEEE
0x07	UES_byte3	R	UES[31:24]	EEEE EEEE
0x08	reset	W	Resets device on write	1111 1111
0x09	trim1_trim	R/W	Trim DAC 1 [7:0]	1000 0000
0x0A	trim2_trim	R/W	Trim DAC 2 [7:0]	1000 0000
0x0B	trim3_trim	R/W	Trim DAC 3 [7:0]	1000 0000
0x0C	trim4_trim	R/W	Trim DAC 4 [7:0]	1000 0000
0x0D	trim5_trim	R/W	Trim DAC 5 [7:0]	1000 0000
0x0E	trim6_trim	R/W	Trim DAC 6 [7:0]	1000 0000

Note: x = unknown, 0 = low, 1 = high, E= E² memory setting (UES string)

I²C Closed-Loop Trim Register

Figure 3-15 shows bit assignments for the ispPAC-POWR6AT6 I²C closed-loop trim status register. There are six read only bits (cltlock_status.in[1:6]) that reflect the present trim status of individual trim output pins. When a closed loop-trim controlled power supply's output reaches the value specified by its Profile 0 configuration setting, that trim output's CLTLOCK_status bit is set to a "1".

The I²C closed-loop trim register has one read/write bit (cltlock_status). When ispPAC-POWR6AT6 is configured in PAC-Designer to operate in SMBus Alert mode, it is set to a "1" by device control logic to send an SMBus Alert. Logic then waits for it to be acknowledged by a host I²C processor (when it is addresses the register), completing

the SMBus Alert cycle. Refer to the CLTLOCK/SMBA pin and SMBus Alert sections of this datasheet for more information on how the closed-loop trim status in this I²C register is used.

Figure 3-15. I²C Closed Loop Trim Status Register

0x00 – CLTLOCK_STATUS (b6 = Read/Write; all others Read Only)

X	SMBA	in6	in5	in4	in3	in2	in1
b7	b6	b5	b4	b3	b2	b1	b0

It is possible to read the value of the voltage present on any of the VMON inputs by using the ispPAC-POWR6AT6's ADC. Three registers provide the I²C interface to the ADC (Figure 3-16).

Figure 3-16. ADC Interface Registers

0x01 - ADC_VALUE_LOW (Read Only)

D3	D2	D1	D0	1	1	1	DONE
b7	b6	b5	b4	b3	b2	b1	b0

0x02 - ADC_VALUE_HIGH (Read Only)

D11	D10	D9	D8	D7	D6	D5	D4
b7	b6	b5	b4	b3	b2	b1	b0

0x03 - ADC_MUX (Read/Write)

X	X	X	ATTEN	X	SEL2	SEL1	SEL0
b7	b6	b5	b4	b3	b2	b1	b0

To perform an A/D conversion, one must set the input attenuator and channel selector. Two input ranges may be set using the attenuator, 0 - 2.048V and 0 - 6.144V. Table 3-5 shows the input attenuator settings.

Table 3-5. ADC Input Attenuator Control

ATTEN (ADC_MUX.4)	Resolution	Full-Scale Range
0	2mV	2.048 V
1	6mV	6.144 V

The input selector may be set to monitor any one of the six VMON inputs or the VCCA input. Table 3-6 shows the codes associated with each input selection.

Table 3-6. V_{MON} Address Selection Table

Select Word			
SEL2 (ADC_MUX.2)	SEL1 (ADC_MUX.1)	SEL0 (ADC_MUX.0)	Input Channel
0	0	0	VMON1
0	0	1	VMON2
0	1	0	VMON3
0	1	1	VMON4
1	0	0	VMON5
1	0	1	VMON6

Writing a value to the ADC_MUX register to set the input attenuator and selector will automatically initiate a conversion. When the conversion is in process, the DONE bit (ADC_VALUE_LOW.0) will be reset to 0. When the conversion is complete, this bit will be set to 1. When the conversion is complete, the result may be read out of the ADC by performing two I^2C read operations; one for ADC_VALUE_LOW, and one for ADC_VALUE_HIGH. It is recommended that the I^2C master load a second conversion command only after the completion of the current conversion command (Waiting for the DONE bit to be set to 1). An alternative would be to wait for a minimum specified time (see Tconvert value in the specifications) and disregard checking the DONE bit.

Note that if the I^2C clock rate falls below 50kHz (see F_{I2C} note in specifications), the only way to insure a valid ADC conversion is to wait the minimum specified time (Tconvert), as the operation of the DONE bit at clock rates lower than that cannot be guaranteed. In other words, if the I^2C clock rate is less than 50kHz, the DONE bit may or may not assert even when a valid conversion result is available. Erroneous ADC readout results are also possible whenever the I^2C clock is less than 50kHz and a second ADC convert is commanded before a full $T_{CONVERT}$ time period has elapsed. Under these conditions, it is still possible to obtain valid results for the second conversion by reading out the ADC low and high byte results twice in succession (read ADC_VALUE_LOW, read ADC_VALUE_HIGH, then repeating the low and high byte reads). Only the second ADC readout value is reliably valid, however.

To insure every ADC conversion result is valid, preferred operation is to clock I^2C at more than 50kHz and verify DONE bit status or wait for the full $T_{CONVERT}$ time period between subsequent ADC convert commands. If an I^2C request is placed before the current conversion is complete, the DONE bit will be set to 1 only after the second request is complete.

The UES word may also be read through the I^2C interface, with the register mapping shown in Figure 3-17.

Figure 3-17. I^2C Register Mapping for UES Bits

0x04 - UES_BYTE0 (Read Only)

UES7	UES6	UES5	UES4	UES3	UES2	UES1	UES0
b7	b6	b5	b4	b3	b2	b1	b0

0x05 - UES_BYTE1 (Read Only)

UES15	UES14	UES13	UES12	UES11	UES10	UES9	UES8
b7	b6	b5	b4	b3	b2	b1	b0

0x06 - UES_BYTE2 (Read Only)

UES23	UES22	UES21	UES20	UES19	UES18	UES17	UES16
b7	b6	b5	b4	b3	b2	b1	b0

0x07 - UES_BYTE3 (Read Only)

UES31	UES30	UES29	UES28	UES27	UES26	UES25	UES24
b7	b6	b5	b4	b3	b2	b1	b0

The I^2C interface also provides the ability to initiate reset operations. The ispPAC-POWR6AT6 may be reset by issuing a write of any value to the I^2C RESET register (Figure 3-18). Refer to the RESET Command via JTAG or I^2C section of this data sheet for further information.

Figure 3-18. I²C Reset Register

0x8 - RESET (Write Only)

X	X	X	X	X	X	X	X
b7	b6	b5	b4	b3	b2	b1	b0

The ispPAC-POWR6AT6 also provides the user with the ability to program the trim values over the I²C interface, by writing the appropriate binary word to the associated trim register (Figure 3-19).

Figure 3-19. I²C Trim Registers

0x9 - TRIM1_TRIM (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
b7	b6	b5	b4	b3	b2	b1	b0

0xA - TRIM2_TRIM (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
b7	b6	b5	b4	b3	b2	b1	b0

0xB - TRIM3_TRIM (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
b7	b6	b5	b4	b3	b2	b1	b0

0xC - TRIM4_TRIM (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
b7	b6	b5	b4	b3	b2	b1	b0

0xD - TRIM5_TRIM (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
b7	b6	b5	b4	b3	b2	b1	b0

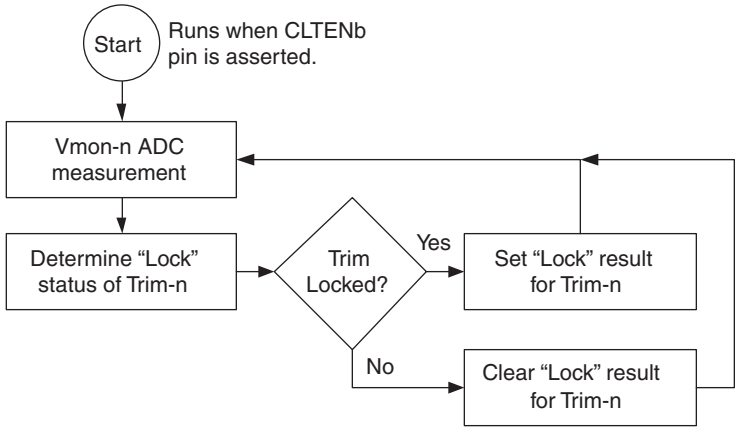
0xE - TRIM6_TRIM (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
b7	b6	b5	b4	b3	b2	b1	b0

Monitoring Closed Loop Trim with the CLTLOCK/SMBA Pin

The ispPAC-POWR6AT6 uses a simple algorithm to determine if closed-loop trimming has reached a stable or locked value. In Figure 3-20, the flow diagram shows whenever the closed-loop trim enable pin (CLTENb) is asserted (low) the status of all six trim output pins is tested and updated at periodic intervals (refer to Table 3-2 for typical cycle times). If a trim lock condition exists for a given pin, a lock result is set and processing continues. Pins not selected for closed-loop trim are automatically reported to be in the lock condition, but timing is kept constant to preserve a constant update rate regardless of how many trim outputs are really involved.

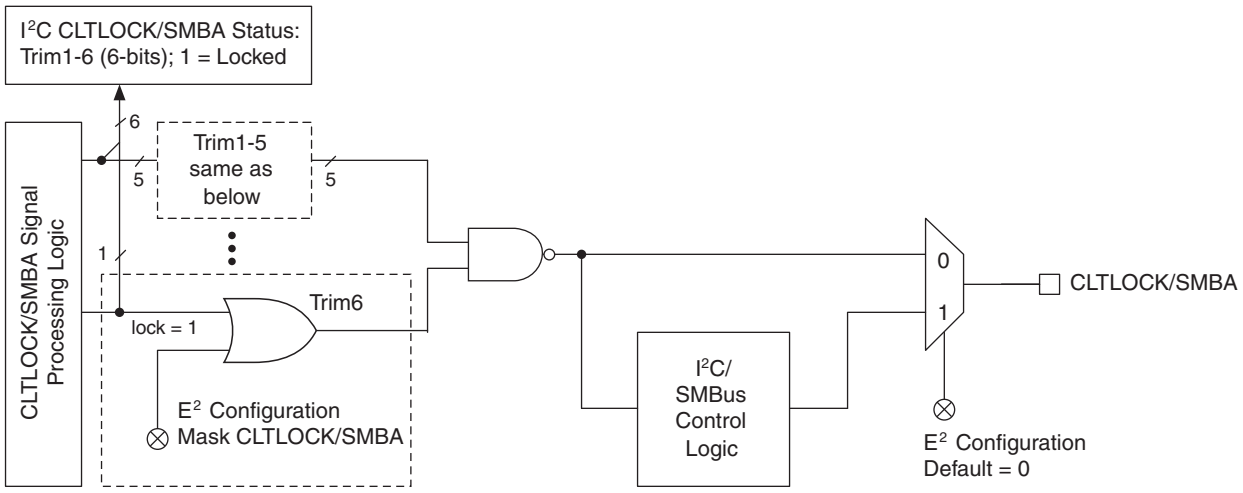
Figure 3-20. Closed-Loop Trim Lock (CLTLOCK/SMBA) Signal Processing Logic Flow Diagram



The ispPAC-POWR6AT6 contains trim detection processing circuitry to signal when closed-loop trimming is complete for selected trim output pins. This signal is output on the closed-loop control output pin (CLTLOCK/SMBA) which has a open drain output and is normally asserted low (pull down). When all closed-loop trim output pins reach a completion or trim "locked" condition, the CLTLOCK/SMBA output pin pulls low. Afterwards, the CLTLOCK/SMBA pin also indicates when a trimming fault exists by de-asserting (going high). Finally, the CLTLOCK/SMBA pin can be configured to work in conjunction with the SMBus Alert protocol to signal when trim lock has been achieved or lost (see the section on SMBus Alert for details).

Figure 3-21 shows a simplified diagram of how the state of the CLTLOCK/SMBA output pin is generated. After closed loop trimming is enabled, the CLTLOCK/SMBA signal processing logic examines the output result from the ADC going to each TrimCell at the end of each trim update cycle. If it is determined that a trim lock condition exists for that trim output pin, the trim lock signal is asserted. The status of an individual trim output can be read via the I^2C closed loop trim register (refer to Figure 3-15). Trim output pins not selected for closed-loop trim operation will automatically indicate a trim locked condition.

Figure 3-21. Closed-Loop Trim Lock Output Pin (CLTLOCK/SMBA) Functionality



Next, an individual lock signal is OR'd with an E^2CMOS mask bit specific to that trim output pin. There are six masking bits, one for each possible trim output pin. When set, masking bits effectively override the lock determination for a particular trim output pin. The default setting for all mask bits is cleared (not set). Changes to the device configuration mask bits can be made using PAC-Designer.

Finally, the individual lock status inputs all meet at a common NAND gate. A trim lock condition is generated when all six trim status inputs are high causing the CLTLOCK/SMBA pin to go low. If the trim lock is lost for any monitored trim output pin, the CLTLOCK/SMBA pin will de-assert (go open). This could be due to a failed power supply for example, or if the ispPAC-POWR6AT6 can no longer adjust a controlled supply to specification. Interrogation of the I^2C register determines which trim output pin lost lock. Also, the ADC can be used to measure individual supplies to further diagnose an underlying fault.

There is an alternative path the CLTLOCK/SMBA signal can take, depending on how the ispPAC-POWR6AT6 has been configured. Refer to the I^2C/SMBus control logic box shown in Figure 3-21. When the alternative output path is enabled in PAC-Designer, the trim lock result is first sent to the I^2C/SMBus control logic for processing before going to the CLTLOCK/SMBA output pin. The purpose of this control logic is to make the CLTLOCK/SMBA signal work in accordance with the SMBus Alert protocol. The main difference between the two output path alternatives is that SMBus Alert stays set (low) until acknowledged by the host I^2C processor. Also, an SMBus Alert is set (pulled low) when a trim lock condition is achieved, as well as when it is lost. Either condition must be acknowledged or the SMBus Alert condition will not go away. Note that on initial device power-on, or after an I^2C software reset, an SMBus Alert is blocked (no trim lock). The SMBus master must explicitly set the CLT_LOCK_STATUS bit-6 low to begin the SMBAlert process.

SMBus SMBAlert Function

The ispPAC-POWR6AT6 provides an SMBus SMBAlert function to request service from the bus master when used as part of an SMBus system. When the SMBAlert signal mode for closed-loop trimming is chosen in PAC-Designer, the CLTLOCK/SMBA output pin will go low whenever the trim lock condition status changes. The reason for this is to report both when all outputs are in trim lock and when one or more trim output pins lose trim lock.

When a selected (unmasked) closed-loop trim output loses its locked status, servicing the resulting SMBus Alert and interrogating the I^2C closed-loop trim register will reveal which trim output pin(s) that are involved. After acknowledgement by the host I^2C processor, the CLTLOCK/SMBA pin will be de-asserted until another change in CLTLOCK/SMBA trim status occurs.

After initial device turn-on and power-on reset (POR) is complete, the SMBA bit in the I^2C register (0x00, bit-6) is set high or “1”. The SMBAlert function of the ispPAC-POWR6AT6 is effectively suspended until this location has been overwritten with a low or “0”. The purpose of this is to prevent output to the CLTLOCK/SMBA pin before the bus master or host processor is ready to process SMBAlerts.

Note that if closed loop trimming is enabled and completes before this action is performed, the initial trim lock indication (as an SMBAlert) will not occur. If this happens, trim status can still be interrogated, however. Reading the I^2C trim status register to see that all trim bits are high (bit-1 to bit-6) is a valid indication that trim lock has been achieved. Otherwise, the CLTENb pin must be held high until after the I^2C SMBA bit is written low and then enabled afterwards to insure detection of the initial trim lock status with an SMBAlert.

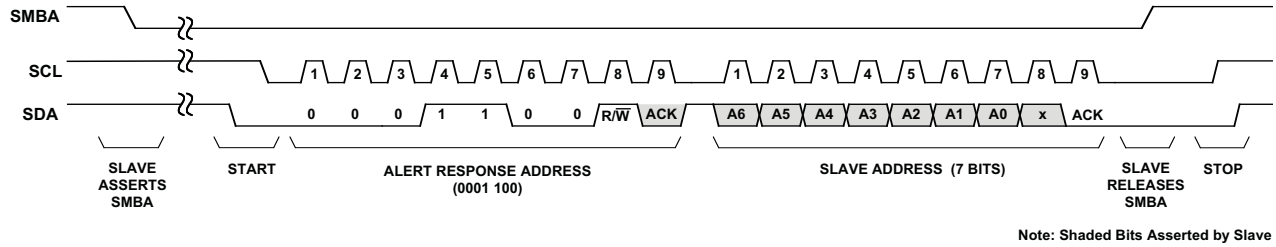
After the SMBA bit has been set low, any subsequent change in trim lock status will be reported with an SMBAlert output to the CLTLOCK/SMBA pin. To process an SMBAlert, the following steps must be performed to service the alert and resume monitoring for the next change in trim lock status:

The typical flow for an SMBAlert transaction is as follows (Figure 3-22):

1. I^2C closed loop trim register SMBA bit is forced to high by internal ispPAC-POWR6AT6 control logic whenever the trim lock status changes
2. ispPAC-POWR6AT6 closed-loop trim control logic pulls the CLTLOCK/SMBA pin low
3. Master responds to interrupt from SMBA line
4. Master broadcasts a read operation by sending the SMBus Alert Response Address (ARA, 18h)
5. ispPAC-POWR6AT6 responds to the ARA request by transmitting its device address

6. If transmitted device address matches ispPAC-POWR6AT6 address, the master completes the cycle by setting the I^2C closed loop trim register SMBA bit low again. This releases the CLTLOCK/SMBA pin (it goes high).

Figure 3-22. SMBAlert Bus Transaction



After CLTLOCK/SMBA has been released, the bus master (typically a microcontroller) may opt to perform some service functions in which it may send data to or read data from the ispPAC-POWR6AT6. As part of the service functions, the bus master will typically need to clear whatever condition initiated the SMBAlert request (power supply malfunction, etc.). For further information on the SMBus functionality, the user should consult the SMBus Standard.

Software-Based Design Environment

Designers can configure the ispPAC-POWR6AT6 using PAC-Designer, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispPAC-POWR6AT6. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available on the Lattice web site for downloading. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. The PAC-Designer schematic window, shown in Figure 3-23, provides access to all configurable ispPAC-POWR6AT6 elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground, and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved, simulated, and downloaded to devices.

Figure 3-23. PAC-Designer ispPAC-POWR6AT6 Design Entry Screen