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ITG-3400
Product Specification
Revision 1.0

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1 Document Information

1.1 Revision History

Revision Date	Revision	Description
12/24/2013	1.0	Initial Release

1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information on the ITG-3400™ gyroscope device. The device is housed in a small 3x3x0.9mm 24-pin QFN package.

Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon. For references to register map and descriptions of individual registers, please refer to the ITG-3400 Register Map and Register Descriptions document.

1.3 Product Overview

The ITG-3400 is a 3-axis gyroscope that is housed in a small 3x3x0.9mm (24-pin QFN) package. It also features a 4096-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. With its dedicated I^2C sensor bus, the ITG-3400 directly accepts inputs from external I^2C devices.

The gyroscope has a programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec. Factory-calibrated initial sensitivity of the sensor reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, a precision clock with 1% drift from -40°C to 85°C, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

Communication with all registers of the device is performed using either I^2C at 400kHz or SPI at 1MHz. For applications requiring faster communications, the sensor and interrupt registers may be read using SPI at 20MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x0.9mm (24-pin QFN), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.4 Applications

- Motion UI
- Handset gaming
- Location based services, points of interest, and dead reckoning
- Health and sports monitoring
- Power management

2 Features

2.1 Gyroscope Features

The triple-axis MEMS gyroscope in the ITG-3400 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250, ±500, ±1000, and ±2000°/sec and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Gyroscope operating current: 3.2mA
- Factory calibrated sensitivity scale factor

2.2 Additional Features

The ITG-3400 includes the following additional features:

- VDD supply voltage range of 1.8 – 3.3V ± 5%
- Smallest and thinnest QFN package for portable devices: 3x3x0.9mm (24-pin QFN)
- 4096 byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope and temp sensor
- 10,000 *g* shock tolerant
- 400kHz Fast Mode I^2C for communicating with all registers
- 1MHz SPI serial interface for communicating with all registers
- 20MHz SPI serial interface for reading sensor and interrupt registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Gyroscope Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL=0		±250		º/s	
	FS_SEL=1		±500		º/s	
	FS_SEL=2		±1000		º/s	
	FS_SEL=3		±2000		º/s	
Gyroscope ADC Word Length			16		bits	
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(º/s)	
	FS_SEL=1		65.5		LSB/(º/s)	
	FS_SEL=2		32.8		LSB/(º/s)	
	FS_SEL=3		16.4		LSB/(º/s)	
Sensitivity Scale Factor Tolerance	25°C		±4		%	1
Sensitivity Scale Factor Variation Over Temperature	0°C to +55°C		±10		%	1
Nonlinearity	Best fit straight line; 25°C		0.2		%	1
Cross-Axis Sensitivity			±2		%	
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±60		º/s	1
ZRO Variation Over Temperature	0°C to +55°C		±60		º/s	
GYROSCOPE NOISE PERFORMANCE (FS_SEL=0)						
Total RMS Noise	DLPFCFG=2 (92 Hz)		0.7		º/s-rms	1
GYROSCOPE MECHANICAL FREQUENCIES		25	27	29	KHz	1
LOW PASS FILTER RESPONSE	Programmable Range	5		250	Hz	
GYROSCOPE START-UP TIME	From Sleep mode		35		ms	1
OUTPUT DATA RATE	Programmable, Normal (Filtered) mode	4		8000	Hz	1

Table 1 Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.2 Electrical Specifications

3.2.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	
VDDIO		1.71	1.8	3.45	V	
SUPPLY CURRENTS						
Normal Mode	3-axis Gyroscope		3.2		mA	1
Standby Mode			1.6		mA	1
Full-Chip Sleep Mode			6		µA	1
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	

Table 2 D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.2.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.1		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Sensitivity	Untrimmed		333.87		LSB/°C	
Room Temp Offset	21°C		0		LSB	
Power-On RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01	20	100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
I^2C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (SYNC, AD0, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		250	ns	
INTERNAL CLOCK SOURCE						
Sample Rate	Fchoice=0,1,2 SMPLRT_DIV=0		32		kHz	
	Fchoice=3; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
	Fchoice=3; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	
Clock Frequency Initial Tolerance	CLK_SEL=0, 6; 25°C	-5		+5	%	1
	CLK_SEL=1,2,3,4,5; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6	-10		+10	%	1
	CLK_SEL=1,2,3,4,5		±1		%	1
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	
	High Speed Characterization		1 ±10%		MHz	
SPI Operating Frequency, Sensor and Interrupt Registers Read Only			20 ±10%		MHz	
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	
	All registers, Standard-mode			100	kHz	

Table 3 A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.3 I2C Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I^2C TIMING	**I^2C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	
t_{LOW}, SCL Low Period		1.3			µs	
t_{HIGH}, SCL High Period		0.6			µs	
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	
C_b, Capacitive Load for each Bus Line			< 400		pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	

Table 4 I^2C Timing Characteristics

Notes:

1. Timing Characteristics apply to both Primary and Auxiliary I2C Bus
2. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

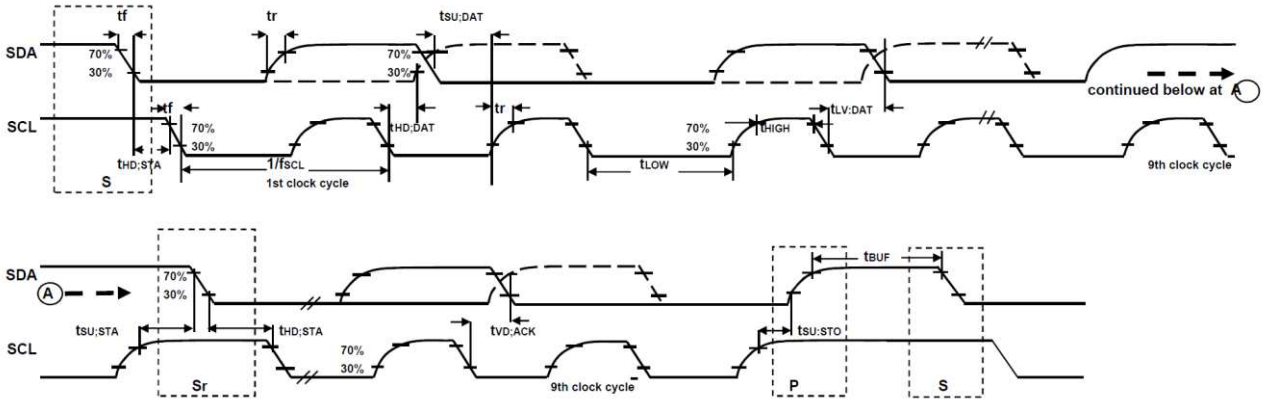


Figure 1 I2C Bus Timing Diagram

3.4 SPI Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				1	MHz	
t_{LOW}, SCLK Low Period		400			ns	
t_{HIGH}, SCLK High Period		400			ns	
$t_{SU.CS}$, CS Setup Time		8			ns	
$t_{HD.CS}$, CS Hold Time		500			ns	
$t_{SU.SDI}$, SDI Setup Time		11			ns	
$t_{HD.SDI}$, SDI Hold Time		7			ns	
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			100	ns	
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20pF	4			ns	
$t_{DIS.SDO}$, SDO Output Disable Time				50	ns	

Table 5 SPI Timing Characteristics

Notes:

3. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

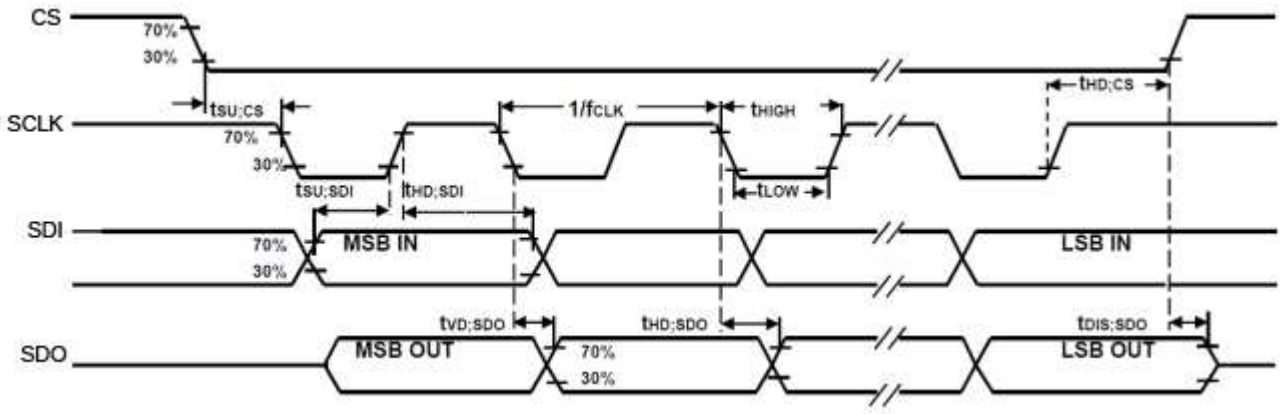


Figure 2 SPI Bus Timing Diagram

3.4.1 fSCLK = 20MHz

Parameters	Conditions	Min	Typical	Max	Units
SPI TIMING					
f_{SCLK}, SCLK Clock Frequency		0.9		20	MHz
t_{LOW}, SCLK Low Period		-		-	ns
t_{HIGH}, SCLK High Period		-		-	ns
$t_{SU.CS}$, CS Setup Time		1			ns
$t_{HD.CS}$, CS Hold Time		1			ns

$t_{SU.SDI}$, SDI Setup Time		0			ns
$t_{HD.SDI}$, SDI Hold Time		1			ns
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF		25		ns
$t_{DIS.SDO}$, SDO Output Disable Time				25	ns

Table 6 fCLK = 20MHz

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

3.5 Absolute Maximum Ratings

Stress above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
PLLFILT	-0.5V to 2V
Input Voltage Level (AD0, SYNC, INT, SCL, SDA)	-0.5V to VDD + 0.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2),125°C ±100mA

Table 7 Absolute Maximum Ratings

4 Applications Information

4.1 Pin Out Diagram and Signal Description

Pin Number	Pin Name	Pin Description
8	VDDIO	Digital I/O supply voltage
9	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
10	REGOUT	Regulator filter capacitor connection
11	FSYNC	Frame synchronization digital input. Connect to GND if unused.
12	INT	Interrupt digital output (totem pole or open-drain)
13	VDD	Power supply voltage and Digital I/O supply voltage
18	GND	Power supply ground
19	RESV	Reserved. Do not connect.
20	RESV	Reserved. Connect to GND.
22	nCS	Chip select (SPI mode only)
23	SCL / SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
24	SDA / SDI	I^2C serial data (SDA); SPI serial data input (SDI)
1 – 7, 14 – 17, 21	NC	No Connect pins. Do not connect.

Table 8 Signal Descriptions

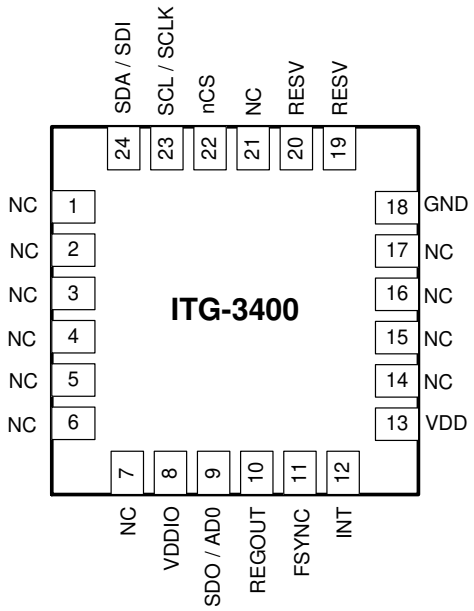
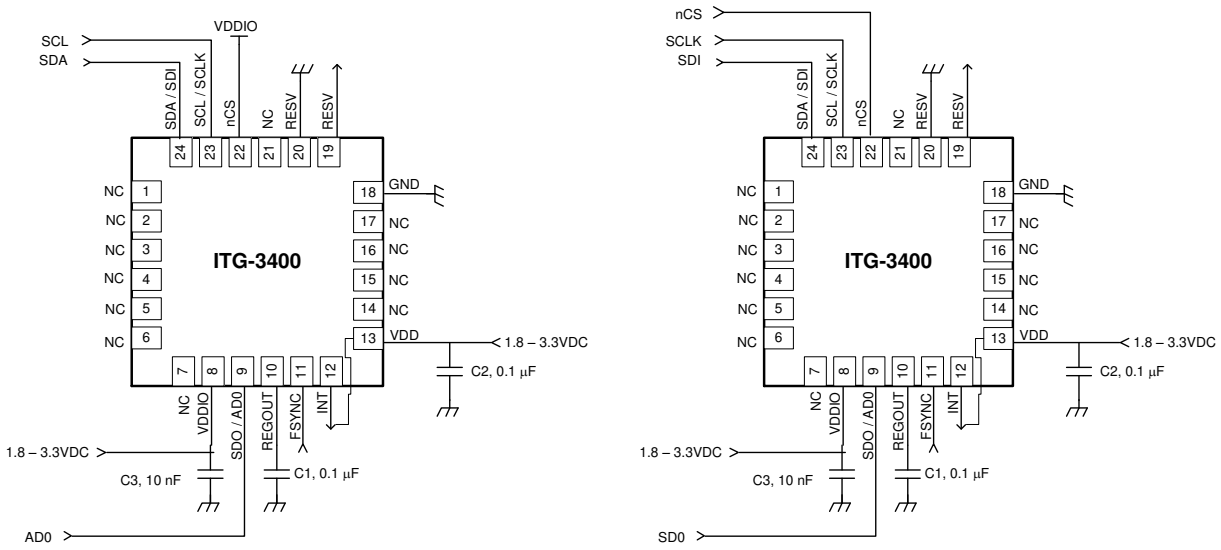


Figure 3 Pin out Diagram for ITG-3400 3.0x3.0x0.9mm QFN

4.2 Typical Operating Circuit



(a) (b)

Figure 4 ITG-3400 QFN Application Schematic. (a) I2C operation, (b) SPI operation.

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
PLL Filter Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 2V	1
VDD Bypass Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10nF ±10%, 4V	1

Table 9 Bill of Materials

4.4 Block Diagram

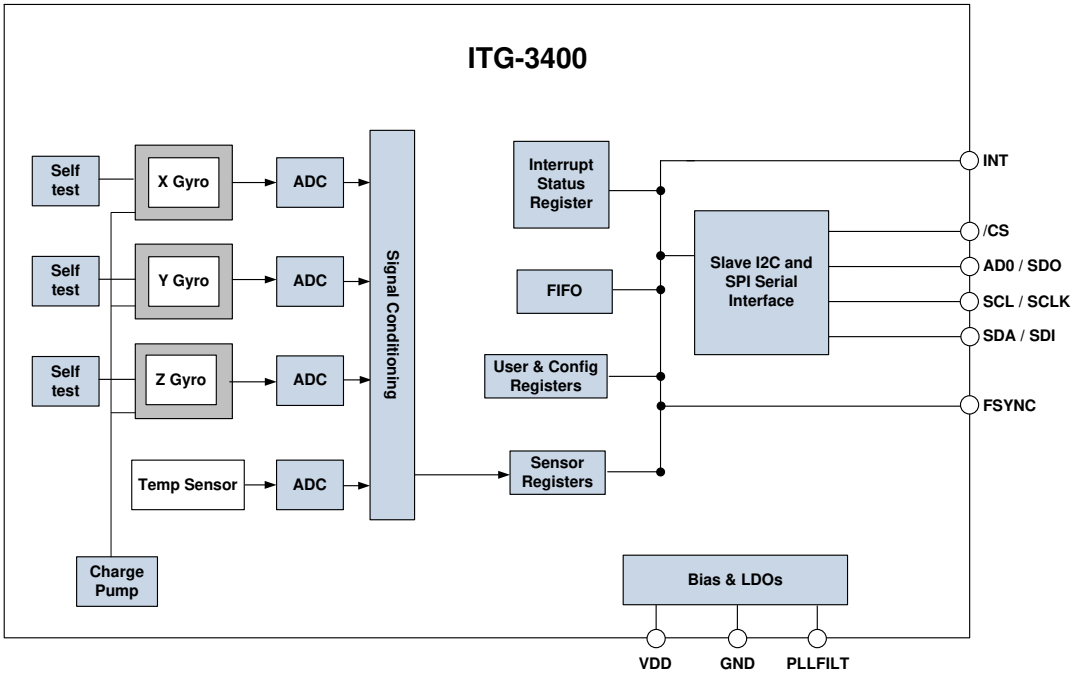


Figure 5 ITG-3400 Block Diagram

4.5 Overview

The ITG-3400 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The ITG-3400 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered

to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 I2C and SPI Serial Communications Interfaces

The ITG-3400 communicates to a system processor using either a SPI or an I^2C serial interface. The ITG-3400 always acts as a slave when communicating to the system processor. The LSB of the of the I^2C slave address is set by pin 4 (AD0).

4.7.1 ITG-3400 Solution Using I2C Interface

In the figure below, the system processor is an I^2C master to the ITG-3400.

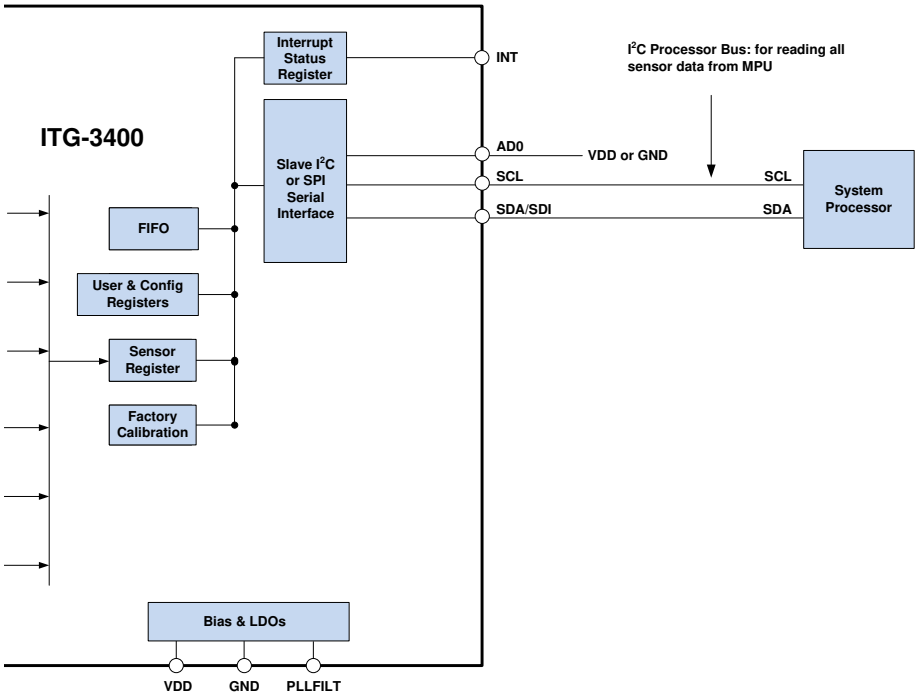


Figure 6 ITG-3400 Solution Using I^2C Interface

4.7.2 ITG-3400 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ITG-3400. Pins 2, 3, 4, and 5 are used to support the SCLK, SDI, SDO, and CS signals for SPI communications.

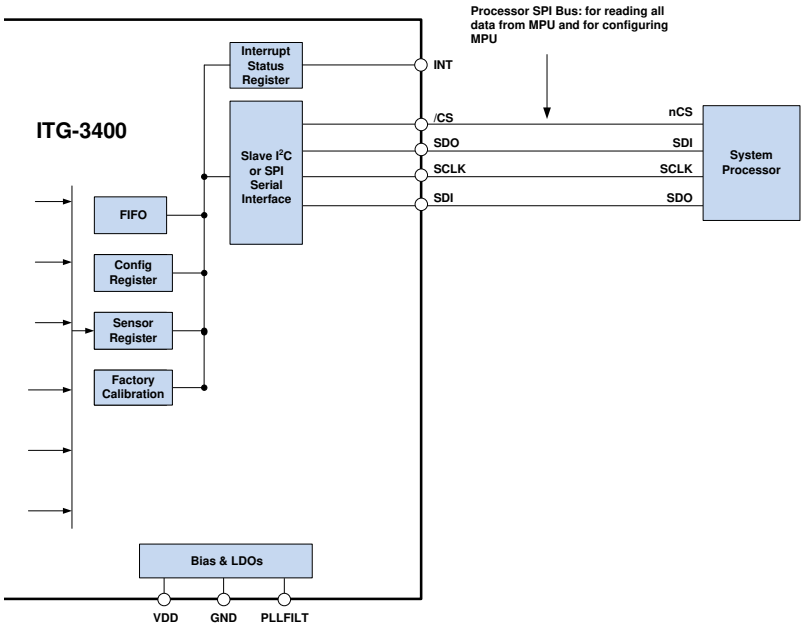


Figure 7 ITG-3400 Solution Using SPI Interface

4.8 Clocking

The ITG-3400 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- Any of the X, Y, or Z gyros (MEMS oscillators with a variation of ±1% over temperature)

Selection of the source for generating the internal synchronous clock depends on the requirements for power consumption and clock accuracy. These requirements will most likely vary by mode of operation.

There are also start-up conditions to consider. When the ITG-3400 first starts up, the device uses its internal clock until programmed to operate from another source. This allows the user, for example, to wait for the MEMS oscillators to stabilize before they are selected as the clock source.

4.9 Sensor Data Registers

The sensor data registers contain the latest gyro, auxiliary sensor, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.10 FIFO

The ITG-3400 contains a 4096-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, temperature readings, auxiliary sensor readings, and SYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

For further information regarding the FIFO, please refer to the ITG-3400 Register Map and Register Descriptions document.

4.11 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); and (2) new data is available to be read (from the FIFO and Data registers). The interrupt status can be read from the Interrupt Status register.

For further information regarding interrupts, please refer to the ITG-3400 Register Map and Register Descriptions document.

4.12 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the ITG-3400 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.13 Bias and LDOs

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ITG-3400. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at PLLFILT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.14 Charge Pump

An on-chip charge pump generates the high voltage required for the MEMS oscillators.

4.15 Standard Power Modes

The following table lists the user-accessible power modes for ITG-3400.

Mode	Name	Gyro
1	Sleep Mode	Off
2	Standby Mode	Drive On
5	Gyroscope Mode	On

Table 10 Standard Power Modes for ITG-3400

Notes:

1. Power consumption for individual modes can be found in section 3.2.1.

5 Programmable Interrupts

The ITG-3400 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

Interrupt Name	Module
FIFO Overflow	FIFO
Data Ready	Sensor Registers
I^2C Master errors: Lost Arbitration, NACKs	I^2C Master
I^2C Slave 4	I^2C Master

Table 11 Table of Interrupt Sources

For information regarding the interrupt enable/disable registers and flag registers, please refer to the ITG-3400 Register Map and Register Descriptions document. Some interrupt sources are explained below.

6 Digital Interface

6.1 I2C and SPI Serial Interfaces

The internal registers and memory of the ITG-3400 can be accessed using either I^2C at 400 kHz or SPI at 1MHz. SPI operates in four-wire mode.

Pin Number	Pin Name	Pin Description
8	VDDIO	Digital I/O supply voltage.
9	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
23	SCL / SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
24	SDA / SDI	I^2C serial data (SDA); SPI serial data input (SDI)

Table 12 Serial Interface

Note:

To prevent switching into I^2C mode when using SPI, the I^2C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 6.3.

For further information regarding the *I2C_IF_DIS* bit, please refer to the ITG-3400 Register Map and Register Descriptions document.

6.2 I2C Interface

I^2C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^2C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ITG-3400 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ITG-3400 is b110111X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two ITG-3400s to be connected to the same I^2C bus. When used in this configuration, the address of the one of the devices should be b1101110 (pin AD0 is logic low) and the address of the other should be b1101111 (pin AD0 is logic high).

6.3 I2C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I^2C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

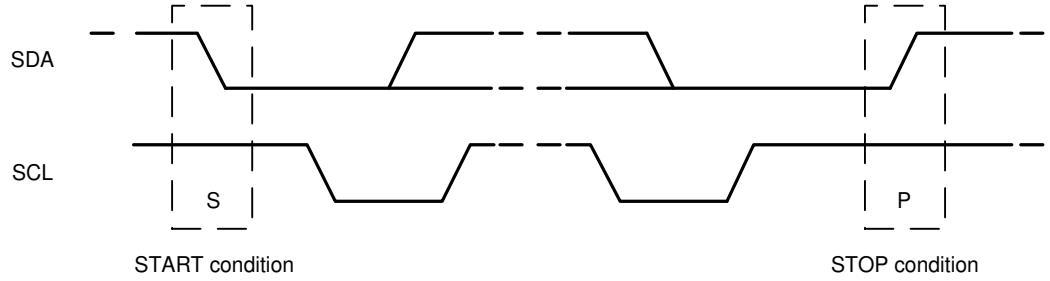


Figure 9 START and STOP Conditions

Data Format / Acknowledge

I^2C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

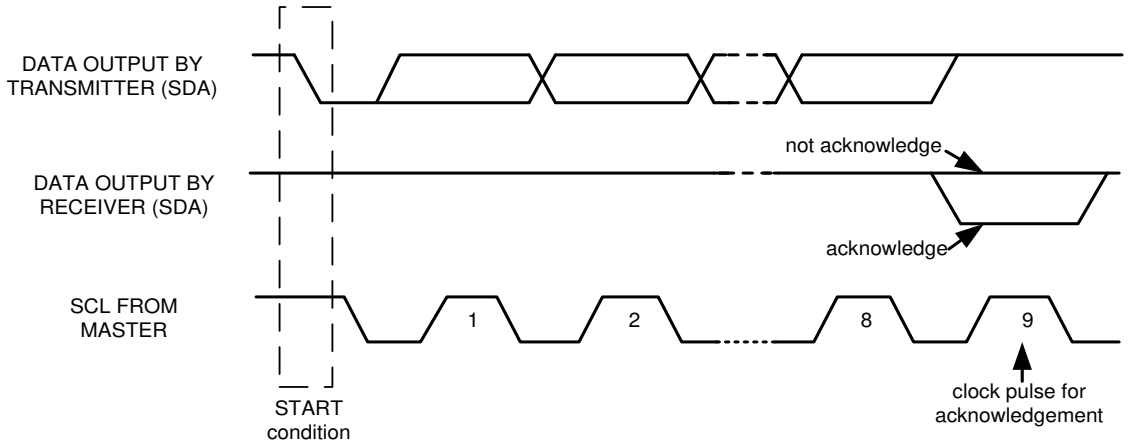


Figure 10 Acknowledge on the I^2C Bus