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# **ITG-3701**

## **Product Specification**

### **Revision 1.0**

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# 1 Document Information

## 1.1 Revision History

Date	Revision	Description
12/13/2013	1.0	Initial Release

## 1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information for the three axis ITG-3701™ gyroscopes. The device is housed in a small 3x3x0.75mm QFN package.

Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon. For references to register map and descriptions of individual registers, please refer to the ITG-3701 Register Map and Register Descriptions document.

## 1.3 Product Overview

The ITG-3701 is a single-chip, digital output, 3 Axis MEMS gyroscope IC which features a 512-byte FIFO. The FIFO can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode.

The gyroscope includes a programmable full-scale range of ±500, ±1000, ±2000, and ±4000 degrees/sec, very low Rate noise at 0.02 dps/√Hz and extremely low power consumption at 3.3mA. Factory-calibrated initial sensitivity reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, a precision clock with 1% drift from -40°C to 85°C, an embedded temperature sensor, and programmable interrupts. The device features I<sup>2</sup>C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the gyro package size down to a footprint and thickness of 3x3x0.75mm (16-pin QFN), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000g shock reliability.

## 1.4 Applications

- Health and sports monitoring
- Motion UI
- Handset gaming

## 2 Power management Features

The ITG-3701 MEMS gyroscope includes a wide range of features:

### 2.1 Sensors

- Monolithic angular rate sensor (gyros) integrated circuit
- Digital-output temperature sensor
- External sync signal connected to the FSYNC pin supports image, video and GPS synchronization
- Factory calibrated scale factor
- High cross-axis isolation via proprietary MEMS design
- 10,000g shock tolerant

### 2.2 Digital Output

- Fast Mode (400kHz) I<sup>2</sup>C serial interface
- 1 MHz SPI serial interface for full read/write capability
- 20 MHz SPI to read gyro sensor & temp sensor data.
- 16-bit ADCs for digitizing sensor outputs
- User-programmable full-scale-range of  $\pm 500^\circ/\text{sec}$ ,  $\pm 1000^\circ/\text{sec}$ ,  $\pm 2000^\circ/\text{sec}$  and  $\pm 4000^\circ/\text{sec}$

### 2.3 Data Processing

- The total data set obtained by the device includes gyroscope data, temperature data, and the one bit external sync signal connected to the FSYNC pin.
- FIFO allows burst read, reduces serial bus traffic and saves power on the system processor.
- FIFO can be accessed through both I<sup>2</sup>C and SPI interfaces.
- Programmable interrupt
- Programmable low-pass filters

### 2.4 Clocking

- On-chip timing generator clock frequency  $\pm 1\%$  drift over full temperature range

### 2.5 Power

- VDD supply voltage range of 1.71V to 3.6V
- Flexible VDDIO reference voltage allows for multiple I<sup>2</sup>C and SPI interface voltage levels
- Power consumption for three axes active: 3.3mA
- Sleep mode: 8 $\mu$ A
- Each axis can be individually powered down

### 2.6 Package

- 3x3x0.75mm footprint and maximum thickness 16-pin QFN plastic package
- MEMS structure hermetically sealed at wafer level
- RoHS and Green compliant

### 3 Electrical Characteristics

#### 3.1 Sensor Specifications

 Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T<sub>A</sub>=25°C.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
<b>GYRO SENSITIVITY</b>						
Full-Scale Range	FS_SEL=0		±500		°/s	
	FS_SEL=1		±1000		°/s	
	FS_SEL=2		±2000		°/s	
	FS_SEL=3		±4000		°/s	
Sensitivity Scale Factor	FS_SEL=0		65.5		LSB/(°/s)	
	FS_SEL=1		32.8		LSB/(°/s)	
	FS_SEL=2		16.4		LSB/(°/s)	
	FS_SEL=3		8.2		LSB/(°/s)	
Gyro ADC Word Length			16		bits	
Sensitivity Scale Factor Tolerance	25°C		±3		%	
Sensitivity Scale Factor Variation Over Temperature	-10°C to +75°C		±4		%	
Nonlinearity	Best fit straight line; 25°C		±0.3		%	
Cross-Axis Sensitivity			±5		%	
<b>GYRO ZERO-RATE OUTPUT (ZRO)</b>						
Initial ZRO Tolerance	25°C		±15		°/s	
ZRO Variation Over Temperature	-10°C to +75°C		±15		°/s	
<b>GYRO NOISE PERFORMANCE</b>						
Total RMS Noise	FS_SEL=0 DLPFCFG=2 (1-100Hz)		0.2		°/s-rms	
Rate Noise Spectral Density	At 10Hz		0.02		°/s/√Hz	
<b>GYRO MECHANICAL</b>						
Mechanical Frequency		25	27	29	kHz	
<b>GYRO START-UP TIME</b>						
ZRO Settling	DLPCFG=0, to ±1°/s of Final					
	From Sleep Mode to ready		35		ms	
	From Power On to ready		50		ms	
<b>TEMPERATURE SENSOR</b>						
Range	Untrimmed		-10 to +75		°C	
Sensitivity			321.4		LSB/°C	
Room-Temperature Offset	21°C		0		LSB	
Linearity			±0.2		°C	
<b>TEMPERATURE RANGE</b>						
Specification Temperature Range		-10		+75	°C	

### 3.2 Electrical Specifications

 Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T<sub>A</sub> = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>VDD POWER SUPPLY</b>						
Operating Voltage Range		1.71		3.6	V	
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value	1		100	ms	
Normal Operating Current	Three Axes Active		3.3		mA	
Sleep Mode Current			8		μA	
<b>VDDIO REFERENCE VOLTAGE</b> (must be regulated)						
Voltage Range		1.71		3.6	V	
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.1		100	ms	
Normal Operating Current	10pF load, 5MHz data rate. Does not include pull up resistor current draw as that is system dependent		300		μA	
<b>START-UP TIME FOR REGISTER READ/WRITE</b>						
	Ready to access registers		12		ms	
<b>I<sup>2</sup>C ADDRESS</b>						
	AD0 = 0		1101000			
	AD0 = 1		1101001			
<b>DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, /CS)</b>						
V <sub>IH</sub> , High Level Input Voltage		0.7*VDDIO			V	
V <sub>IL</sub> , Low Level Input Voltage				0.3*VDDIO	V	
C <sub>I</sub> , Input Capacitance			< 5		pF	
<b>DIGITAL OUTPUT (INT, SDO)</b>						
V <sub>OH</sub> , High Level Output Voltage	R <sub>LOAD</sub> =1MΩ	0.9*VDDIO			V	
V <sub>OL1</sub> , LOW-Level Output Voltage	R <sub>LOAD</sub> =1MΩ			0.1*VDDIO	V	
V <sub>OL.INT1</sub> , INT Low-Level Output Voltage	OPEN=1, 0.3mA sink current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t <sub>INT</sub> , INT Pulse Width	LATCH_INT_EN=0		50		μs	



### 3.3 Electrical Specifications, continued

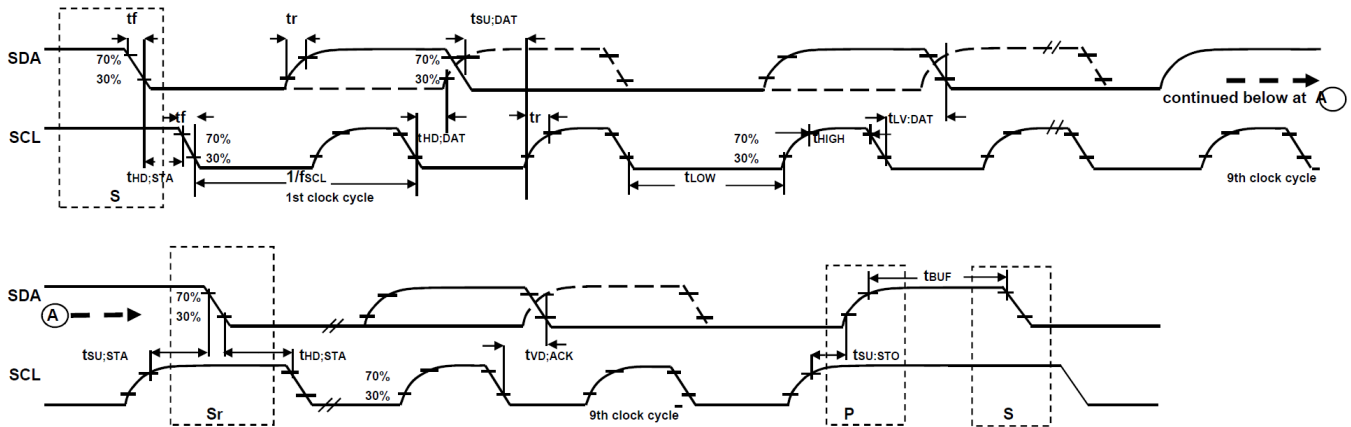
 Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T<sub>A</sub>=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>I<sup>2</sup>C I/O (SCL, SDA)</b>						
V <sub>IL</sub> , LOW Level Input Voltage			-0.5V to 0.3*VDDIO		V	
V <sub>IH</sub> , HIGH-Level Input Voltage			0.7*VDDIO to VDDIO + 0.5V		V	
V <sub>hys</sub> , Hysteresis			0.1*VDDIO		V	
V <sub>OL1</sub> , LOW-Level Output Voltage	3mA sink current		0 to 0.4		V	
I <sub>OL</sub> , LOW-Level Output Current	V <sub>OL</sub> = 0.4V		3		mA	
	V <sub>OL</sub> = 0.6V		6		mA	
Output Leakage Current			100		nA	
t <sub>of</sub> , Output Fall Time from V <sub>IHmax</sub> to V <sub>ILmax</sub>	C <sub>b</sub> bus capacitance in pf		20+0.1C <sub>b</sub> to 250		ns	
C <sub>I</sub> , Capacitance for Each I/O pin			< 10		pF	
<b>INTERNAL CLOCK SOURCE</b>						
	Fchoice=0,1,2 SMPLRT_DIV=0		32		kHz	
Sample Rate	Fchoice=3; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	
	Fchoice=3; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	
Clock Frequency Initial Tolerance	CLK_SEL=0, 6; 25°C	-2		+2	%	
	CLK_SEL=1,2,3,4,5; 25°C	-1		+1	%	
Frequency Variation over Temperature	CLK_SEL=0,6		-10 to +10		%	
	CLK_SEL=1,2,3,4,5		±1		%	
PLL Settling Time	CLK_SEL=1,2,3,4,5		4		ms	

### 3.4 I<sup>2</sup>C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T<sub>A</sub>=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>I<sup>2</sup>C TIMING</b>						
<b>I<sup>2</sup>C FAST-MODE</b>						2
f <sub>SCL</sub> , SCL Clock Frequency		0		400	kHz	
t <sub>HD,STA</sub> , (Repeated) START Condition Hold Time		0.6			μs	
t <sub>LOW</sub> , SCL Low Period		1.3			μs	
t <sub>HIGH</sub> , SCL High Period		0.6			μs	
t <sub>SU,STA</sub> , Repeated START Condition Setup Time		0.6			μs	
t <sub>HD,DAT</sub> , SDA Data Hold Time		0			μs	
t <sub>SU,DAT</sub> , SDA Data Setup Time		100			ns	
t <sub>r</sub> , SDA and SCL Rise Time	C <sub>b</sub> bus cap. from 10 to 400pF	20+0.1 C <sub>b</sub>		300	ns	
t <sub>f</sub> , SDA and SCL Fall Time	C <sub>b</sub> bus cap. from 10 to 400pF	20+0.1 C <sub>b</sub>		300	ns	
t <sub>SU,STO</sub> , STOP Condition Setup Time		0.6			μs	
t <sub>BUF</sub> , Bus Free Time Between STOP and START Condition		1.3			μs	
C <sub>b</sub> , Capacitive Load for each Bus Line			< 400		pF	
t <sub>VD,DAT</sub> , Data Valid Time				0.9	μs	
t <sub>VD,ACK</sub> , Data Valid Acknowledge Time				0.9	μs	



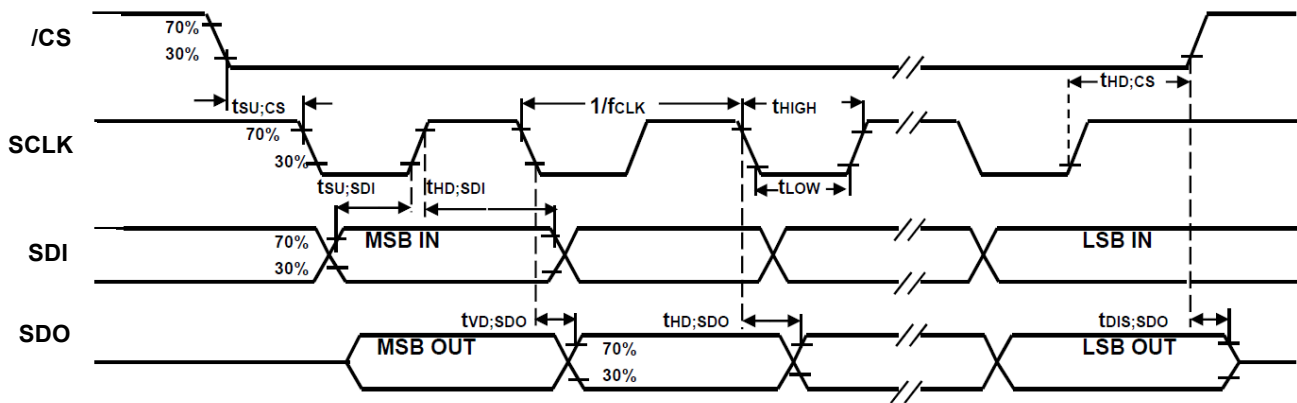
I<sup>2</sup>C Bus Timing Diagram

### 3.5 SPI Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T<sub>A</sub> = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>SPI TIMING (fSCLK = 1 MHz) R/W</b>						
f <sub>SCLK</sub> , SCLK Clock Frequency				1	MHz	
t <sub>LOW</sub> , SCLK Low Period		400			ns	
t <sub>HIGH</sub> , SCLK High Period		400			ns	
t <sub>SU,CS</sub> , CS Setup Time		8			ns	
t <sub>HD,CS</sub> , CS Hold Time		500			ns	
t <sub>SU,SDI</sub> , SDI Setup Time		11			ns	
t <sub>HD,SDI</sub> , SDI Hold Time		7			ns	
t <sub>VD,SDO</sub> , SDO Valid Time	C <sub>load</sub> = 20pF			100	ns	
t <sub>HD,SDO</sub> , SDO Hold Time		4			ns	
t <sub>DIS,SDO</sub> , SDO Output Disable Time				50	ns	
t <sub>BUF</sub> , CS high time between transactions				600	ns	

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>SPI TIMING (fSCLK = 20 MHz) Read<sup>3</sup></b>						
f <sub>SCLK</sub> , SCLK Clock Frequency				20	MHz	
t <sub>LOW</sub> , SCLK Low Period		-	25	-	ns	
t <sub>HIGH</sub> , SCLK High Period		-	25	-	ns	
t <sub>SU,CS</sub> , CS Setup Time		25			ns	
t <sub>HD,CS</sub> , CS Hold Time		25			ns	
t <sub>SU,SDI</sub> , SDI Setup Time		5			ns	
t <sub>HD,SDI</sub> , SDI Hold Time		6			ns	
t <sub>VD,SDO</sub> , SDO Valid Time	C <sub>load</sub> = 20pF			30	ns	
t <sub>HD,SDO</sub> , SDO Hold Time		4			ns	
t <sub>DIS,SDO</sub> , SDO Output Disable Time				25	ns	
t <sub>BUF</sub> , CS high time between transactions				600	ns	



SPI Bus Timing Diagram

### 3.6 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

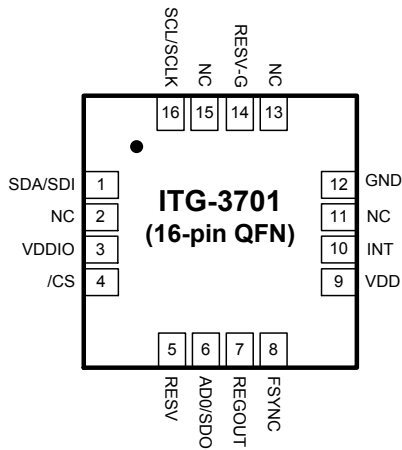
#### Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, VDD	-0.5V to 4.0V
VDDIO Input Voltage Level	-0.5V to 4.0V
REGOUT	-0.5V to 2V
Input Voltage Level (AD0, FSYNC)	-0.5V to VDDIO
SCL, SDA, INT (SPI enable)	-0.5V to VDDIO
SCL, SDA, INT (SPI disable)	-0.5V to VDDIO
Acceleration (Any Axis, unpowered)	10,000g for 0.2ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2), 125°C, ±100mA

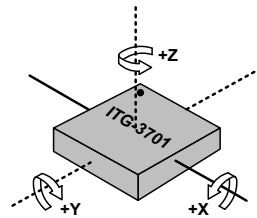
## 4 Applications Information

### 4.1 Pin Out and Signal Description

Pin Number 3x3x0.75mm	Pin Name	Pin Description
1	SDA/SDI	I <sup>2</sup> C serial data (SDA); SPI serial data input (SDI)
3	VDDIO	I/O supply voltage.
4	/CS	SPI chip select (0=SPI mode, 1= I <sup>2</sup> C mode)
5	RESV	Reserved. Do not connect.
6	AD0 / SDO	I <sup>2</sup> C Slave Address LSB (AD0); SPI serial data output (SDO)
7	REGOUT	Regulator filter capacitor connection
8	FSYNC	Frame synchronization digital input. Connect to GND if not used.
9	VDD	Power supply voltage
10	INT	Interrupt digital output (totem pole or open-drain)
12	GND	Power supply ground
14	RESV-G	Reserved. Connect to Ground.
16	SCL/SCLK	I <sup>2</sup> C serial clock (SCL); SPI serial clock (SCLK)
2, 11, 13, 15	NC	Not internally connected. May be used for PCB trace routing.

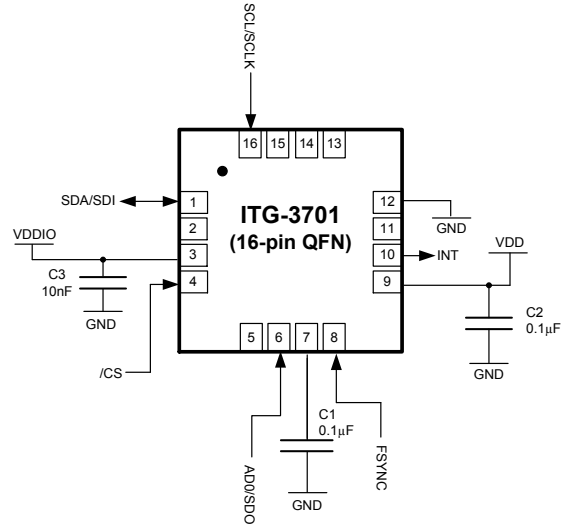


**QFN Package (Top View)**  
 16-pin, 3mm x 3mm x 0.75mm  
 Footprint and maximum thickness



**Orientation of Axes of Sensitivity and Polarity of Rotation**

### 4.2 Typical Operating Circuit



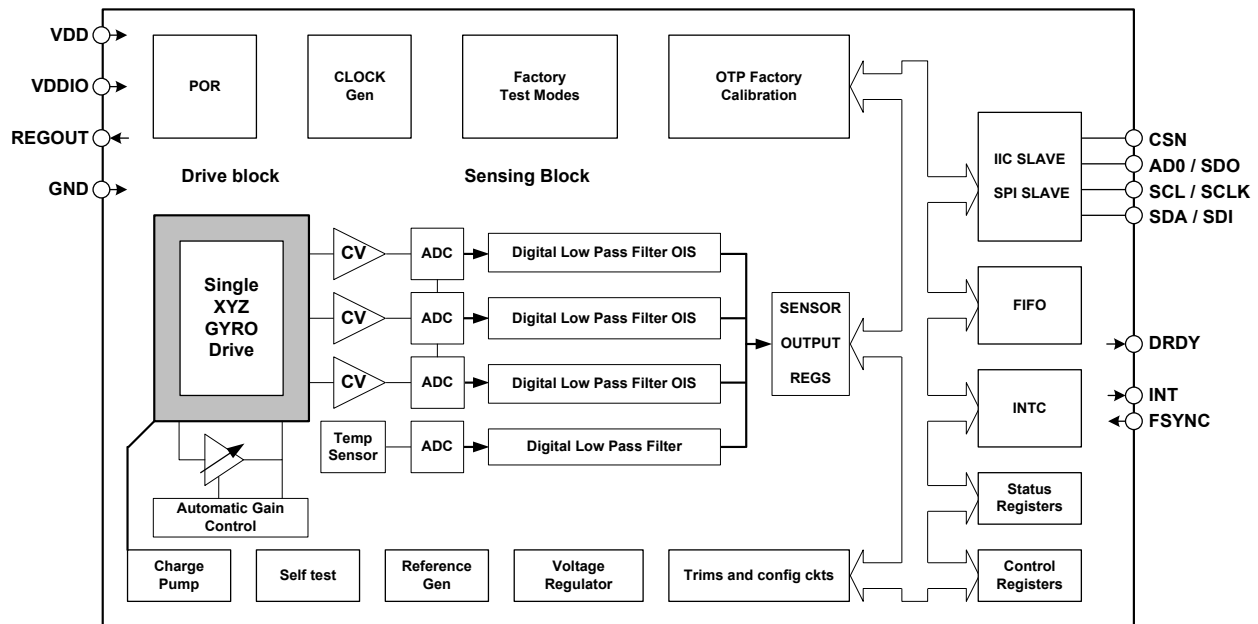
Typical Operating Circuit

### 4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
Regulator Filter Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 2V	1
VDD Bypass Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10nF ±10%, 4V	1

## 5 Functional Overview

### 5.1 Block Diagram



### 5.2 Overview

The ITG-3701 is comprised of the following key blocks / functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- I<sup>2</sup>C and SPI serial communications interfaces
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO

### 5.3 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The ITG-3701 consists of a single structure vibratory MEMS rate gyroscope, which detects rotation about the XY&Z axes, respectively. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pick off. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The chip features a programmable full-scale range of the gyroscope sensors of  $\pm 500$ ,  $\pm 1000$ ,  $\pm 2000$ , and  $\pm 4000$  dps. User-selectable low-pass filters enable a wide range of cut-off frequencies. The ADC sample rate can be programmed to 32 kHz, 8 kHz, 1 kHz, 500 Hz, 333.3 Hz, 250 Hz, 200 Hz, 166.7 Hz, 142.9 Hz, or 125 Hz.

### 5.4 I<sup>2</sup>C and SPI Serial Communications Interface

The ITG-3701 has both I<sup>2</sup>C and SPI serial interfaces. The device always acts as a slave when communicating to the system processor. The logic level for communications to the master is set by the voltage on the VDDIO pin. The LSB of the I<sup>2</sup>C slave address is set by the AD0 pin. The I<sup>2</sup>C and SPI protocols are described in more detail in Section 6.

## 5.5 Internal Clock Generation

The ITG-3701 uses a flexible clocking scheme, allowing for a variety of internal clock sources for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, various control circuits, and registers.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- PLL (gyroscope based clock)

In order for the gyroscope to perform to spec, the PLL must be selected as the clock source. When the internal 20MHz oscillator is chosen as the clock source, the device can operate while having the gyroscope disabled. However, this is only recommended if the user wishes to use the internal temperature sensor in this mode.

## 5.6 Sensor Data Registers

The sensor data registers contain the latest gyro and temperature data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime, however, the interrupt function may be used to determine when new data is available.

## 5.7 FIFO

The ITG-3701 contains a 512-byte FIFO register that is accessible via the both the I<sup>2</sup>C and SPI Serial Interfaces. The FIFO configuration register determines what data goes into it, with possible choices being gyro data, temperature readings and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

## 5.8 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources), (2) new data is available to be read (from the FIFO and Data registers), and (3) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

## 5.9 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the device's die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

## 5.10 Bias and LDO

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ITG-3701. Its two inputs are unregulated VDD of 1.71V to 3.6V and a VDDIO logic reference supply voltage of 1.71V to 3.6V. The LDO output is bypassed by a 0.1µF capacitor at REGOUT.



## 6 Digital Interface

### 6.1 I<sup>2</sup>C Serial Interface

The internal registers and memory of the ITG-3701 can be accessed using the I<sup>2</sup>C interface.

#### Serial Interface

Pin Number	Pin Name	Pin Description
3	VDDIO	Digital I/O supply voltage.
6	AD0 / SDO	I <sup>2</sup> C Slave Address LSB (AD0); SPI serial data output (SDO)
16	SCL / SCLK	I <sup>2</sup> C serial clock (SCL); SPI serial clock (SCLK)
1	SDA / SDI	I <sup>2</sup> C serial data (SDA); SPI serial data input (SDI)

#### 6.1.1 I<sup>2</sup>C Interface

I<sup>2</sup>C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I<sup>2</sup>C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ITG-3701 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

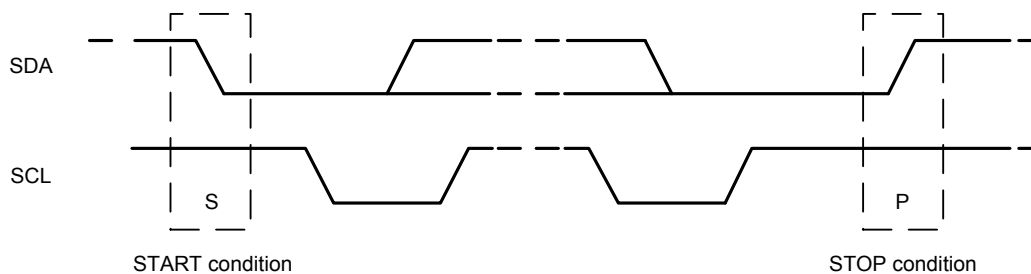
The slave address of the device is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows the device to be connected to the same I<sup>2</sup>C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high). The I<sup>2</sup>C address is stored in WHO\_AM\_I register.

#### I<sup>2</sup>C Communications Protocol

##### *START (S) and STOP (P) Conditions*

Communication on the I<sup>2</sup>C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

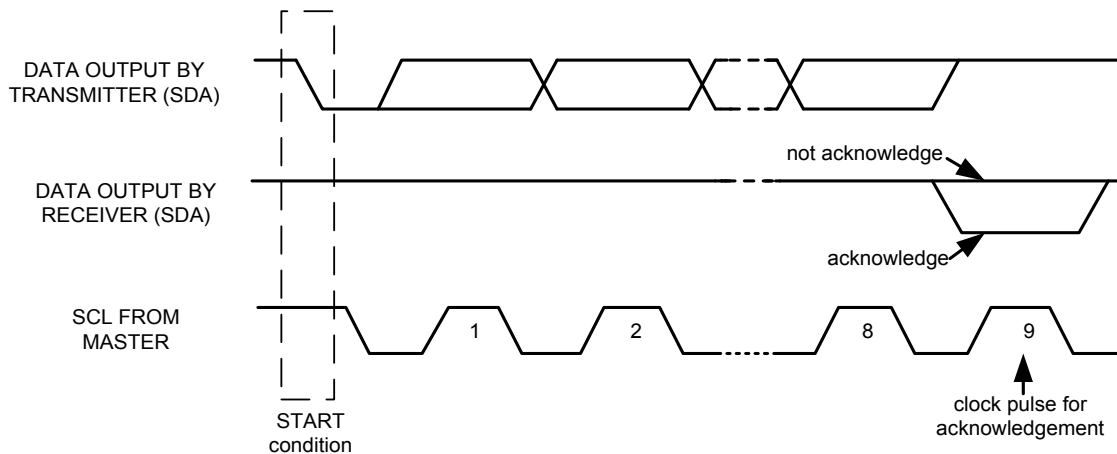


**START and STOP Conditions**

Data Format / Acknowledge

I<sup>2</sup>C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

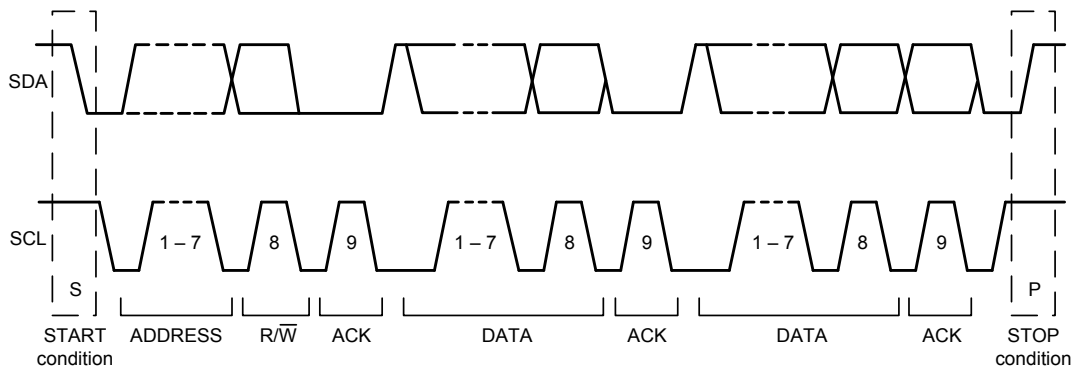
If a slave is busy and is unable to transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).



**Acknowledge on the I<sup>2</sup>C Bus**

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8<sup>th</sup> bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.



**Complete I<sup>2</sup>C Data Transfer**

To write the internal registers, the master transmits the start condition (S), followed by the I<sup>2</sup>C address and the write bit (0). At the 9<sup>th</sup> clock cycle (when the clock is high), the device acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the device acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the device automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

### Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

### Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal device registers, the master sends a start condition, followed by the I<sup>2</sup>C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the device, the master transmits a start signal followed by the slave address and read bit. As a result, the device sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9<sup>th</sup> clock cycle. The following figures show single and two-byte read sequences.

### Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

### Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

## I<sup>2</sup>C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I <sup>2</sup> C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9 <sup>th</sup> clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9 <sup>th</sup> clock cycle
RA	The internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

## 6.1.2 SPI interface

SPI is a 4-wire synchronous serial interface that uses two control and two data lines. The ITG-3701 always operates as a Slave device during standard Master-Slave SPI operation. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDO) and the Data Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (/CS) for each Slave device; /CS goes low at the start of transmission and goes back high at the end. The Serial Data Output (SDO) line, remains in a high-impedance (high-z) state when the device is not selected, so it does not interfere with any active devices.

### SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. SCLK frequency is 1MHz max for SPI in full read/write capability mode. When the SPI frequency is set to 20MHz, its operation is limited to reading sensor registers only.
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

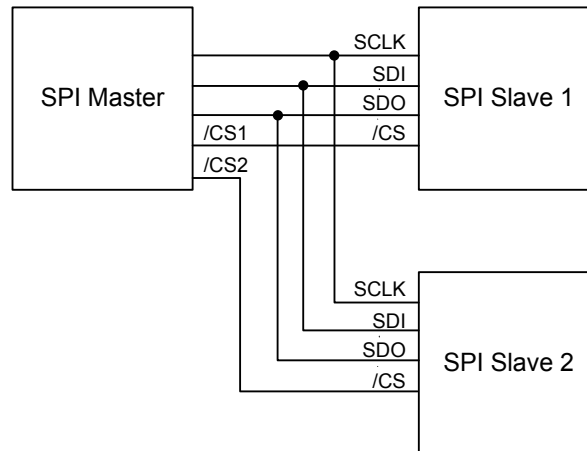
#### SPI Address format

MSB							LSB
R/W	A6	A5	A4	A3	A2	A1	A0

#### SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

**Typical SPI Master / Slave Configuration**

Each SPI slave requires its own Chip Select (/CS) line. SDO, SDI and SCLK lines are shared. Only one /CS line is active (low) at a time ensuring that only one slave is selected at a time. The /CS lines of other slaves are held high which causes their respective SDO pins to be high-Z.

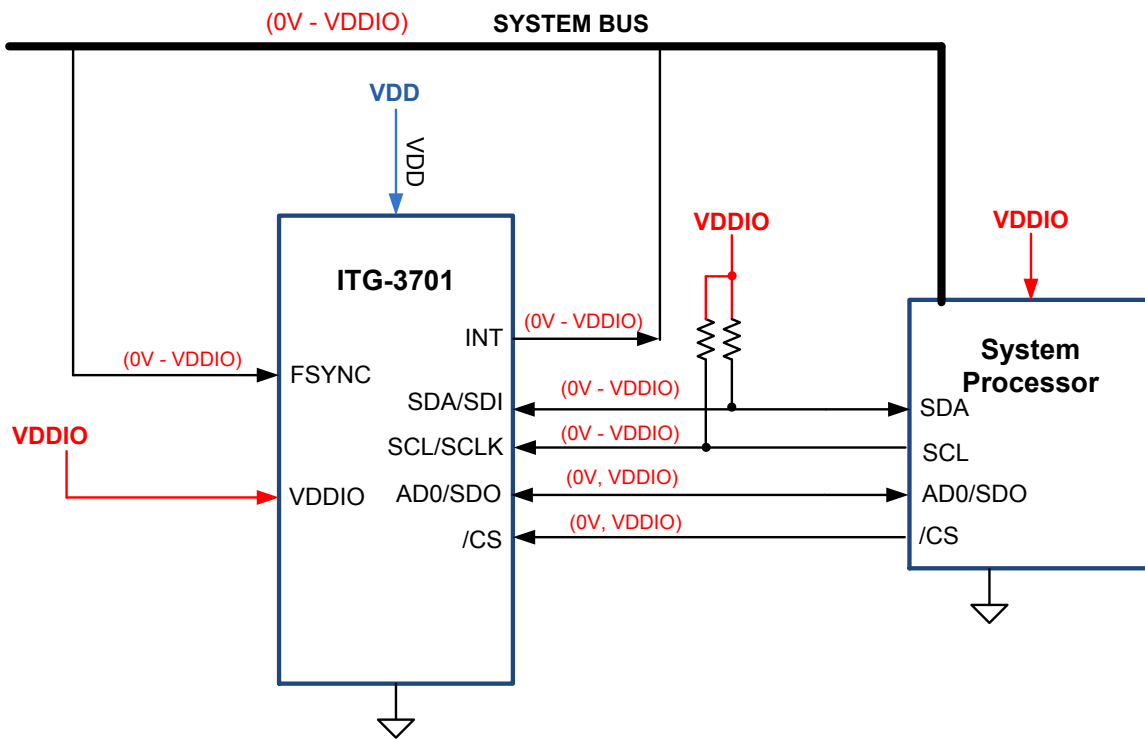
## 7 Serial Interface Considerations

### 7.1 Supported Interfaces

The ITG-3701 supports I<sup>2</sup>C and SPI communications.

### 7.2 Logic Levels

The I/O logic levels are set to VDDIO. VDDIO may be set to be equal to VDD or to another voltage, such that it is between 1.71 V and 3.6V at all times. Both I<sup>2</sup>C and SPI communication support VDDIO.

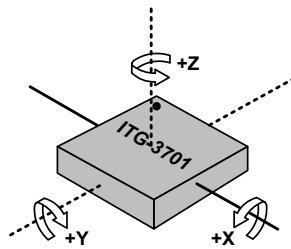


## 8 Assembly

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in Quad Flat No leads package (QFN) surface mount integrated circuits.

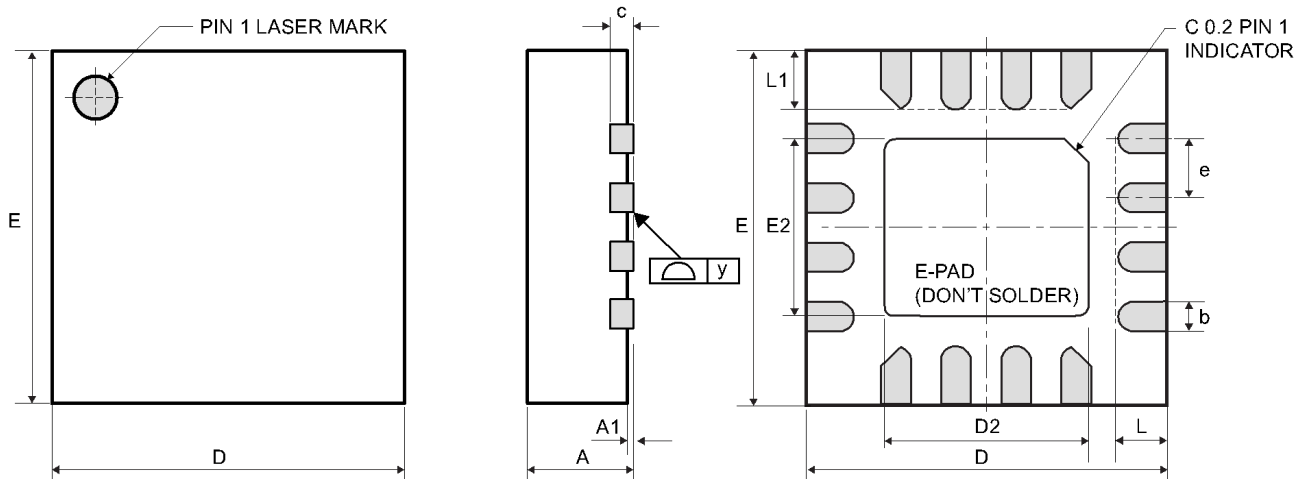
### 8.1 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier in the figure.



**Orientation of Axes of Sensitivity and Polarity of Rotation**

## 8.2 Package Dimensions



Dimensions in Millimeters			
Dimension	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	---	0.15 ref	---
D	2.90	3.00	3.10
D2	1.65	1.70	1.75
E	2.90	3.00	3.10
E2	1.45	1.50	1.55
e	---	0.50	---
L	0.35	0.40	0.45
L1	0.45	0.50	0.55
y	0.000	---	0.075

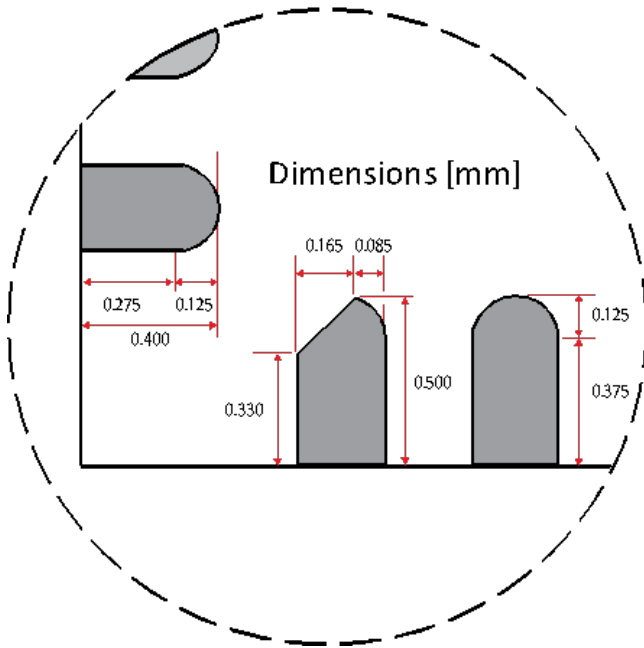
## 8.3 PCB Design Guidelines

Do not solder the center Exposed Pad (E-pad). This is a solder keep-out area.

### Recommendations:

Size the PCB pad layout to match the QFN pad leads. Use the package dimensions shown in the Table above. The Dimensions Table is supplemented with the first figure that follows.

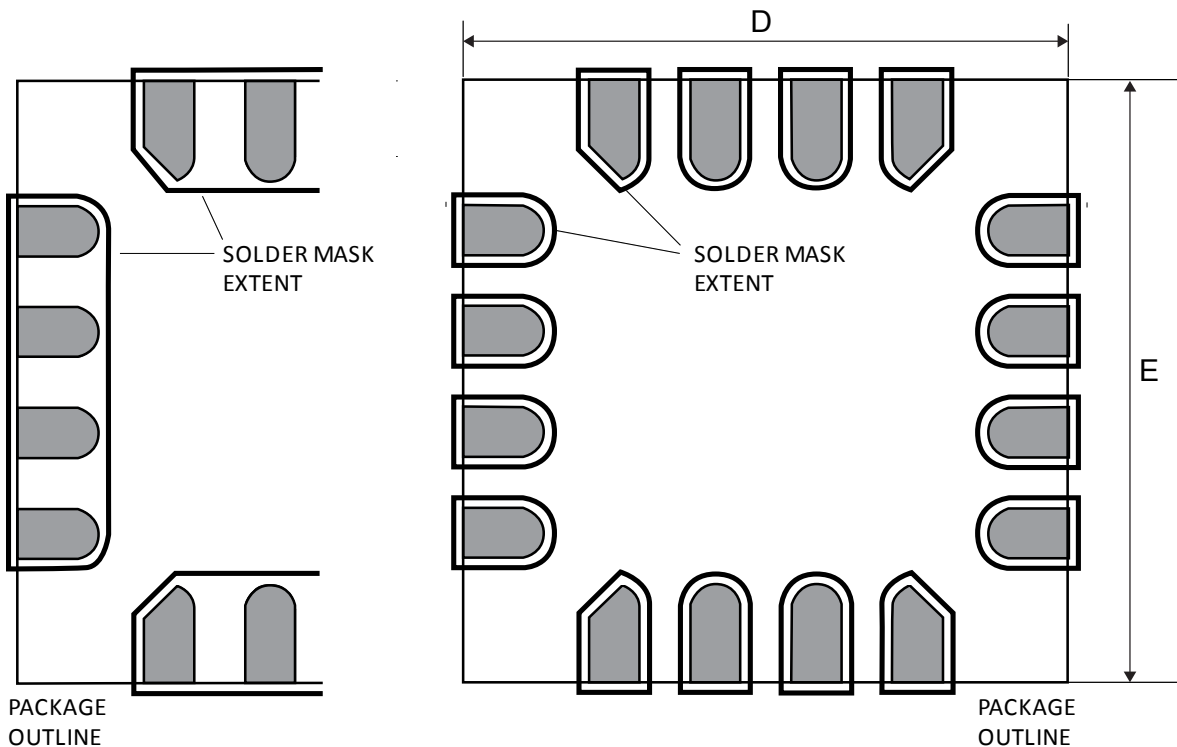




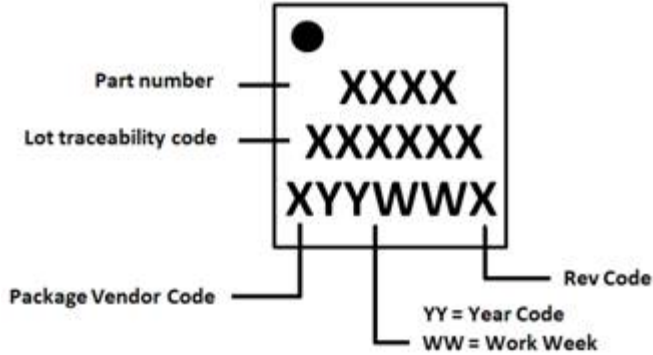
Design the PCB pad layout with Non Solder Mask Defined pads (NSMD). NSMD pads are recommended over Solder Mask Defined (SMD) pads. NSMD pads provide a tighter tolerance on copper etching, provide a larger copper pad area, and allow the solder to anchor to the edges of the copper pads to improve solder joint reliability. As a recommendation, set the solder mask aperture a minimum of 0.05 mm larger than the component solder pad per edge. Two alternative PCB layouts are shown below for reference.

**Blocked Areas – Solder Mask**

**Individually Outlined Pads – Solder Mask**



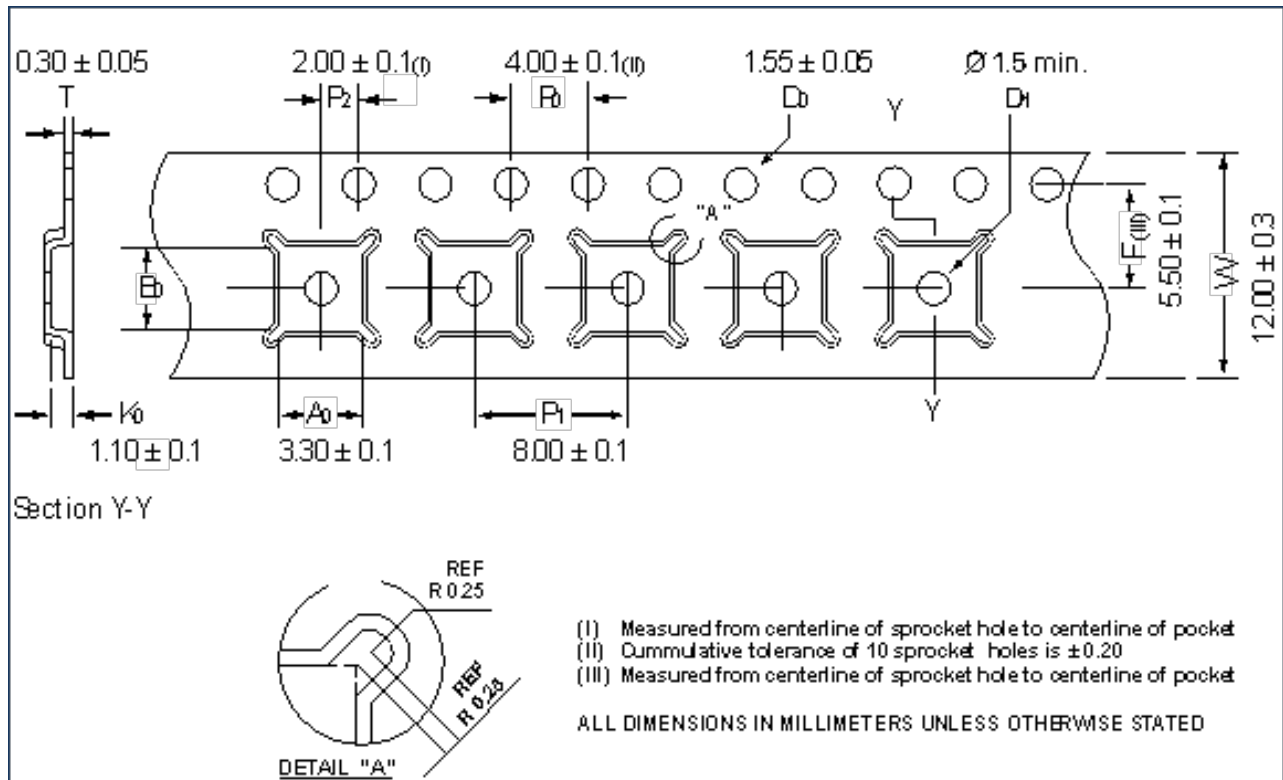
**8.4 Product Marking Specification**



Part number Identification:

Product	Top Mark
ITG-3701	IT37

**8.5 Tape & Reel Specification**



- (I) Measured from centerline of sprocket hole to centerline of pocket
- (II) Cumulative tolerance of 10 sprocket holes is ±0.20
- (III) Measured from centerline of sprocket hole to centerline of pocket

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED