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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# ITS4200S-SJ-D

Smart High-Side NMOS-Power Switch

## Data Sheet

Rev 1.0, 2012-09-01

Standard Power



## 1 Overview

### Features

- CMOS compatible input
- Switching all types of resistive, inductive and capacitive loads
- Fast demagnetization of inductive loads
- Very low standby current
- Optimized Electromagnetic Compatibility (EMC)
- Open drain diagnostic output for overtemperature and short circuit
- Open load detection in OFF-state with external resistor
- Overload protection
- Current limitation
- Short circuit protection
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Reverse battery protection with external resistor
- Loss of GND and loss of V<sub>bb</sub> protection
- Electrostatic Discharge Protection (ESD)
- Green Product (RoHS compliant)

ITS4200S-SJ-D is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications.

### Description

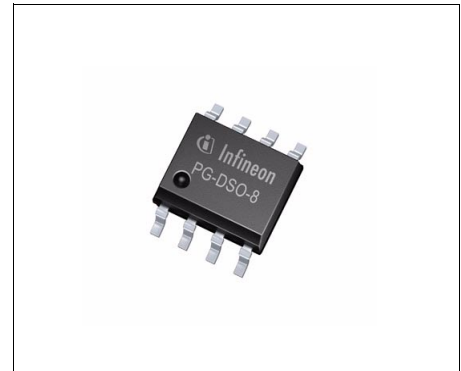
The ITS4200S-SJ-D is a protected 200m Ω single channel Smart High-Side NMOS-Power Switch in a PG-DSO-8 package with charge pump, CMOS compatible input and diagnostic feedback.

### Product Summary

Overvoltage protection  $V_{SAZmin} = 62V$   
 Operating voltage range:  $6V < V_S < 52V$   
 On-state resistance  $R_{DSON} = \text{typ } 150m\Omega$   
 Nominal load current  $I_{LNOM} = 1.2A$   
 Operating Temperature range:  $T_j = -40^\circ C$  to  $125^\circ C$

### Application

- All types of resistive, inductive and capacitive loads
- Power switch for 12V, 24V and 45V DC applications with CMOS compatible control interface
- Open drain diagnosis feedback for overtemperature and short circuit
- Driver for electromagnetic relays
- Power management for high-side-switching with low current consumption in OFF-mode



PG-DSO-8

Type	Package	Marking
ITS4200S-SJ-D	PG-DSO-8	I200SD

## 2 Block Diagram and Terms

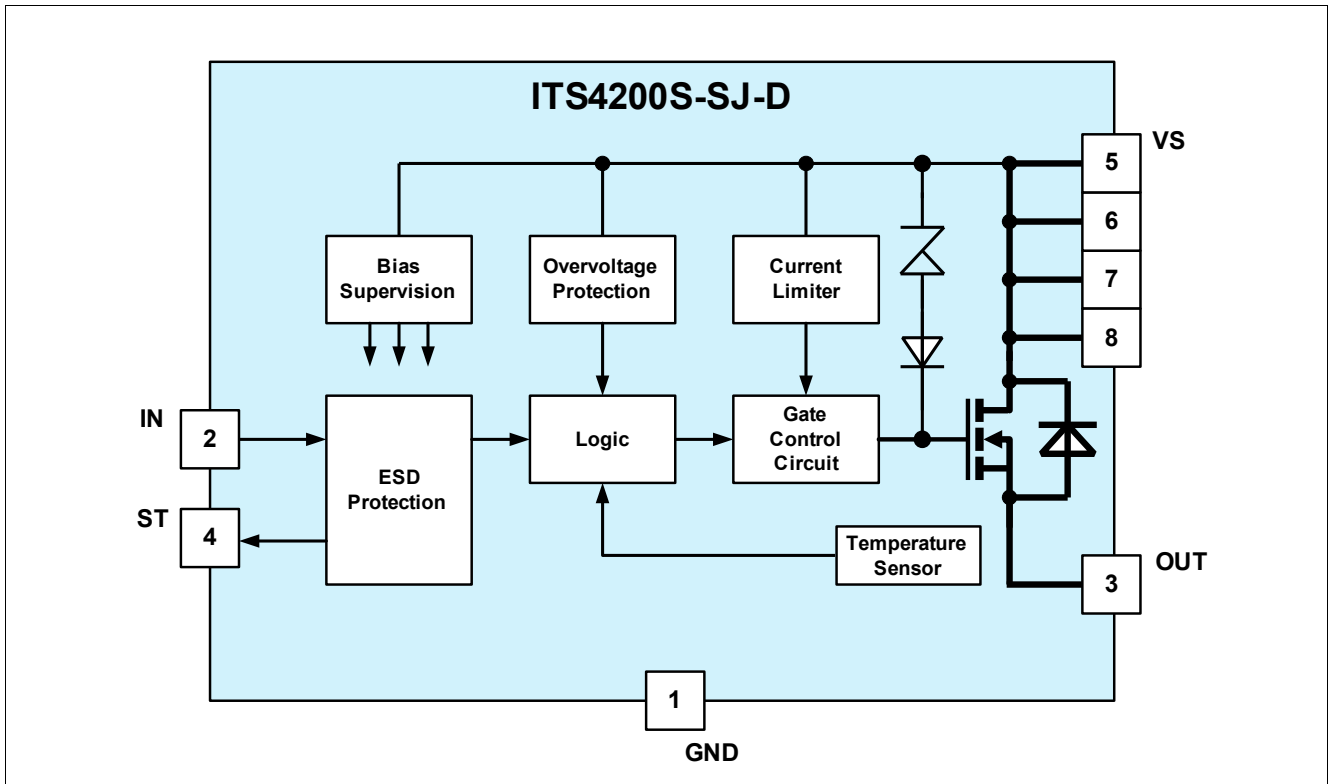


Figure 1 Block diagram

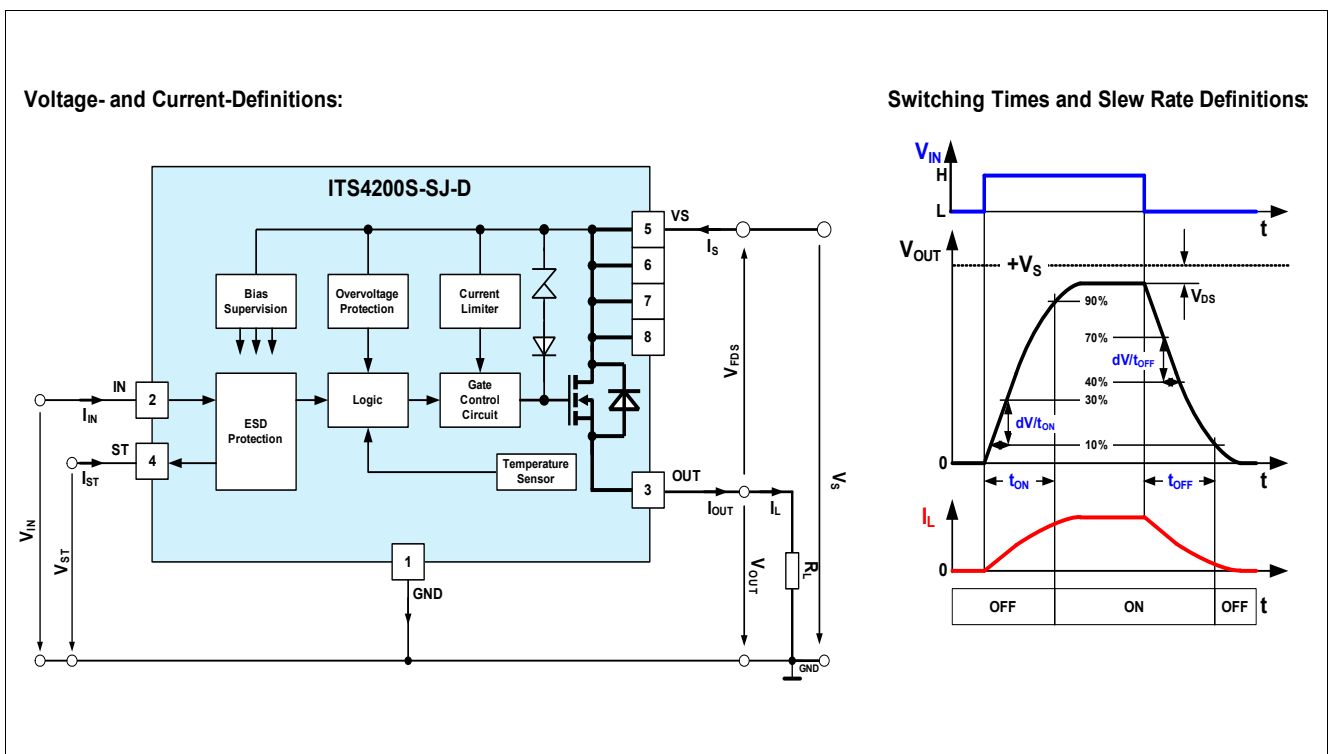


Figure 2 Terms - parameter definition

### 3 Pin Configuration

#### 3.1 Pin Assignment

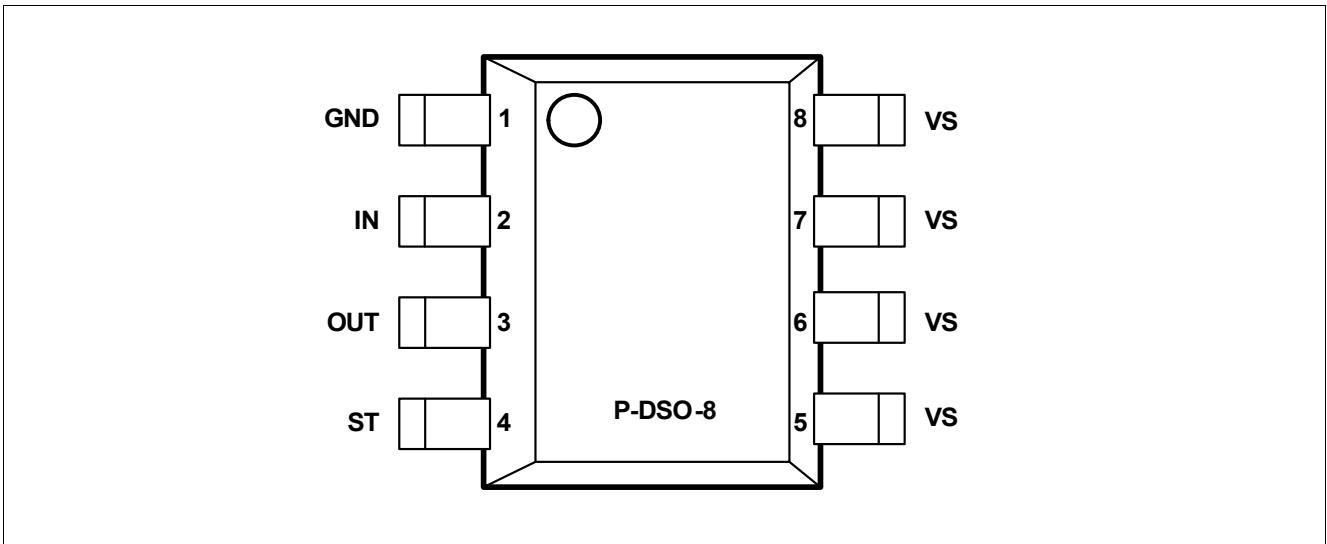


Figure 3 Pin configuration top view, PG-DSO-8

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Logic ground
2	IN	Input, controls the power switch; the powerswitch is ON when high
3	OUT	Output to the load
4	ST	Status flag; diagnosis feedback; NMOS open drain
5, 6, 7, 8	VS	Supply voltage (design the wiring for the maximum short circuit current and also for low thermal resistance)

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute maximum ratings <sup>1)</sup> at  $T_j = 25^\circ\text{C}$  unless otherwise specified. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Supply voltage VS</b>							
Voltage	$V_S$			52	V		4.1.1
Voltage for short circuit protection	$V_{SSC}$			36	V		4.1.2
<b>Output stage OUT</b>							
Output Current; (Short circuit current see electrical characteristics)	$I_{OUT}$			self limited	A		4.1.3
<b>Input IN</b>							
Current	$I_{IN}$	-5		5	mA		4.1.4
<b>Status ST</b>							
Current	$I_{ST}$	-5		5	mA		4.1.5
<b>Temperatures</b>							
Junction Temperature	$T_j$	-40		125	$^\circ\text{C}$		4.1.6
Storage Temperature	$T_{stg}$	-55		125	$^\circ\text{C}$		4.1.7
<b>Power dissipation</b>							
$T_a = 25^\circ\text{C}^{2)}$	$P_{tot}$			1.4	W		4.1.8
<b>Inductive load switch-off energy dissipation</b>							
$T_j = 125^\circ\text{C}; I_L = 1\text{A}^{3)}$	$E_{AS}$			125	mJ	single pulse	4.1.9
<b>ESD Susceptibility</b>							
ESD susceptibility (input pin)	$V_{ESD}$	-1		1	kV	HBM <sup>4)</sup>	4.1.10
ESD susceptibility (all other pins)	$V_{ESD}$	-5		5	kV	HBM <sup>5)</sup>	4.1.11

1) Not subject to production test, specified by design

2) Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70mm thick) copper area for V<sub>bb</sub> connection. PCB is vertical without blown air

3) Not subject to production test, specified by design

4) ESD susceptibility HBM according to EIA/JESD 22-A 114.

5) ESD susceptibility HBM according to EIA/JESD 22-A 114.

*Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.*

## 4.2 Functional Range

**Table 2** Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	$V_S$	6		52	V	$V_S$ increasing	4.2.1

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 3** Thermal Resistance<sup>1)</sup>

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance - Junction to pin5	$R_{thj-pin5}$		23.3		K/W		4.3.1
Thermal Resistance - Junction to Ambient - 1s0p, minimal footprint	$R_{thJA\_1s0p}$		128.7		K/W	<sup>2)</sup>	4.3.2
Thermal Resistance - Junction to Ambient - 1s0p, 300mm <sup>2</sup>	$R_{thJA\_1s0p\_300mm^2}$		70.1		K/W	<sup>3)</sup>	4.3.3
Thermal Resistance - Junction to Ambient - 1s0p, 600mm <sup>2</sup>	$R_{thJA\_1s0p\_600mm^2}$		65.6		K/W	<sup>4)</sup>	4.3.4
Thermal Resistance - Junction to Ambient - 2s2p	$R_{thJA\_2s2p}$		55.4		K/W	<sup>5)</sup>	4.3.5
Thermal Resistance - Junction to Ambient with thermal vias - 2s2p	$R_{thJA\_2s2p}$		53.5		K/W	<sup>6)</sup>	4.3.6

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70 $\mu$ m Cu.
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm<sup>2</sup>; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70 $\mu$ m Cu.
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm<sup>2</sup>; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70 $\mu$ m Cu.
- 5) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 $\mu$ m Cu, 2 x 35 $\mu$ m Cu).
- 6) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 $\mu$ m Cu, 2 x 35 $\mu$ m Cu). The diameter of the two vias are equal 0.3mm and have a plating of 25 $\mu$ m with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.



## 5 Electrical Characteristics

**Table 4**  $V_S = 12V$  to  $42V$ ;  $T_j = -40^\circ C$  to  $125^\circ C$ ; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at  $V_S = 13.5V$ ,  $T_j = 25^\circ C$

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Powerstage</b>							
NMOS ON Resistance	$R_{DSON}$		150	200	m $\Omega$	$I_{OUT} = 1A$ ; $T_j = 25^\circ C$ ; $9V < V_S < 52V$ ; $V_{IN} = 5V$	5.0.1
NMOS ON Resistance	$R_{DSON}$		250	350	m $\Omega$	$I_{OUT} = 1A$ ; $T_j = 125^\circ C$ ; $9V < V_S < 52V$ ; $V_{IN} = 5V$	5.0.2
Nominal Load Current; device on PCB <sup>1)</sup>	$I_{LNOM}$	1.2			A	$T_{pin5} = 85^\circ C$	5.0.3
<b>Timings of Power Stages<sup>2)</sup></b>							
Turn ON Time(to 90% of $V_{out}$ ); $V_S$ to GND transition of $V_{IN}$	$t_{ON}$		80	180	$\mu s$	$V_S = 13.5V$ ; $R_L = 47\Omega$	5.0.4
Turn OFF Time (to 10% of $V_{out}$ ); $V_S$ to GND transition of $V_{IN}$	$t_{OFF}$		80	200	$\mu s$	$V_S = 13.5V$ ; $R_L = 47\Omega$	5.0.5
ON-Slew Rate (10 to 30% of $V_{out}$ ); L to H transition of $V_{IN}$	$SR_{ON}$		0.7	2.0	V / $\mu s$	$V_S = 13.5V$ ; $R_L = 47\Omega$	5.0.6
OFF-Slew Rate; $dV_{OUT} / dt_{ON}$ (70 to 40% of $V_{out}$ ); H to L transition of $V_{IN}$	$SR_{OFF}$		0.9	2.0	V / $\mu s$	$V_S = 13.5V$ ; $R_L = 47\Omega$	5.0.7
<b>Under voltage lockout (charge pump start-stop-restart)</b>							
Supply undervoltage; charge pump stop voltage	$V_{SUV}$			4	V	$V_S$ decreasing $-40^\circ C < T_j < 85^\circ C$	5.0.8
Supply undervoltage; Charge pump stop voltage	$V_{SUV}$			5.5	V	$V_S$ decreasing $T_j = 125^\circ C$	5.0.9
Supply startup voltage; Charge pump restart voltage	$V_{SSU}$		4	5.5	V	$V_S$ increasing	5.0.10
<b>Current consumption</b>							
Operating current	$I_{GND}$		0.8	2	mA	$V_{IN} = 5V$	5.0.11
Standby current	$I_{SSTB}$			15	$\mu A$	$V_{IN} = 0V$ ; $V_{OUT} = 0V$ $-40^\circ C < T_j < 85^\circ C$	5.0.12
Standby current	$I_{SSTB}$			18	$\mu A$	$V_{IN} = 0V$ ; $T_j = 125^\circ C$	5.0.13
Output leakage current	$I_{OUTLK}$			5	$\mu A$	$V_{IN} = 0V$ ; $V_{OUT} = 0V$	5.0.14
<b>Protection functions <sup>3)</sup></b>							
Initial peak short circuit current limit	$I_{LSCP}$			9	A	$T_j = -40^\circ C$ ; $V_S = 20V$ ; $V_{IN} = 5.0V$ ; $t_m = 150\mu s$	5.0.15
Initial peak short circuit current limit	$I_{LSCP}$		6.5		A	$T_j = 25^\circ C$ ; $V_S = 20V$ ; $V_{IN} = 5.0V$ ; $t_m = 150\mu s$	5.0.16



## Electrical Characteristics

**Table 4**  $V_S = 12V$  to  $42V$ ;  $T_j = -40^\circ C$  to  $125^\circ C$ ; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at  $V_S = 13.5V$ ,  $T_j = 25^\circ C$

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Initial peak short circuit current limit	$I_{LSCP}$	4			A	$T_j = 125^\circ C$ ; $V_S = 20V$ ; $V_{IN} = 5.0V$ ; $t_m = 150\mu s$	5.0.17
Initial peak short circuit current limit <sup>4)</sup>	$I_{LSCP}$		5		A	$V_S > 40V$ ; $V_{IN} = 5.0V$ ; $t_m = 150\mu s$	5.0.18
Repetitive short circuit current limit $T_j = T_{jTrip}$ ; see timing diagrams	$I_{LSCR}$		6		A	$V_{IN} = 5.0V$ ; $V_S < 40V$	5.0.19
Repetitive short circuit current limit $T_j = T_{jTrip}$ ; see timing diagrams	$I_{LSCR}$		4.5		A	$V_{IN} = 5.0V$ ; $V_S > 40V$	5.0.20
Output clamp at $V_{OUT} = V_S - V_{DSCCL}$ (inductive load switch off)	$V_{DSCCL}$	59	63		V	$I_S = 4mA$	5.0.22
Oversvoltage protection $V_{OUT} = V_S - V_{ONCL}$	$V_{SAZ}$	62			V	$I_S = 4mA$	5.0.23
Thermal overload trip temperature	$T_{jTrip}$	150			$^\circ C$		5.0.24
Thermal hysteresis	$T_{HYS}$		10		K		5.0.25
<b>Reverse Battery<sup>5)</sup></b>							
Continuous reverse battery voltage	$V_{SREV}$			52	V		5.0.26
Forward voltage of the drain-source reverse diode	$V_{FDS}$		600		mV	$I_{FDS} = 200mA$ ; $V_{IN} = 0V$ ; $T_j = 125^\circ C$	5.0.27
<b>Input interface; pin IN</b>							
Input turn-ON threshold voltage	$V_{INON}$	2.2			V		5.0.28
Input turn-OFF threshold voltage	$V_{INOFF}$			0.8	V		5.0.29
Input threshold hysteresis	$V_{INHYS}$		0.4		V		5.0.30
Off state input current	$I_{INOFF}$	1		25	$\mu A$	$V_{IN} = 0.7V$	5.0.31
On state input current	$I_{INON}$	3		25	$\mu A$	$V_{IN} = 5.0V$	5.0.32
Input resistance	$R_{IN}$	2.0	3.5	5.0	k $\Omega$		5.0.33
<b>Status output (NMOS open drain); pin ST</b>							
Status output zener voltage	$V_{STZ}$	5.4	6.1	6.8	V	$I_{ST} = 1.6mA$	5.0.34
Status output low voltage	$V_{STLO}$			0.4	V	$I_{ST} = 1.6mA$ ; $T_j < 25^\circ C$	5.0.35
Status output low voltage	$V_{STLO}$			0.6	V	$I_{ST} = 1.6mA$ ; $T_j < 125^\circ C$	5.0.36
Status leakage current	$I_{STLK}$			2	$\mu A$	$V_{ST} = 5V$ ; $T_j < 105^\circ C$	5.0.37
Status invalid time after positive input slope <sup>6)7)</sup>	$t_{dP}$		120	160	$\mu s$	$V_S = 13.5V$	5.0.38
Status invalid time after negative input slope <sup>8)9)</sup>	$t_{dN}$		250	400	$\mu s$	$V_S = 13.5V$	5.0.39
<b>Diagnostic characteristics</b>							
Short circuit detection voltage	$V_{OUTSC}$		2.8		V		5.0.40
Open load detection voltage <sup>10)</sup>	$V_{OUTOL}$		3	4	V		5.0.41
Internal pull down resistor <sup>11)</sup>	$R_{OUTPD}$		200		k $\Omega$	$V_{OUT} = 4V$	5.0.42

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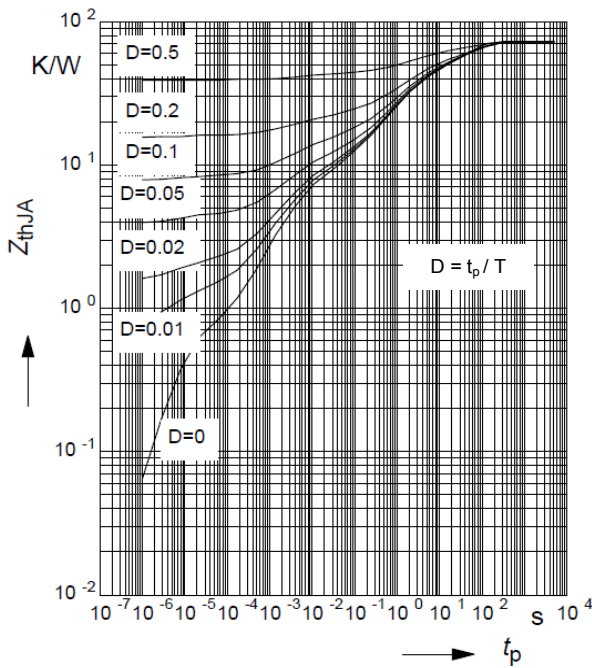
**Electrical Characteristics**

- 1) Device on 50mm x 50mm x 1,5mm epoxy FR4 PCB with 6cm<sup>2</sup> (one layer copper 70um thick) copper area for supply voltage connection. PCB in vertical position without blown air.
- 2) Timing values only with high slewrate input signal; otherwise slower.
- 3) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.
- 4) No subject to production test; specified by design.
- 5) Requires a 150W resistor in GND connection. The reverse load current trough the intrinsic drain-source diode of the power-MOS has to be limited by the connected load. Power dissipation is higher compared to normal operation due to the votage drop across the drain-source diode. The temperature protection is not functional during reverse current operation! Input current has to be limited (see max ratings).
- 6) No delay time after overtemparature switch off and short circuit in on-state.
- 7) No subject to production test; specified by design.
- 8) No delay time after overtemparature switch off and short circuit in on-state.
- 9) No subject to production test; specified by design.
- 10) External pull up resistor required for open load detection in off state.
- 11) No subject to production test; specified by design.

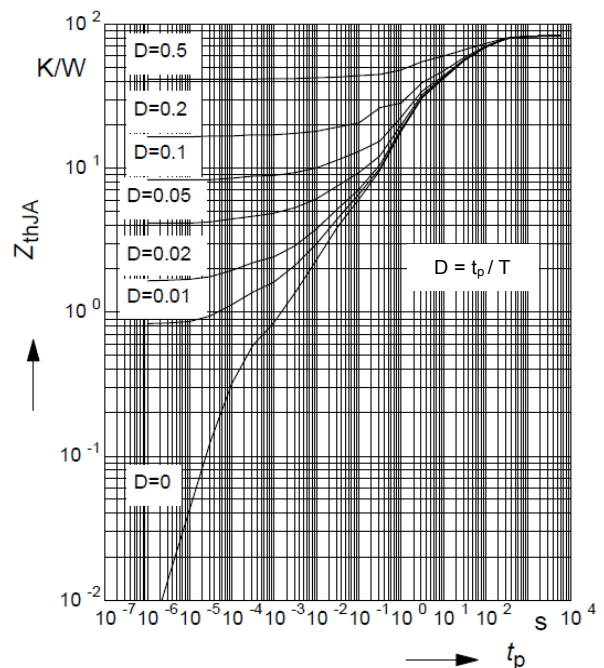
## 6 Typical Performance Graphs

### Typical Characteristics

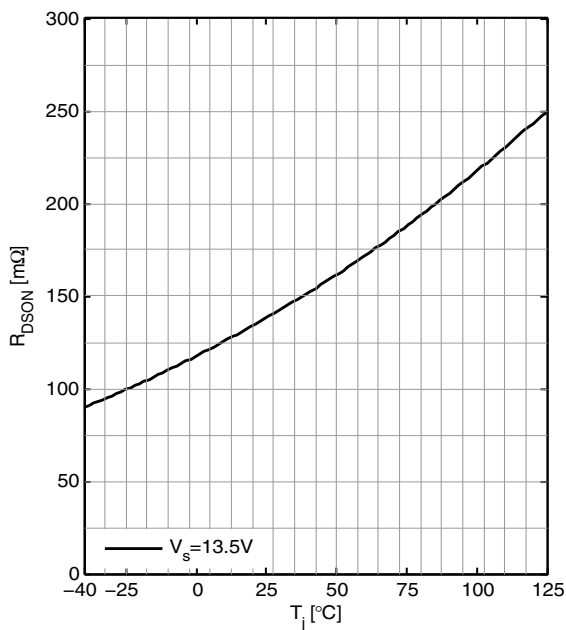
Transient Thermal Impedance  $Z_{thJA}$  versus Pulse Time  $t_p$  @ 6cm<sup>2</sup> heatsink area



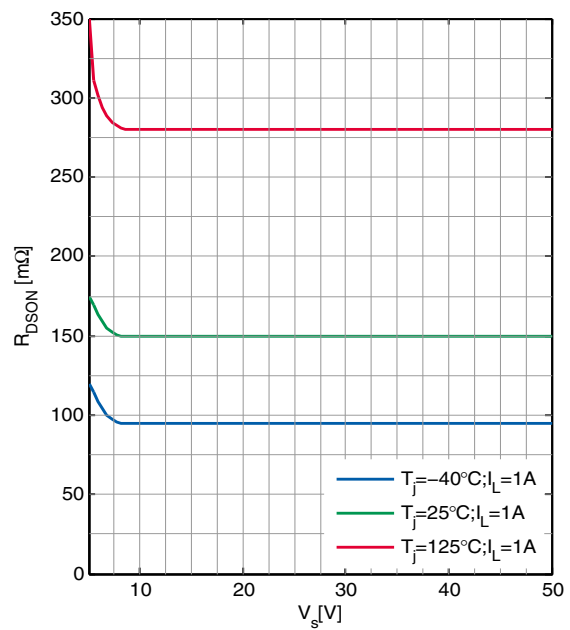
Transient Thermal Impedance  $Z_{thJA}$  versus Pulse Time  $t_p$  @ min footprint



On-Resistance  $R_{DS(on)}$  versus Junction Temperature  $T_j$

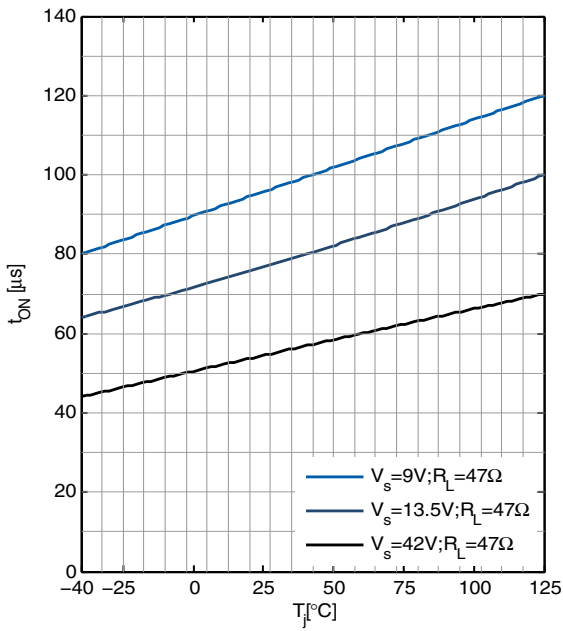


On-Resistance  $R_{DS(on)}$  versus Supply Voltage  $V_s$

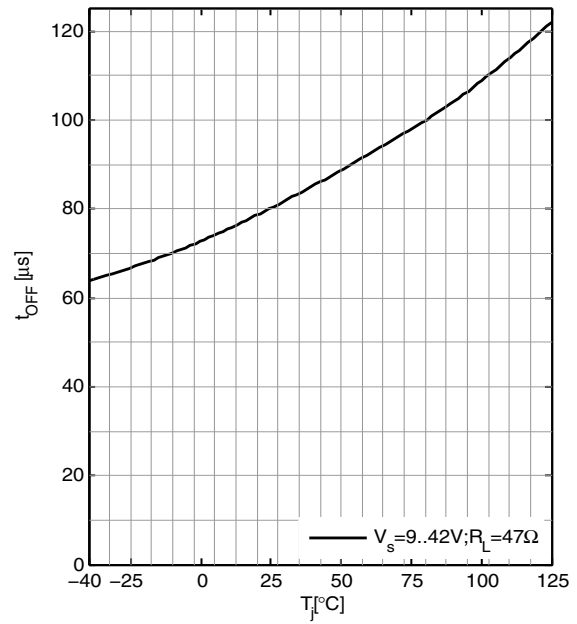


Typical Characteristics

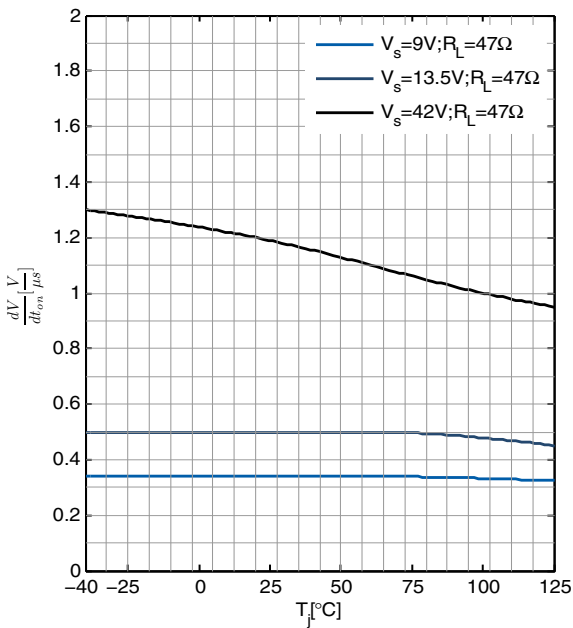
Switch ON Time  $t_{ON}$  versus Junction Temperature  $T_j$



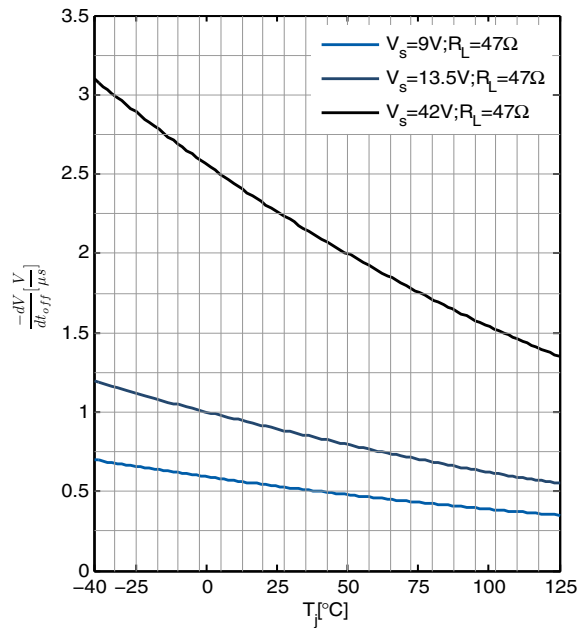
Switch OFF Time  $t_{OFF}$  versus Junction Temperature  $T_j$



ON Slewrate  $SR_{ON}$  versus Junction Temperature  $T_j$



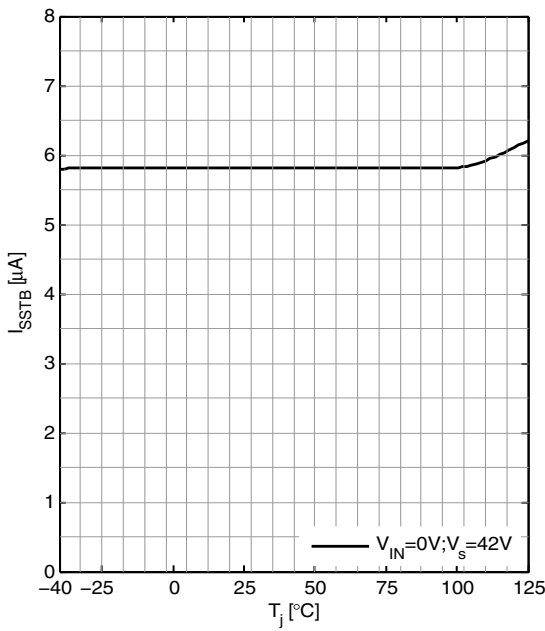
OFF Slewrate  $SR_{OFF}$  versus Junction Temperature  $T_j$



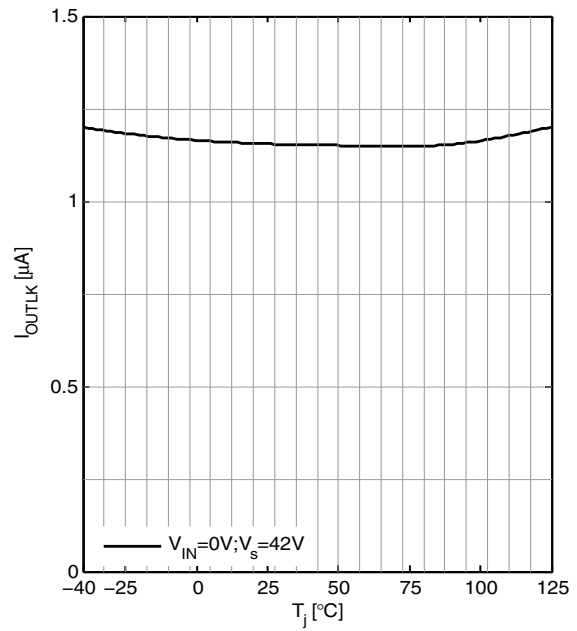


Typical Characteristics

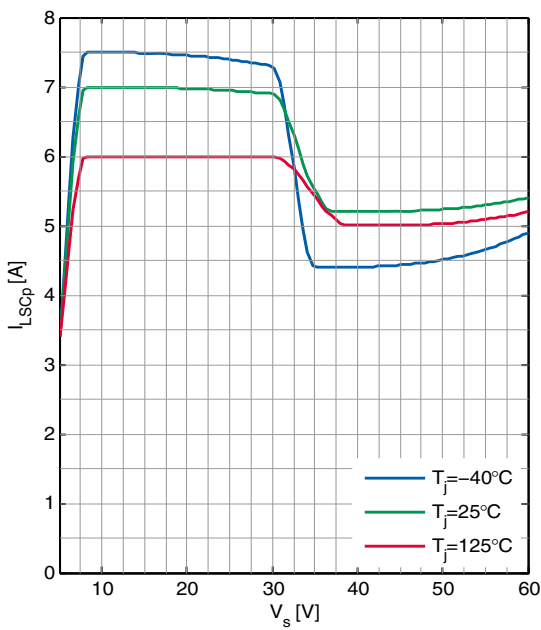
Standby Current  $I_{SSTB}$  versus Junction Temperature  $T_j$



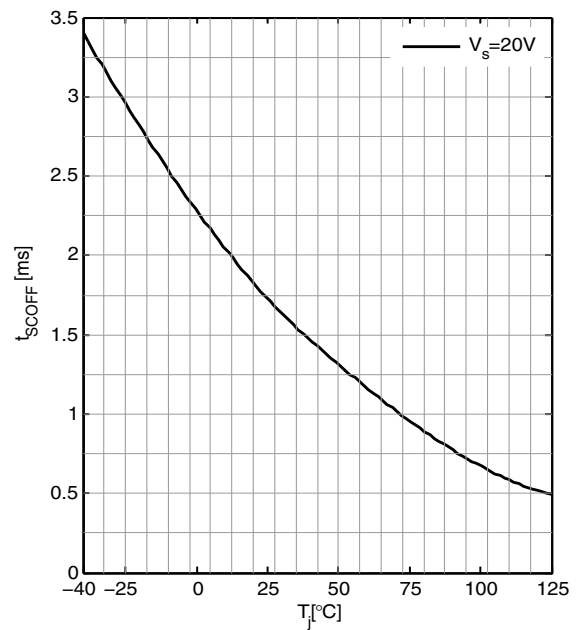
Output Leakage current  $I_{OUTLK}$  versus Junction Temperature  $T_j$



Initial Peak Short Circuit Current Limit  $I_{LSCP}$  versus Junction Temperature  $T_j$

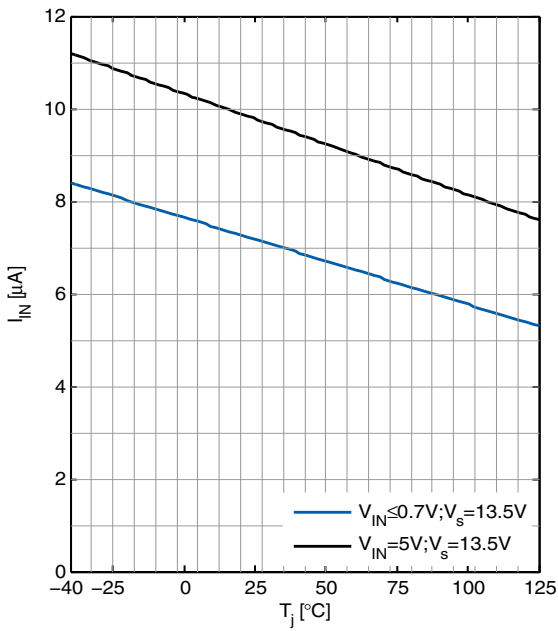


Initial Short Circuit Shutdown time  $t_{SCOFF}$  versus Junction Temperature  $T_j$

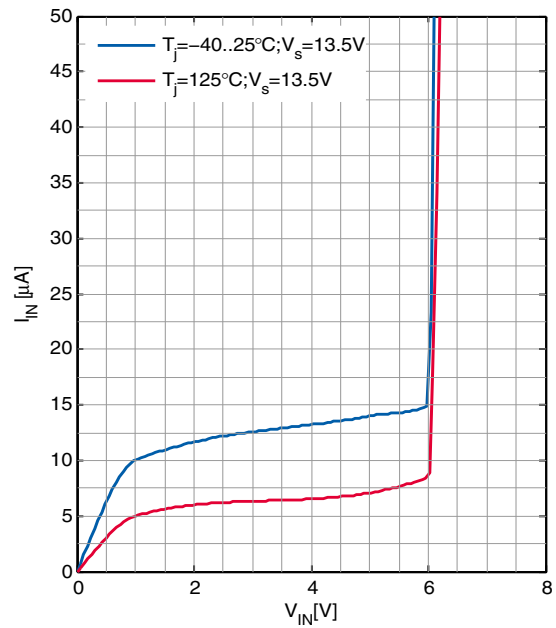


Typical Characteristics

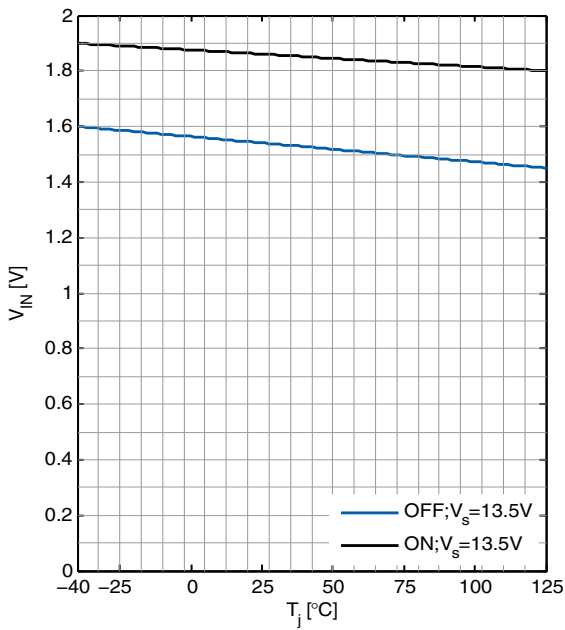
Input Current Consumption  $I_{IN}$  versus Junction Temperature  $T_j$



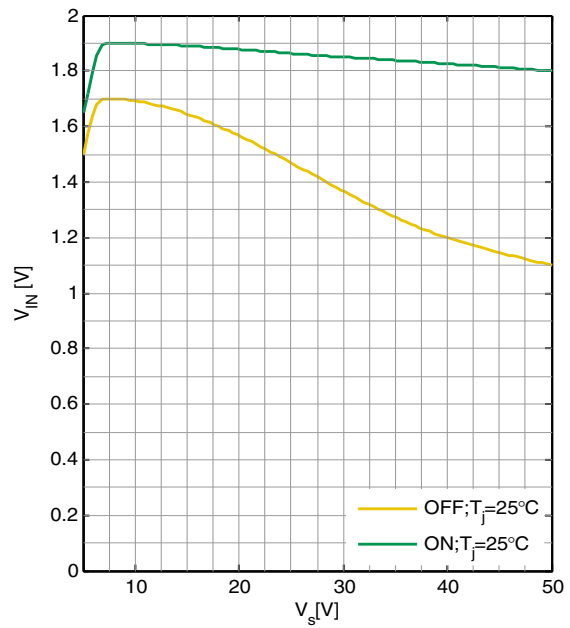
Input Current Consumption  $I_{IN}$  versus Input voltage  $V_{IN}$



Input Threshold voltage  $V_{IN,H,L}$  versus Junction Temperature  $T_j$

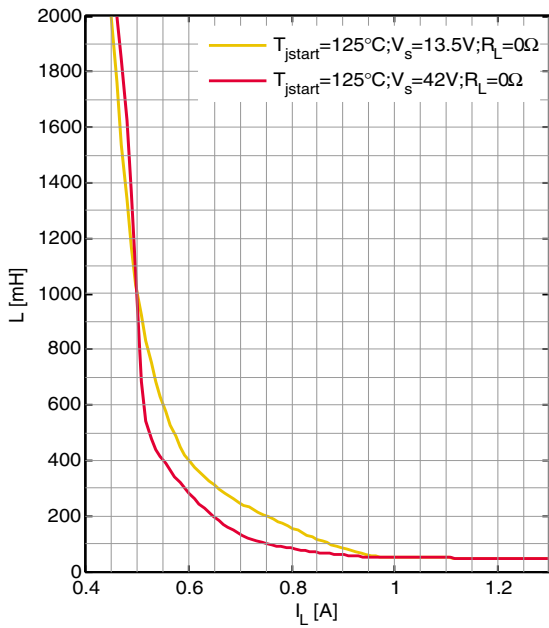


Input Threshold voltage  $V_{IN,H,L}$  versus Supply Voltage  $V_S$

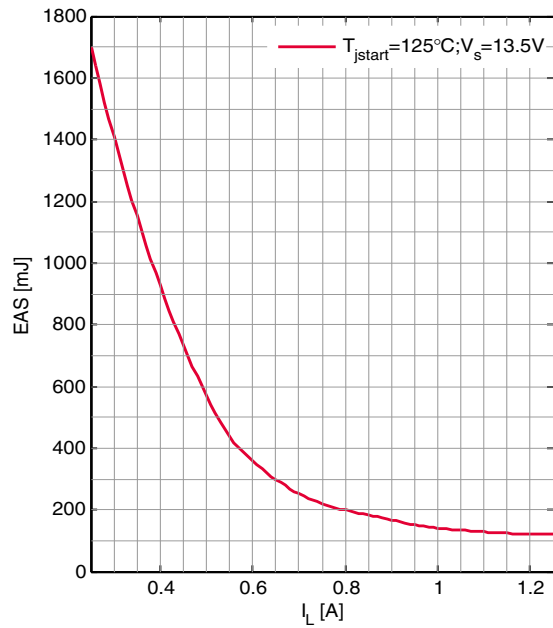


Typical Characteristics

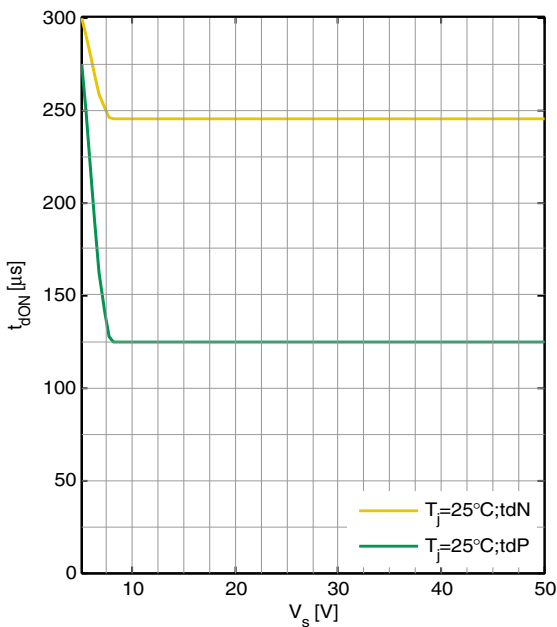
Max. allowable Load Inductance  $L$  versus Load current  $I_L$



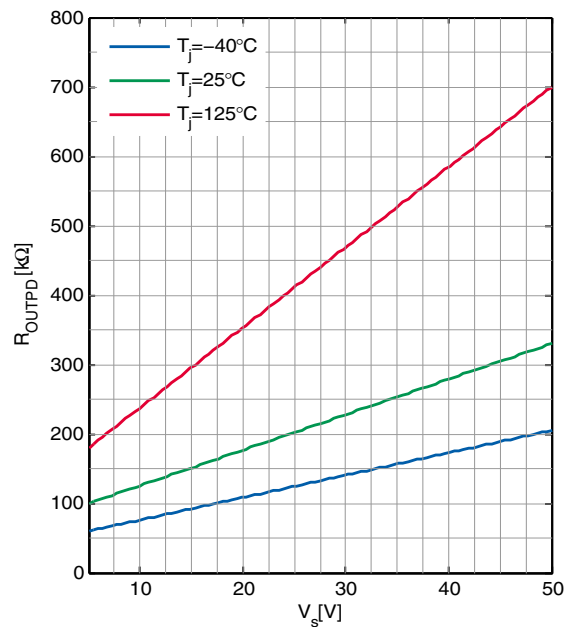
Max. allowable Inductive single pulse Switch-off Energy  $E_{AS}$  versus Load current  $I_L$



Status Delay Time  $t_{N,P}$  versus Supply Voltage  $V_S$



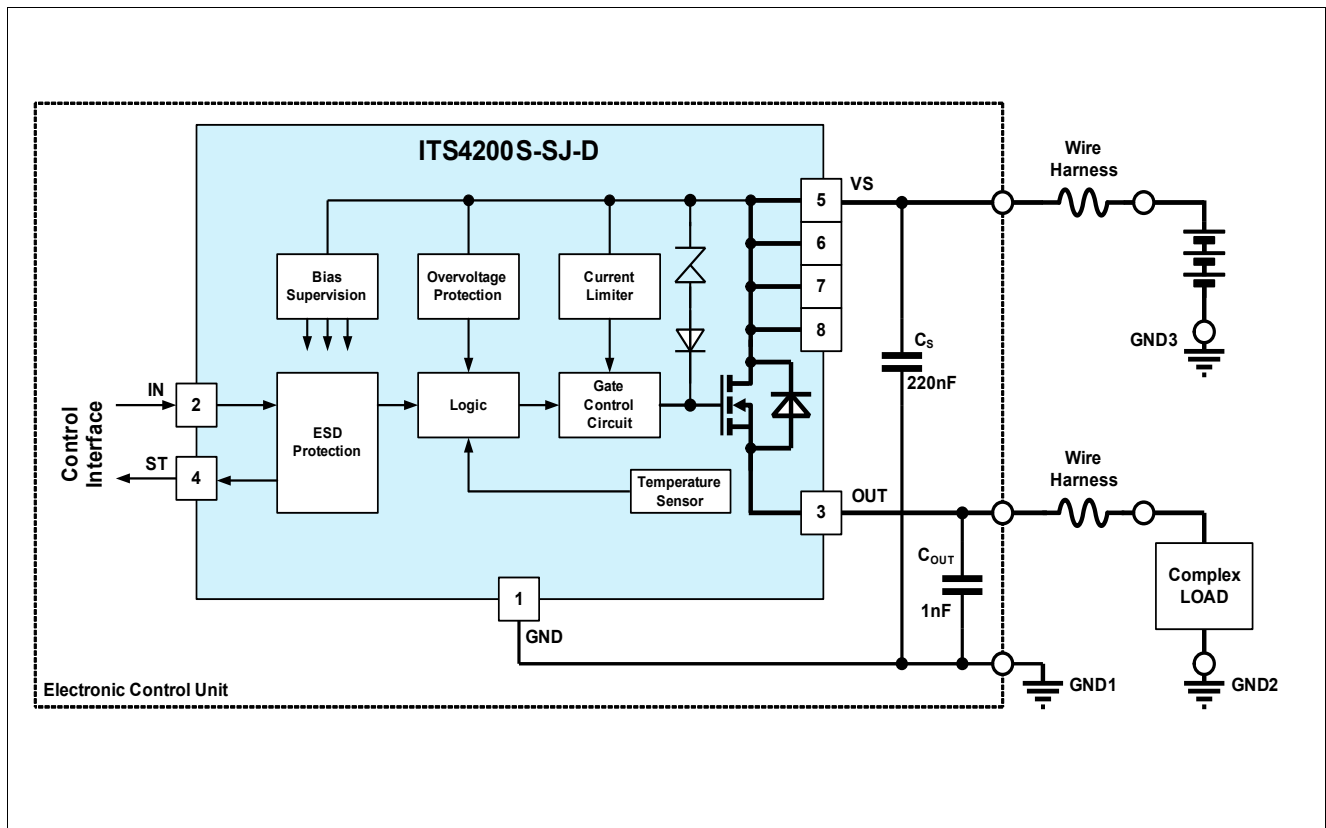
Internal Output pull down Resistor  $R_{OUTOPD}$  versus Supply Voltage  $V_S$



## 7 Application Information

### 7.1 Application Diagram

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty for a certain functionality, condition or quality of the device.



**Figure 4 Application Diagram**

The ITS4200S-SJ-D can be connected directly to the battery of a supply network. It is recommended to place a ceramic capacitor (e.g.  $C_S = 220\text{nF}$ ) between supply and GND of the ECU to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The ITS4200S-SJ-D can be switched on and off with standard logic ground related logic signal at pin IN.

In standby mode (IN=L) the ITS4200S-SJ-D is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transition to minimize emissions. Only a small ceramic capacitor  $C_{OUT}=1\text{nF}$  is recommended to attenuate RF noise.

In the following chapters the main features, some typical waveforms and the protection behaviour of the ITS4200S-SJ-D is shown. For further details please refer to application notes on the Infineon homepage.



## 7.2 Diagnosis Description

For diagnostic purpose the device provides a digital output pin ST in order to indicate fault conditions.

The status output (ST) of the ITS4200S-SJ-D is a high voltage open drain output.

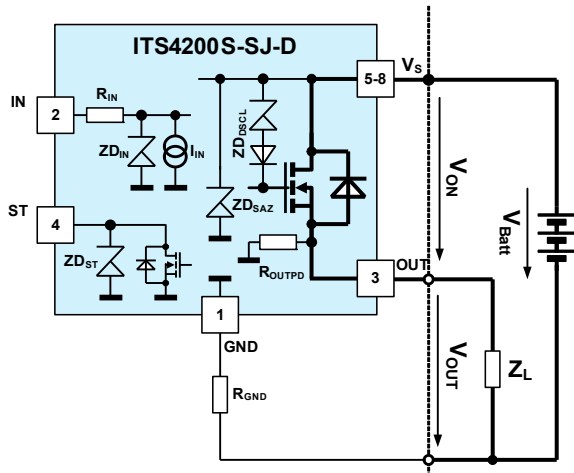
In “normal” operation mode the NMOS open drain transistor is switched OFF.

The following truth table defines the status output.

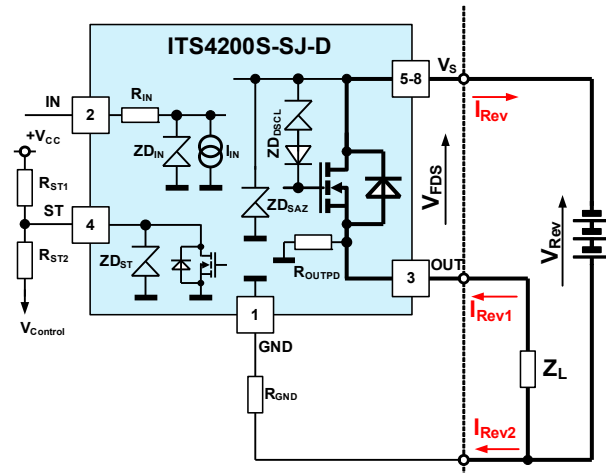
**Table 5 Truth Table of diagnosis feature**

Device Operation	IN	OUT	ST	Comment
Normal Operation	L	L	H	
Normal Operation	H	H	H	
Short circuit to GND	L	L	H	
Short circuit to GND	H	L	L	OUT=L: $V_{OUT} < V_{OUTSC}$ ; Short circuit detection voltage; typ 2.8V
Short Circuit to $V_S$ (in OFF state)	L	H	L	
Short Circuit to $V_S$ (in OFF state)	H	H	H	
Overload	L	L	H	
Overload	H	H	H	OUT=H: $V_{OUT} > V_{OUTSC}$ ; Short circuit detection voltage; typ 2.8V
Overtemperature	L	L	H	
Overtemperature	H	L	L	
Open Load in OFF state	L	Z	H	OUT=Z: high impedance; potential depends on external circuit
Open Load in OFF state	L	H	L	with external resistor between $V_S$ and OUT

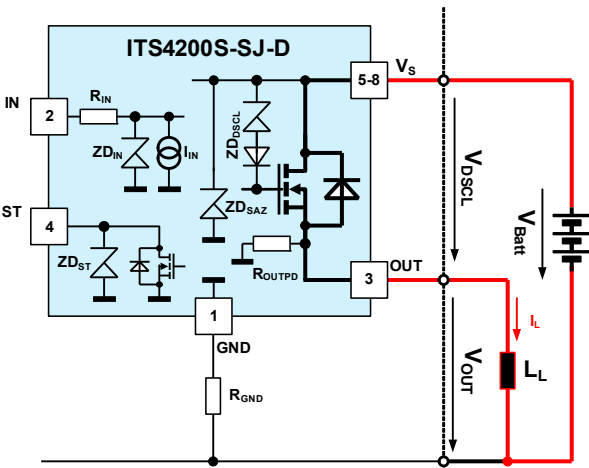
## 7.3 Special Feature Description

**Supply over voltage:**


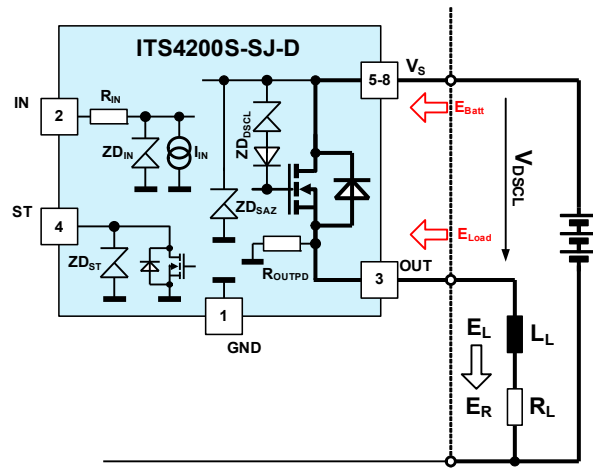
If over-voltage is applied to the  $V_S$ -Pin:  
 Voltage is limited to  $V_{ZD_{SAZ}}$ ; current can be calculated:  
 $I_{ZD_{SAZ}} = (V_S - V_{ZD_{SAZ}}) / R_{GND}$   
 A typical value for  $R_{GND}$  is 150 $\Omega$ .  
 In case of ESD pulse on the input pin there is in both polarities a peak current  $I_{IN_{peak}} \sim V_{ESD} / R_{IN}$

**Supply reverse voltage:**


If reverse voltage is applied to the device:  
 1.) Current via load resistance  $R_L$ :  
 $I_{Rev1} = (V_{Rev} - V_{FDS}) / R_L$   
 2.) Current via Input pin IN and diagnostic pin ST:  
 $I_{Rev2} = I_{ST} + I_{IN} \sim (V_{Rev} - V_{CC}) / R_{IN} + (V_{Rev} - V_{CC}) / R_{ST1,2}$   
 Current  $I_{ST}$  must be limited with the external series resistor  $R_{ST}$ . Both currents will sum up to:  
 $I_{Rev} = I_{Rev1} + I_{Rev2}$

**Drain-Source power stage clamper  $V_{DSCL}$ :**


When an inductive load is switched off a current path must be established until the current is sloped down to zero (all energy removed from the inductive load). For that purpose the series combination  $Z_{DSCL}$  is connected between Gate and Drain of the power DMOS acting as an active clamp.  
 When the device is switched off, the voltage at OUT turns negative until  $V_{DSCL}$  is reached.  
 The voltage on the inductive load is the difference between  $V_{DSCL}$  and  $V_S$ .

**Energy calculation:**


Energy stored in the load inductance is given by:  
 $E_L = I_L^2 * L / 2$   
 While demagnetizing the load inductance the energy dissipated by the Power-DMOS is:  
 $E_{AS} = E_S + E_L - E_R$   
 With an approximate solution for  $R_L = 0\Omega$ :  
 $E_{AS} = \frac{1}{2} * L * I_L^2 * \{(1 - V_S / (V_S - V_{DSCL}))\}$

**Figure 5 Special feature description**

## 7.4 Typical Application Waveforms

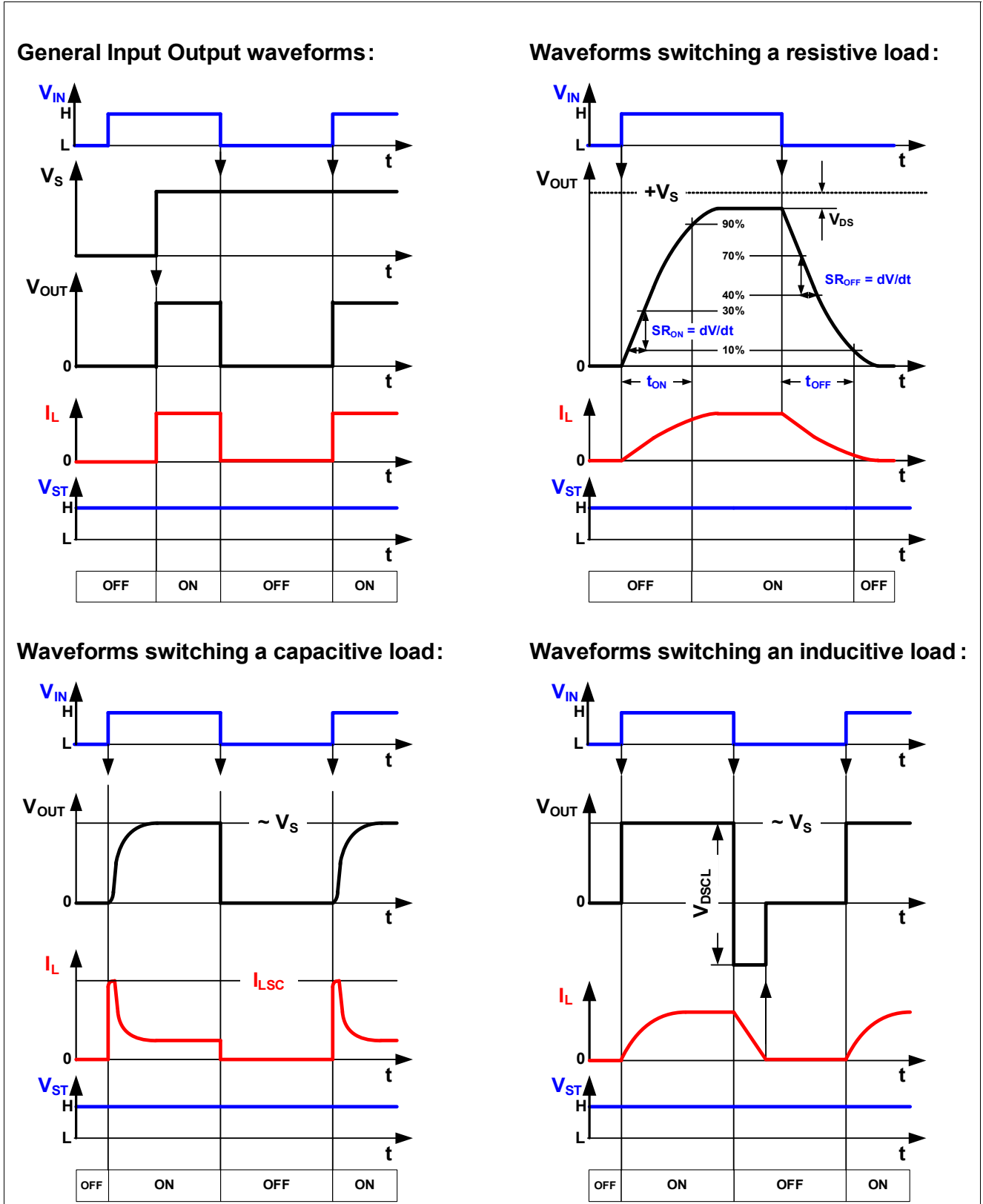


Figure 6 Typical application waveforms of the ITS4200S-SJ-D

## 7.5 Protection Behavior

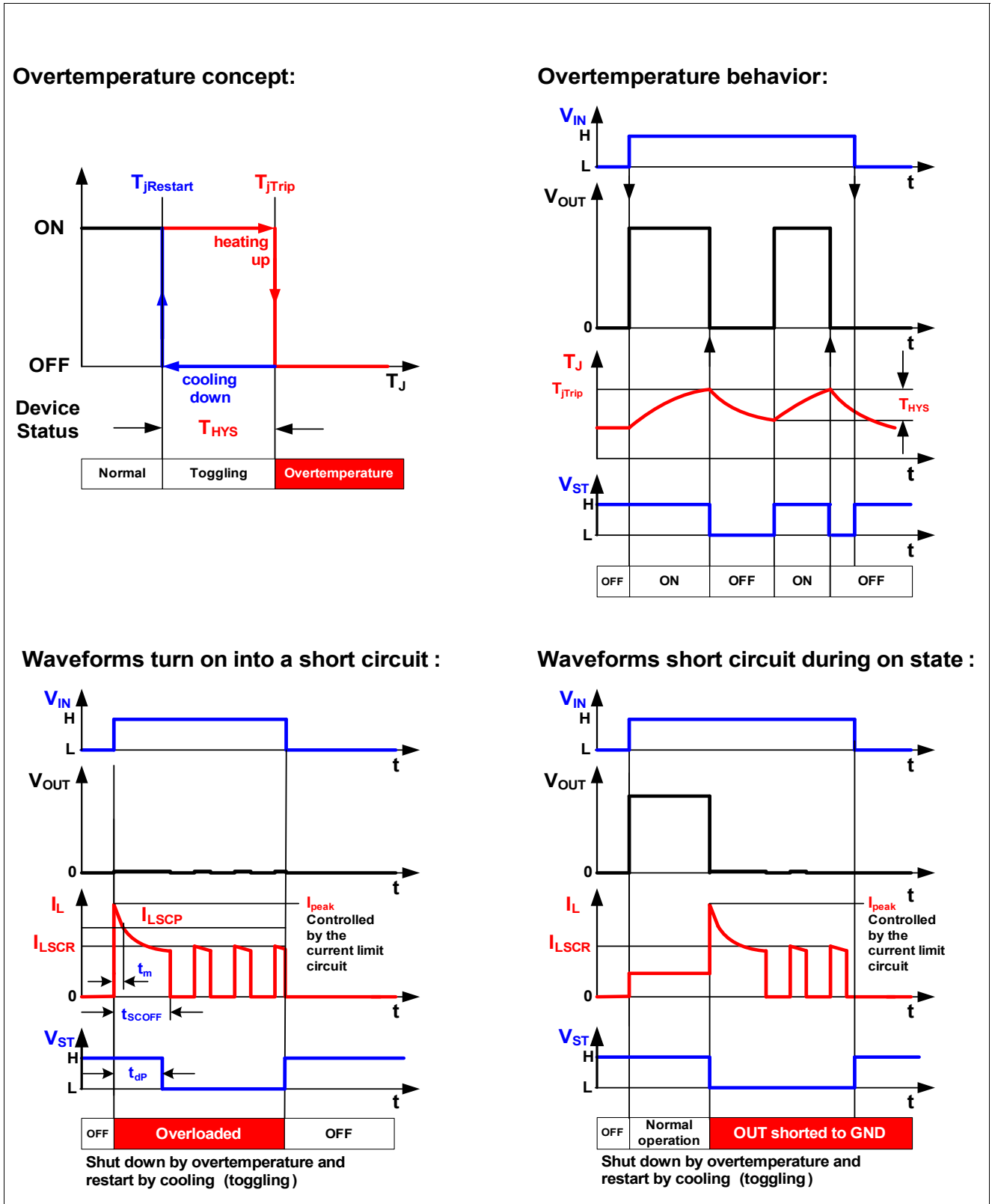
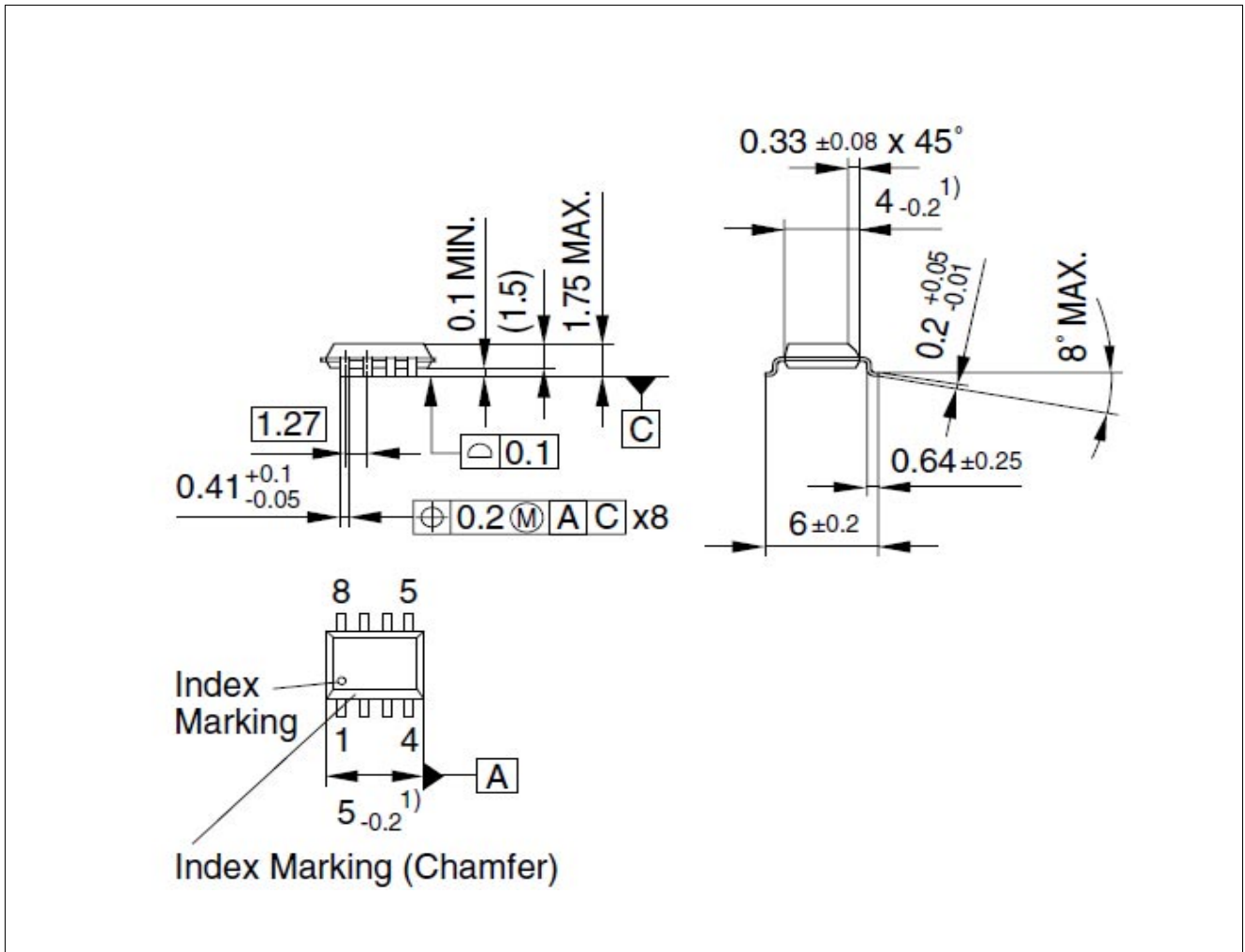


Figure 7 Protective behaviour of the ITS4200S-SJ-D



## 8 Package outlines and footprint



**Figure 8** PG-DSO-8 (Plastic Dual Small Outline Package, RoHS-Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020

## 9 Revision History

Revision	Date	Changes
V 1.0	12-09-01	Datasheet release

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Last Trademarks Update 2011-11-11

**Edition 2012-09-01**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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