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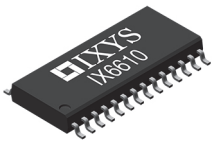
IX6610

Transformer Coupled Driver Logic Interface



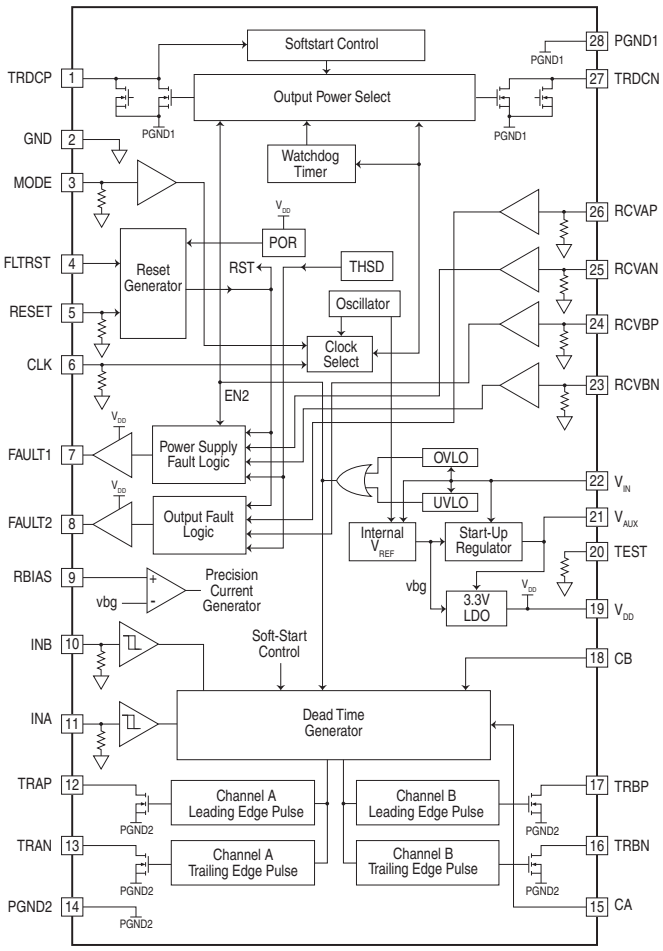
Features

- TTL Logic level micro-controller Interface
- Pulse transformer bidirectional data interface
- Short input pulse suppression
- Interlock and dead time control
- Four 1A pulse transformer drivers
- Two 1A drivers for push-pull power converter for the secondary side power supply
- Non-overlap operation of high side and low side drivers
- Internal startup oscillator
- Primary side fault monitoring
- Secondary side fault monitoring
- Two fault status outputs
- 2mA quiescent current (non- switching)

Applications

- Pulse transformer coupled IGBT/MOSFET gate driver interface

IX6610 Block Diagram



Description

The IX6610 is a primary side logic interface device that implements a dual channel bidirectional transformer interface to drive a secondary side intelligent IGBT driver. The bidirectional transformer interface transmits the primary side input commands, secondary side output faults, and power supply faults. Asynchronous data transmission is through high frequency narrow pulses to avoid duty cycle restrictions, to achieve shorter delays, and to prevent any transformer core saturation issues. The IX6610 contains all the necessary blocks to implement a power converter that supplies isolated power to the secondary side IGBT drivers. IX6610 is a primary side device with built-in interlock and dead time control that can be interfaced directly to a low voltage microcontroller to provide input signal conditioning as well as fault management.

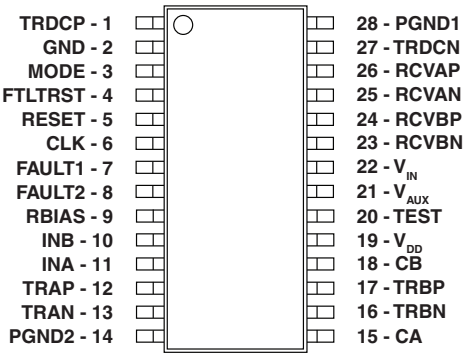
The IX6610 operates over a temperature range of -40°C to +85°C. The IX6610 is available in either 28-lead TSSOP with exposed pad or as tested die.

Ordering Information

Part	Description
IX6610T	28-Pin TSSOP, in Tubes, Exposed Tab (50/Tube)
IX6610TR	28-Pin TSSOP, Exposed Pad, Tape & Reel (1000/Reel)
IX6610	Tested Die

1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Description
1	TRDCP	Power converter transformer primary positive terminal
2	GND	Ground terminal; analog ground
3	MODE	Enable external MCU V_{DD} supply feature
4	FLT RST	Fault reset input terminal
5	RESET	Global reset input terminal
6	CLK	External clock input terminal
7	FAULT1	Primary and secondary side power supply status terminal
8	FAULT2	Secondary side IGBT output status terminal
9	RBIAS	Bias current setting resistor terminal
10	INB	Channel B TTL level logic input terminal
11	INA	Channel A TTL level logic input terminal
12	TRAP	Channel A transmit signal pulse transformer primary positive terminal
13	TRAN	Channel A transmit signal pulse transformer primary negative terminal
14	PGND2	Ground terminal; transmit signal transformer switch ground
15	CA	Channel A dead time capacitor terminal
16	TRBN	Channel B transmit signal pulse transformer primary negative terminal
17	TRBP	Channel B transmit signal pulse transformer primary positive terminal
18	CB	Channel B dead time capacitor terminal
19	V_{DD}	3.3V LDO regulator output terminal
20	TEST	Test configuration terminal
21	V_{AUX}	Auxiliary bootstrap supply winding terminal
22	V_{IN}	Positive power supply input terminal
23	RCVBN	Channel B receive signal pulse transformer secondary negative terminal
24	RCVBP	Channel B receive signal pulse transformer secondary positive terminal
25	RCVAN	Channel A receive signal pulse transformer secondary negative terminal
26	RCVAP	Channel A receive signal pulse transformer secondary positive terminal
27	TRDCN	Power converter transformer primary negative terminal
28	PGND1	Ground terminal. power converter transformer switch ground

1.3 Absolute Maximum Ratings @ 25°C

Parameter	Symbol	Limits	Units
Supply voltage	V_{IN}	-0.3 to 18	V
Auxiliary winding voltage	V_{AUX}	-0.3 to 6	V
LDO terminal voltage	V_{DD}	-0.3 to 6	V
Logic input voltages	INA, INB, RESET, CLK, FLTRST, TEST, MODE	-0.3 to V_{DD}+0.3	V
Analog I/O terminal voltages	CA, CB	-0.3 to V_{DD}+0.3	V
Fault output terminal voltages	FAULT1, FAULT2	-0.3 to V_{DD}+0.3	V
Pulse Transformer receive input terminal voltages	RCVAP, RCVAN, RCVBP, RCVBN	-0.3 to V_{DD}+0.3	V
Pulse transformer driver output terminal voltages	TRAP, TRAN, TRBP, TRBN	-0.3 to V_{IN}+0.3	V
Power converter transformer driver output terminal voltage	TRDCP, TRDCN	-0.3 to ($2V_{IN}$+4)	V
Operating junction temperature range	T_J	-55 to +150	°C
Storage temperature range	T_{STG}	-65 to +150	°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

1.4 ESD Warning

ESD (electrostatic discharge) sensitive device. Electrostatic charges can readily accumulate on test equipment and the human body in excess of 4000V. This energy can discharge without detection. Although the IX6610 features proprietary ESD protection circuitry, permanent damage may be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

1.5 Electrical Characteristics

T_A=-40°C to +85°C unless otherwise noted.

1.5.1 Input Power Supply

Logic and the output switches are conditioned to be in the appropriate logic state during the supply ramp-up. The minimum V_{IN} required for a stable logic state: V_{IN_MIN} = 3V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Normal operating power supply voltage range	V_{IN}	Nominal operating range	14	15	15.5	V
Power supply Current 1	I_{IN_TST}	Test mode, V_{IN}=15V, power converter transformer disconnected, internal oscillator, no external load on LDO	-	1	3	mA
Power supply Current 2	I_{IN_NORMAL}	Normal mode, V_{IN}=15V, f_{CLK} = 200kHz	-	Note 1	-	mA

Note 1: Power supply current will depend on Secondary side power load, as well as transmit clock frequency and R_{LOAD} when Pulse transformers are sourced from V_{DD} .

1.5.2 Thermal Characteristics

Parameter	Rating	Units
Θ_{JA}	25	°C/W
Θ_{JC}	8	°C/W

1.5.3 Auxiliary Winding Bootstrap Supply (V_{AUX})

The LDO pass device shuts off once the V_{TH_AUX} voltage has been exceeded. The V_{AUX} voltage pin can operate up to ~(V_{IN} -2V). The V_{AUX} pin is only used to supply power to the V_{DD} regulator pass device.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Auxiliary winding voltage	V_{AUX}	V_{IN} = 14V to 15V, power converter duty cycle D= 35% to 50%	4	5	6 (Note 1)	V
V_{CC} switch over threshold	V_{TH_AUX}	Transfer the V_{CC} regulator load current from V_{IN} to V_{AUX}	-	4	-	V

Note 1: V_{AUX} can safely go higher than 6V but V_{AUX} cannot exceed the V_{IN} supply voltage.

1.5.4 Start Up Regulator (V_{CC})

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Regulator output voltage	V_{CC}	V_{IN}=14V to 16V	3.9	4.1	4.3	V
Input line regulation	ΔV_{CC_VIN}	V_{IN}=8V to 16V	-	-	0.5	V
Output load regulation	ΔV_{CC_IL}	V_{IN}=15V, I_{VCC}=1mA to 20mA	-	-	0.5	V
Dropout voltage	V_{DROP}	V_{DROP}=(V_{IN}-V_{CC}), I_{VDD}=10mA	-	-	2	V
Short circuit output current	I_{CC_Short}	V_{IN}=15V	-	-	150	mA

1.5.5 LDO Regulator (V_{DD})

LDO is powered from the V_{AUX} pin (Either Startup Regulator or Auxiliary Winding Voltage V_{AUX}). LDO to supply the MCU startup current of 50mA for 100ms.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LDO output voltage	V_{DD}	V_{IN} = 15V, V_{AUX}=5V, C_{OUT}=22µF	3	3.3	3.6	V
Input line regulation	ΔV_{DD_VCC}	V_{AUX}=4V to 5.5V, I_{VDD}=1mA	-	-	50	mV
Output load regulation	ΔV_{DD_IL}	V_{IN}=15V, V_{AUX}=5V, I_{VDD}=1mA to 50mA	-	-	50	mV
Short circuit output current	I_{DD_Short}	V_{IN}=15V, V_{AUX}=5V	-	-	100	mA
Dropout voltage	V_{DROP}	V_{DROP}=V_{AUX}-V_{DD}, V_{IN}=15V, I_{VDD}=50mA	-	-	1	V
Output bypass capacitance ESR	C_{VDD_ESR}	C_{VDD}=22µF, 1mA ≤ I_{VDD} ≤ 50mA	0.3	-	-	Ω

1.5.6 Digital Input Terminals

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input leakage current	I_{INLKG}	CLK, RESET, INA, INB, TEST=GND	-1	-	1	µA
Input pull-down current (25kΩ)	I_{INPD}	CLK, RESET, INA, INB, TEST=V_{DD}	75	130	300	µA
Input leakage current	I_{FLTRST}	FLTRST=GND or V_{DD}	-1	-	1	µA
Minimum high level input voltage	V_{IH}	INA, INB, RESET, FLTRST, CLK, TEST	2	-	-	V
Maximum low level input voltage	V_{IL}	INA, INB, RESET, FLTRST, CLK, TEST	-	-	0.8	V

1.5.7 Internal Voltage Reference

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Internal voltage reference	$V_{REF\_INTERNAL}$	Measured @ RBIAS pin, V_{IN}=15V, V_{CC}=4.6V	1.21	1.26	1.31	V
Internal voltage reference tolerance	V_{REF_TOL}	-	-4	-	+4	V

1.5.8 Digital Input Interface and Dead Time Generator.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INA, INB frequency	f_{INA}, f_{INB}	-	0	-	250	kHz
INA, INB input pulse width	t_{PW_INA}, t_{PW_INB}	(Note 1)	500	-	-	ns
INA, INB dead time no cap	t_{INDEAD_NOCAP}	No capacitors at CA and CB pins	20	30	50	ns
INA,INB dead time programmable range	t_{INDEAD_RANGE}	CA=CB=0nF	200	-	(Note 2)	ns
Reset pulse width	t_{PW_RESET}	-	200	-	-	ns
Fault reset pulse width	t_{PW_FLTRST}	-	200	-	-	ns

Note 1: INA will override INB and t_{PW} is reduced by t_{INDEAD} when INA overlaps INB.

*Note 2: The formula for t_{INDEAD} is 2000*CA or 2000*CB (CA or CB is the capacitor value in Farads). Example $2000*200e^{-12}$ = 400nS. The maximum value of t_{INDEAD} is only limited by the application*

1.5.9 External Clock and Internal Oscillator

To protect power converter switches, the power converter shuts down if the external converter clock (CLK) is high for greater than t_{DOG_OSC} (40µs). The power converter will remain shut down until eight valid clocks are received.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
External clock	f_{CLK}	Input from MCU	180	200	220	kHz
External clock duty cycle	D_{CLK}	Input from MCU	10	-	50	%
External clock watchdog time out	t_{DOG_CLK}	Information parameter	-	40	-	µs
Internal oscillator frequency	f_{OSC}	Information parameter	-	200	-	kHz
Internal oscillator divider output frequency	f_{DC_OSC}	Measured at the power converter driver output	65	100	140	kHz

1.5.10 Thermal Shutdown Circuit

Specifications are characterized and guaranteed by design. All units are not production tested.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal shutdown rising threshold	t_{SHDN_RISE}	-	+130	+145	+160	°C
Thermal shutdown hysteresis	t_{SHDN_HYS}	-	-	20	-	°C

1.5.11 UVLO Circuit

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under voltage lockout threshold	$UVLO_{RISE}$	V_{IN} UVLO rising threshold is measured by monitoring state change at FAULT1 terminal.	10	11	12	V
Under voltage lockout hysteresis	$UVLO_{HYST}$	-	-	0.5	-	V

1.5.12 OVLO Circuit

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Over voltage lockout threshold	$OVLO_{RISE}$	V_{IN} OVLO rising threshold is measured by monitoring state change at FAULT1 and FAULT2 terminals.	16.25	17	17.75	V
Over voltage lockout hysteresis	$OVLO_{HYST}$	-	-	0.5	-	V

1.5.13 Power Converter Control Circuit

See **Figure 2** and **Figure 3** for reference.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Converter switching clock frequency	f_{DC_CLK}	Normal operation, external clock	90	100	110	kHz
Converter switching clock duty cycle	D_{DC_CLK}	Normal operation, external clock	35	40	50	%
Converter switching clock pulse width	t_{PW_CLK}	Normal operation, external clock	900	-	-	ns
Converter startup switching clock frequency	f_{DC_OSC}	Startup operation, internal oscillator + clock divider	80	100	150	kHz
Converter startup switching clock duty cycle	D_{DC_OSC}	Startup operation, internal oscillator + clock divider	-	47	-	%
Converter transformer primary driver switch output sink resistance	R_{OUT_DCN}	Normal operation. Measured at TRDCP and TRDCN terminals @ I_{SINK} = 400mA.	-	0.4 Note 2	0.7	Ω
Converter transformer primary driver switch output sink resistance	R_{OUT_DCS}	Startup operation. Measured at TRDCP and TRDCN terminals @ I_{SINK} = 200mA	-	2.5	5	Ω
Converter transformer primary driver switch output peak sink current	I_{PEAK}	-	-	-	1	A
Converter transformer primary driver switch max drain voltage limit	V_{DSMAX}	-	-	-	40	V
Converter transformer primary driver output fall time	t_{F_TRDCP} t_{F_TRDCN}	V_{IN}=15V, R_L=1kΩ, C_L=50pF	-	-	50	ns

Note 1: Power converter needs to deliver 2 Watts of power @20V to the secondary side IGBT drivers, ~ 0.275 watts power @5.5V to the LDO. If the V_{CC} (5V) regulator is also powered from V_{AUX} then the converter power delivery needs to increase to accommodate V_{CC} regulator.

Note 2: Package and board resistance must be minimized to achieve this R_{OUT_DCN} specification.

1.5.14 Signal Transformer Primary (Transmit) Switch and Pulse Generator

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Transmit signal transformer primary switch sink resistance	R_{OUTS}	V_{CC} / V_{IN} = 5V / 15V, Measured at terminals TRAP, TRAN, TRBP, TRBN@ V_{DD} = 3.3V, I_{SINK} = 100mA	-	0.5	1	Ω
Transmit signal transformer primary switch peak sink current	I_{PEAKS}	V_{CC} / V_{IN} = 5V / 15V, Measured at terminals TRAP, TRAN, TRBP, TRBN@ V_{DD} = 3.3V, 200ns Pulse	0.7	1	-	A
Transmit signal transformer primary switch low level output voltage	V_{OLS}	V_{CC} / V_{IN} = 5V / 15V, Measured at terminals TRAP, TRAN, TRBP, TRBN@ V_{DD} = 3.3V, R_L = 5Ω	-	0.3	1	V
Transmit signal transformer primary switch max drain voltage limit	V_{DSMAX}	@ I_{DS_LEAK} = 1μA	-	-	15	V
Leading edge pulse width related to the input signals INA, INB	T_{PWL}	Measured at terminals TRAP, TRBP @ V_{DD} = 3.3V, R_L = 1kΩ, C_L=50pF	100	200	300	ns
Trailing edge pulse width related to the input signals INA, INB	T_{PWT}	Measured at terminals TRAN, TRBN@ V_{DD} = 3.3V, R_L = 1kΩ, C_L=50pF	100	200	300	ns
Channel A vs Channel B pulse width distortion	T_{DST}	Measured at terminals TRAP, TRAN, TRBP, TRBN @ V_{DD} = 3.3V R_L = 1kΩ, C_L = 50pF	-	20	-	ns

1.5.15 Signal Transformer Secondary Receive Inputs and Fault Detect

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Receive input resistance	R_{IN}	Measured at terminals @ RCVAP, RCVAN, RCVBP, RCVBN	0.7	1	1.3	kΩ
Receive input positive threshold voltage	V_{THP}	Measured at terminals RCVAP, RCVAN, RCVBP, RCVBN by monitoring the state change at FAULT1 and FAULT2 terminals @ V_{DD} = 3.3V	2.2	-	-	V
Receive input hysteresis	V_{HYS}		0.5	1	-	
FAULT1, FAULT2 output high voltage	V_{OH_FLT1} V_{OH_FLT2}	V_{DD} = 3.3V, I_{SOURCE} = 10mA	V_{DD}-0.2	-	-	V
FAULT1, FAULT2 output low voltage	V_{OL_FLT1} V_{OL_FLT2}	V_{DD} = 3.3V, I_{SOURCE} = 10mA	-	-	0.2	V
FAULT1, FAULT2 signal propagation delay	t_{FD}	V_{DD} = 3.3V, Measured from RCVAP, RCVBP to FAULT2 and from RCVAN, RCVBN to FAULT1	-	-	50	ns

1.6 Timing Diagrams

Figure 1 Input Signal Timing

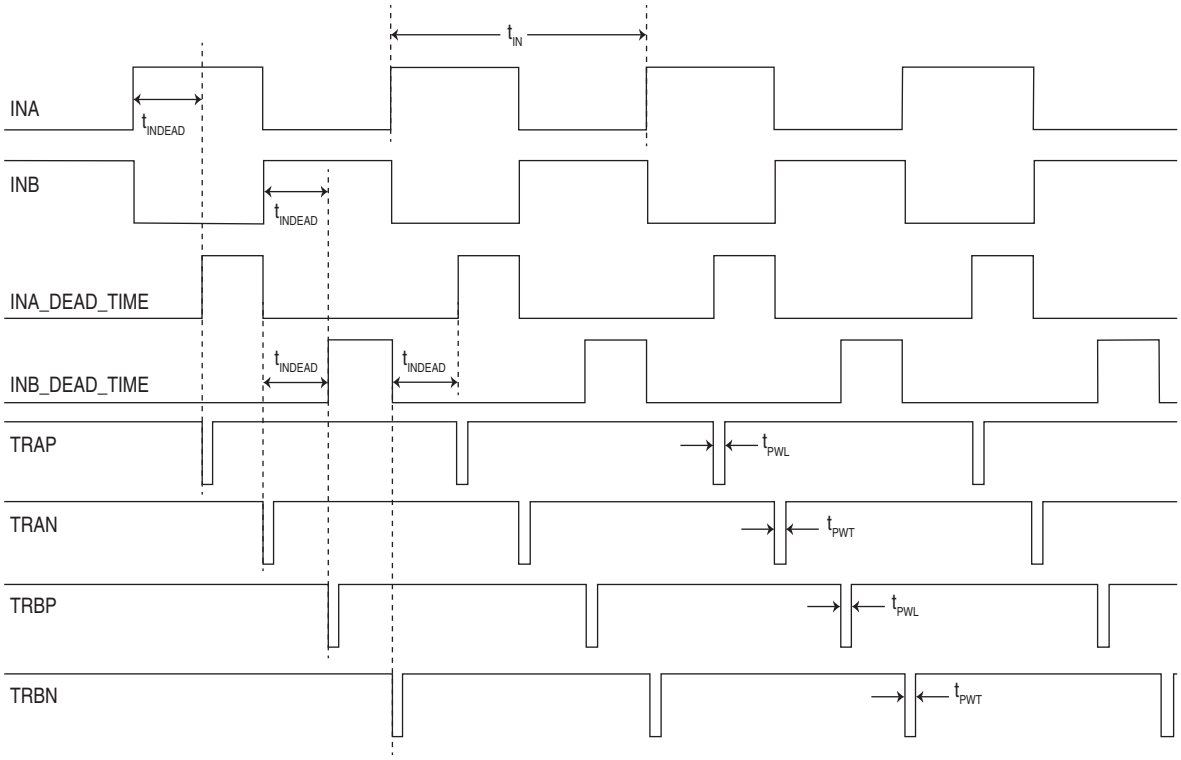


Figure 2 Power Converter Timing (Internal Oscillator)

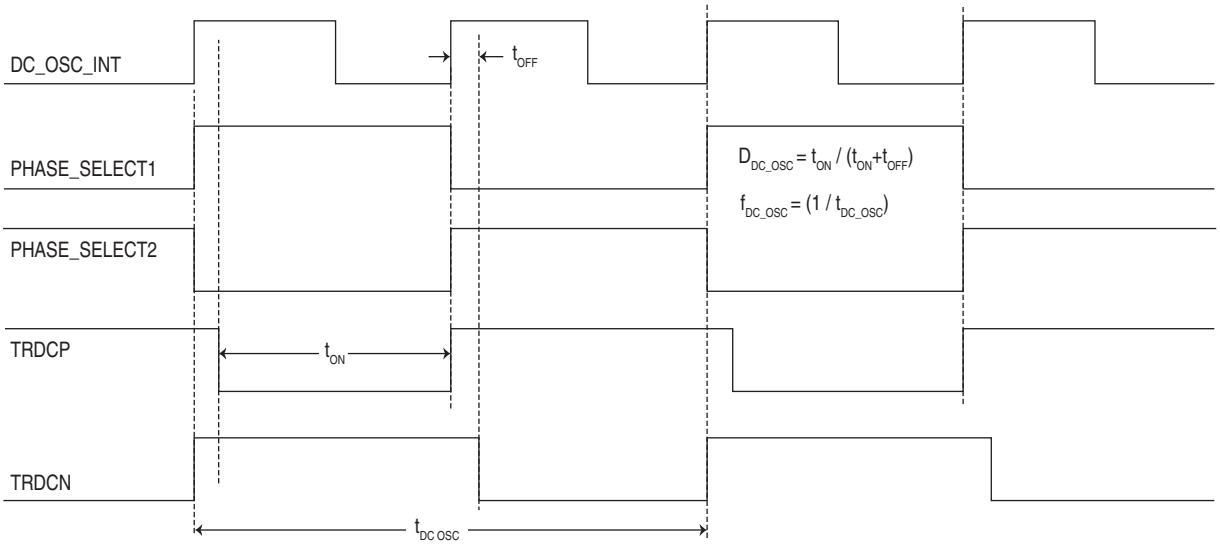


Figure 3 Power Converter Timing (External Clock)

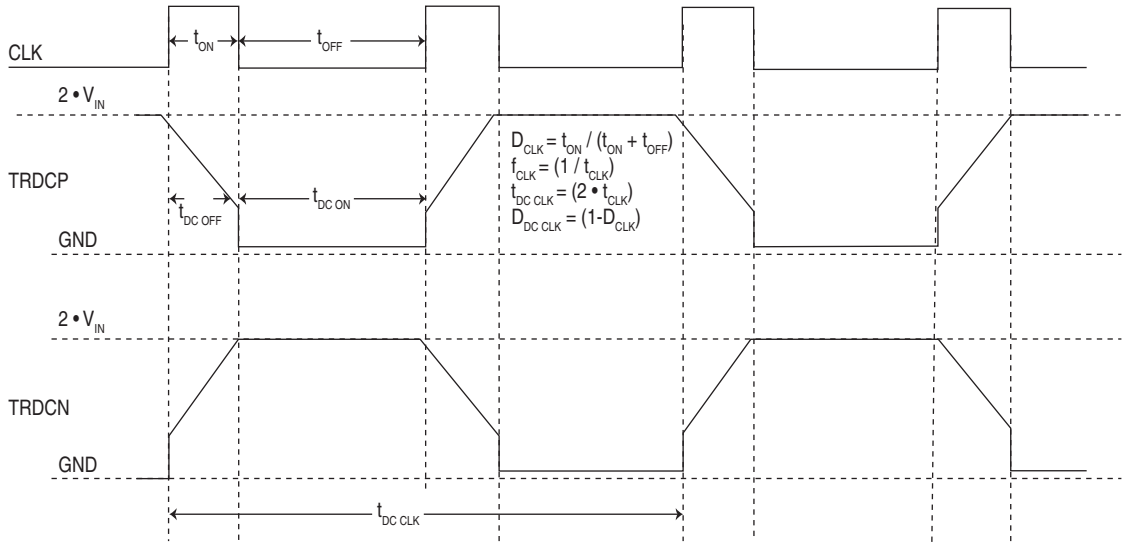


Figure 4 Input Signal Interlock Timing (A Channel has Priority)

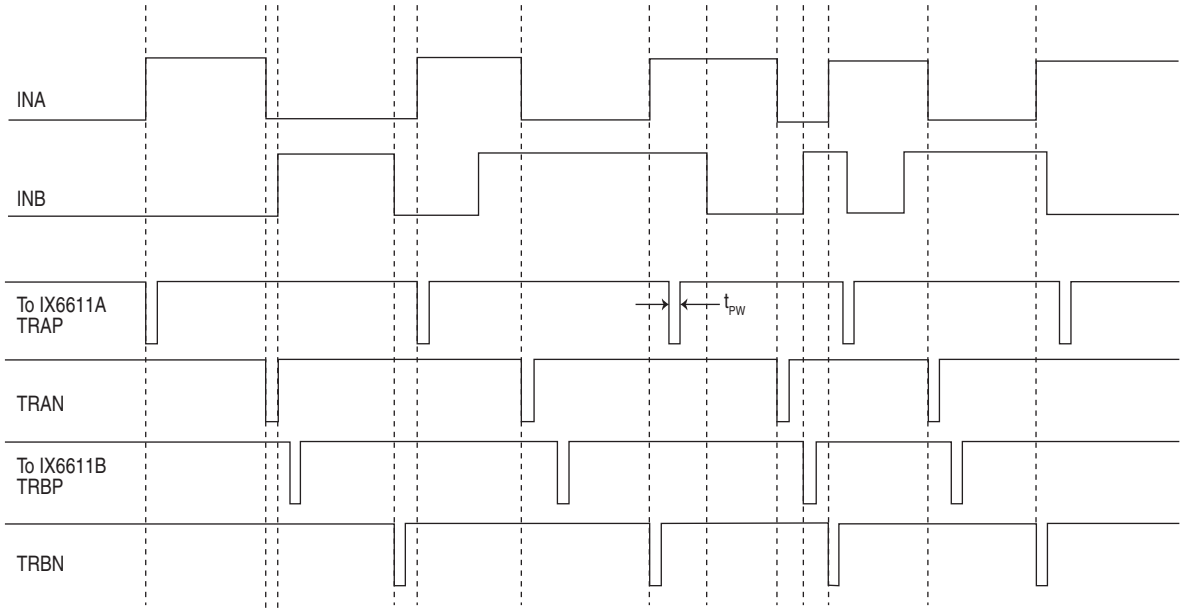


Figure 5 Secondary Side Under Voltage Condition FAULT1 Signal Timing

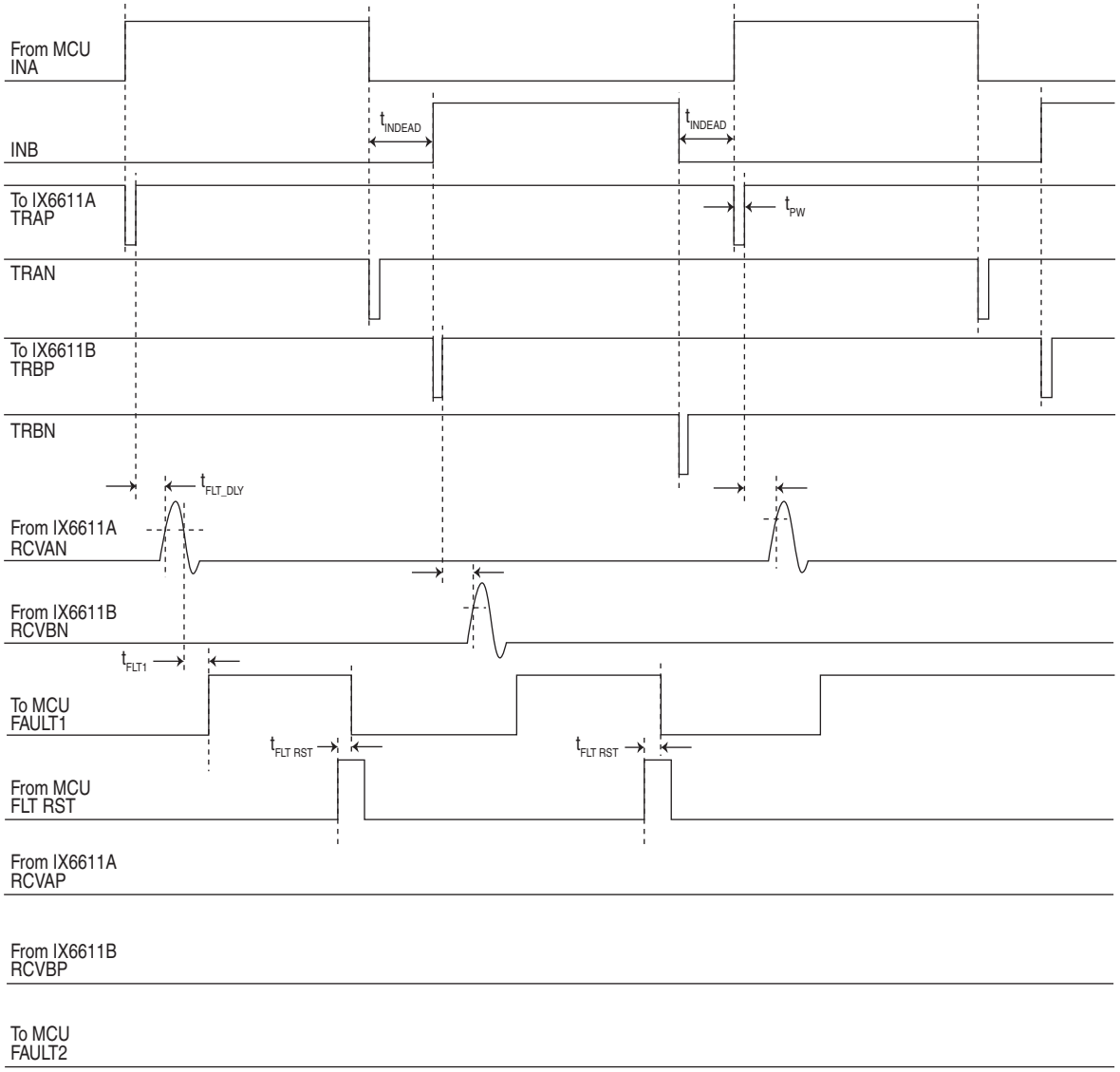


Figure 6 Secondary Side Over Voltage Condition FAULT1 & FAULT2 Signal Timing

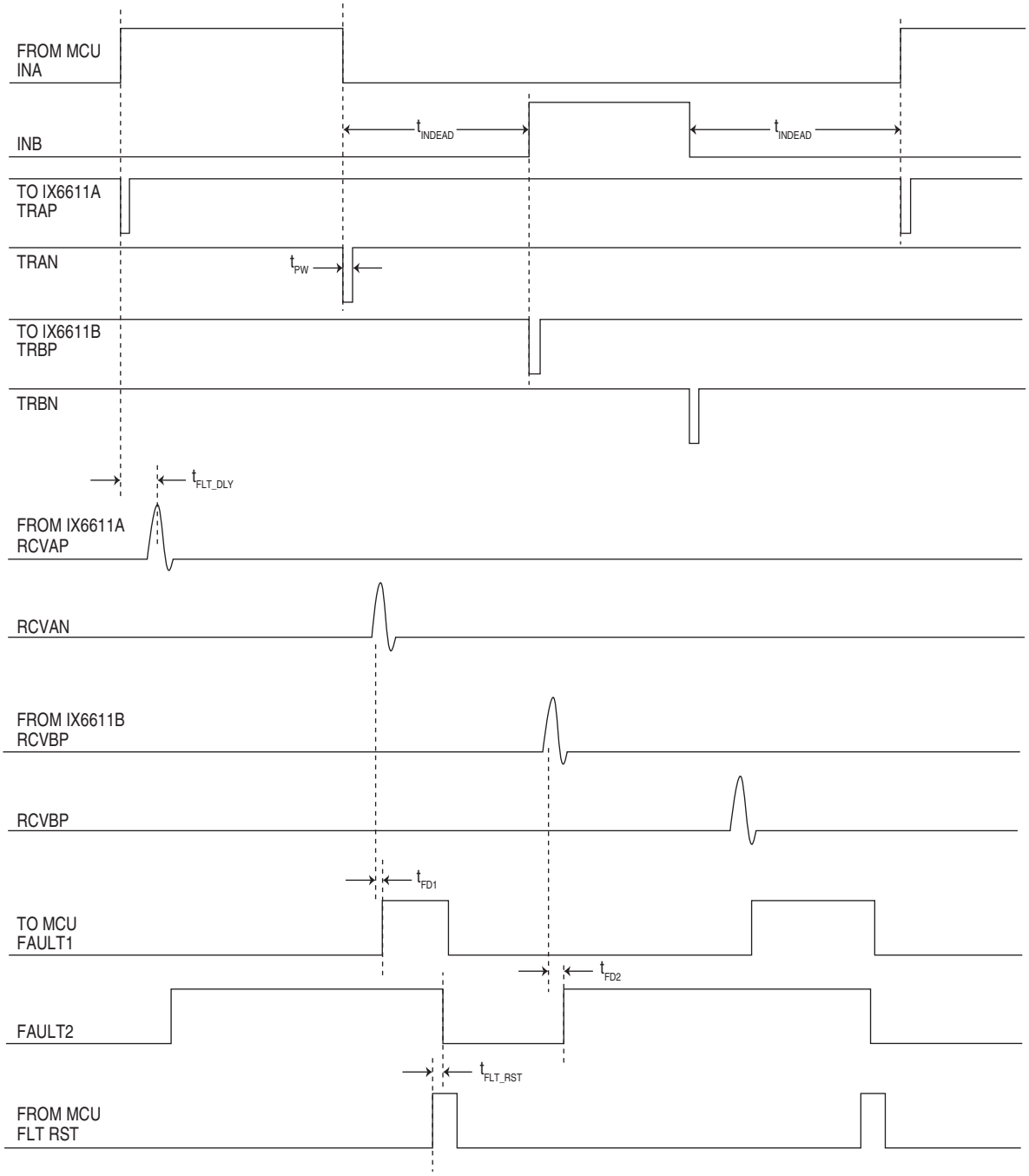


Figure 7 Secondary Side IGBT Over Current Fault Condition FAULT1 & FAULT2 Signal Timing

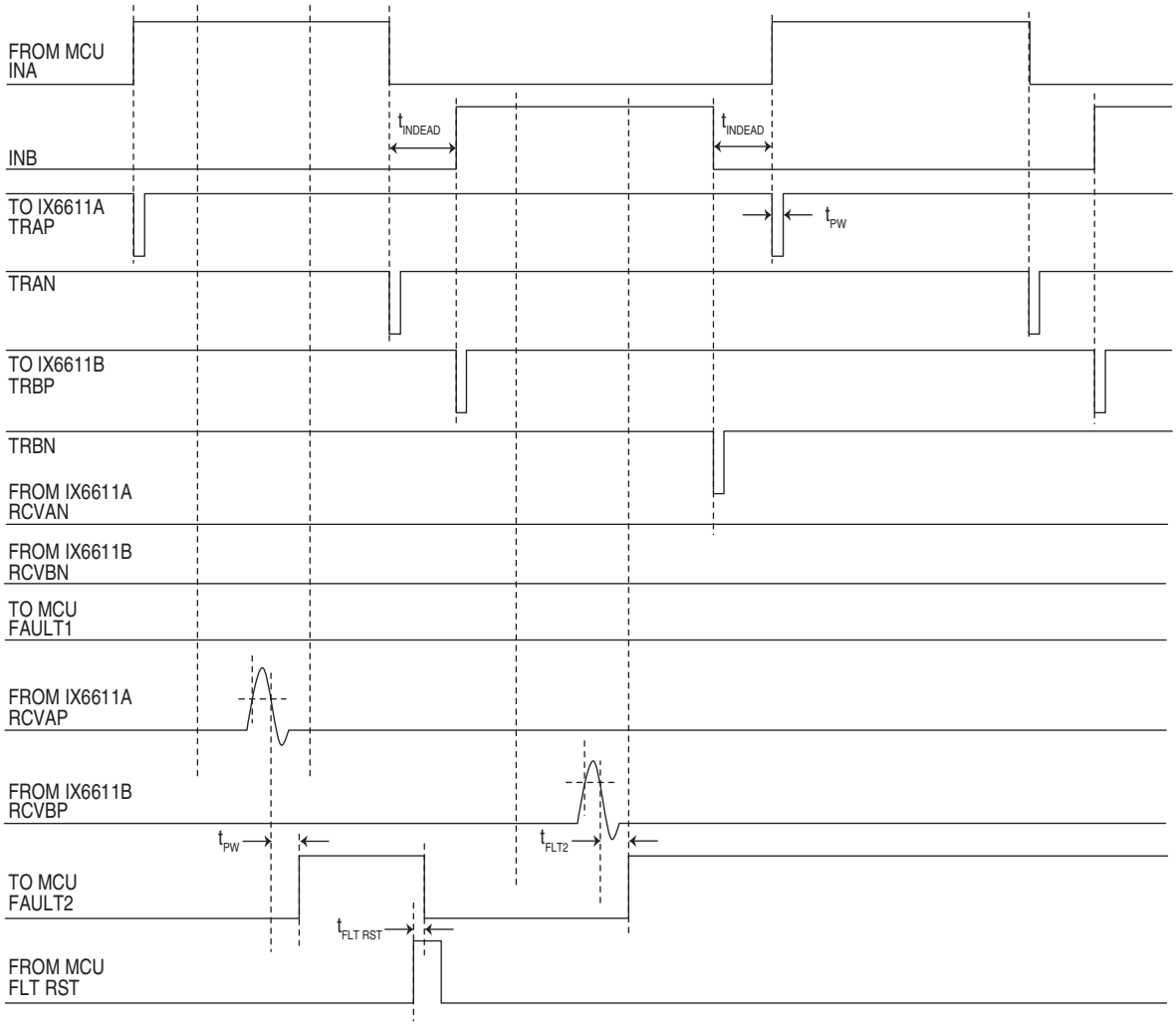


Figure 8 Primary Side UVLO Condition FAULT1 Timing Diagram (FAULT2=0V)

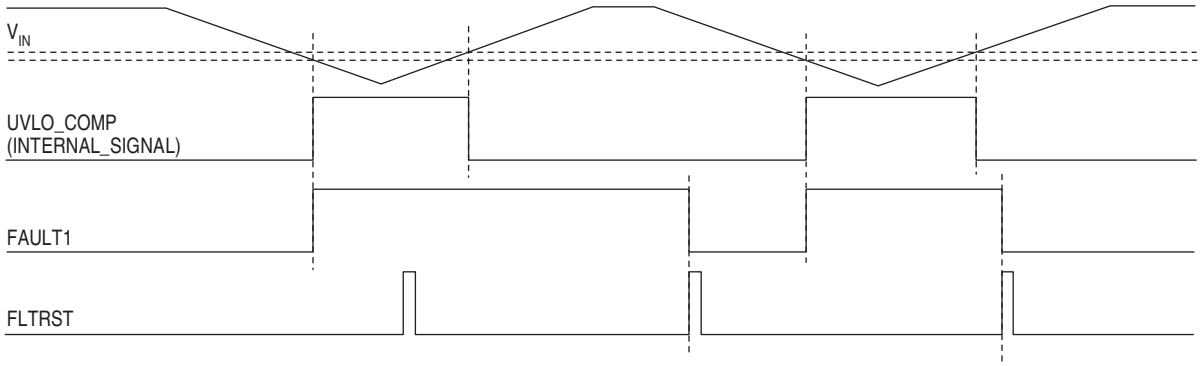


Figure 9 Primary Side OVLO Condition FAULT2 Timing Diagram (FAULT1=0V)

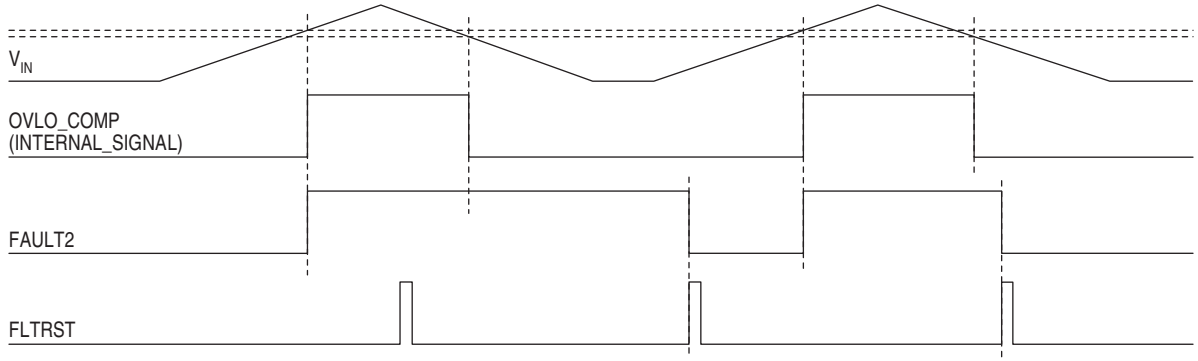


Figure 10 Primary Side Overtemp Condition FAULT1 & FAULT2 Timing Diagram

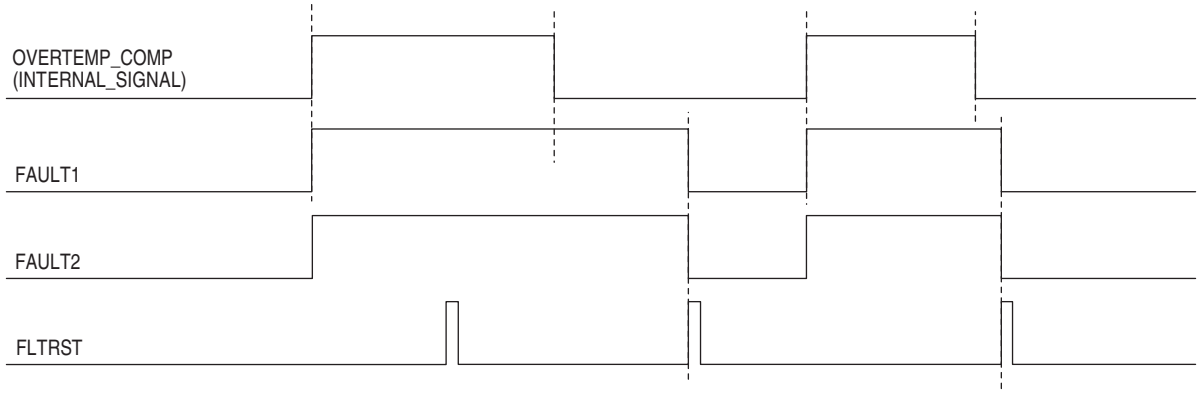


Figure 11 MCU Fault Handling Flow

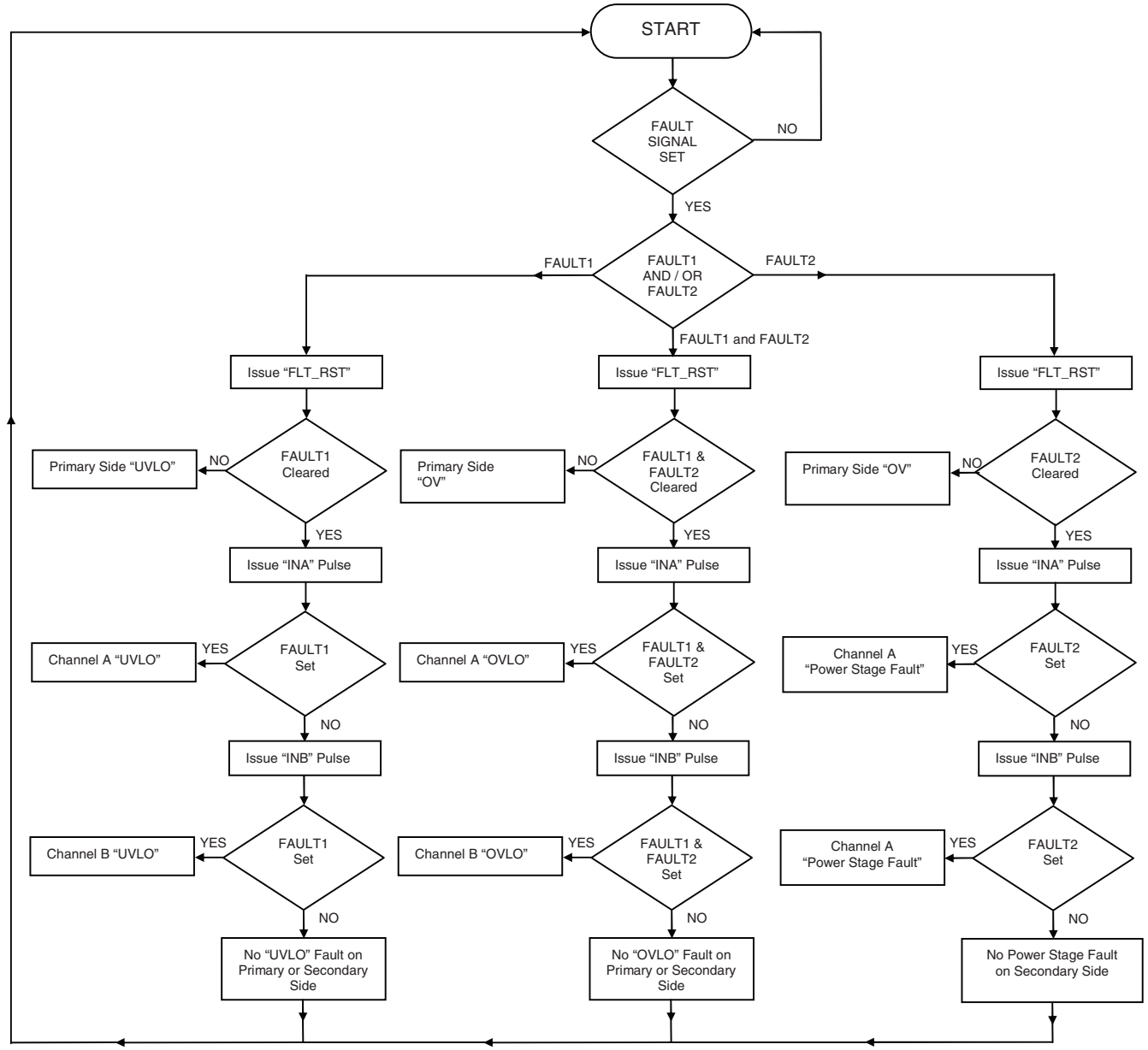
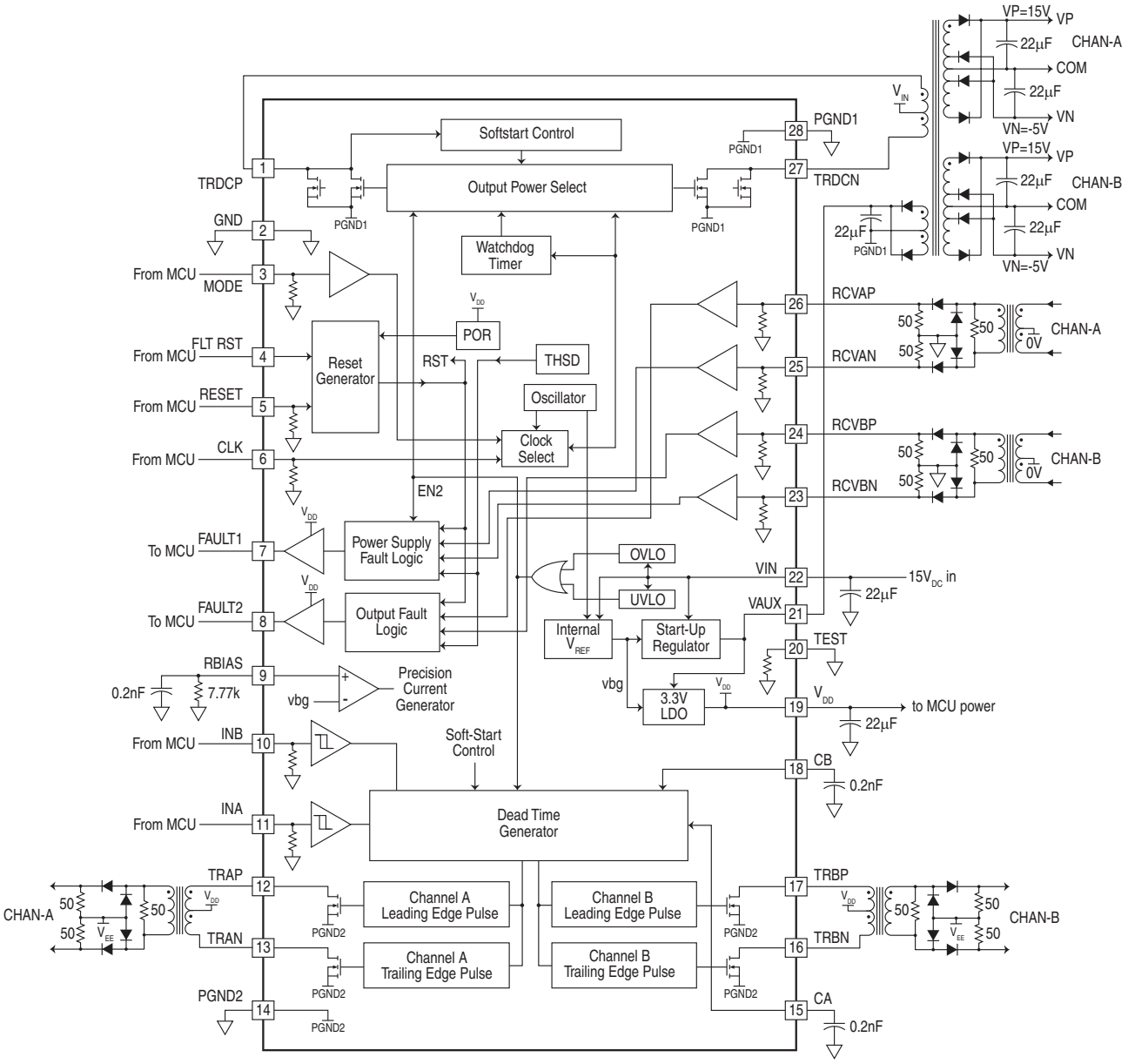


Figure 12 IX6610 Application Diagram



2 Theory of Operation

The IX6610 is a PWM logic signal interface IC used on the primary side of a transformer coupled IGBT gate driver.

2.1 Detailed Circuit Description

2.1.1 Digital Input Interface

The external MCU provides TTL level compatible input signals INA and INB. These input signals are fed through the Schmitt trigger buffers to control the secondary side IGBT drivers. An input signal interlock function is implemented to prevent the simultaneous conduction of the secondary side High side and Low side IGBT's. **Figure 4** shows the behavior of the interlock function.

2.1.2 Short Pulse Filter

A narrow pulse detector is implemented in the IX6610 to prevent transmission of very narrow false PWM input signals to the IGBT drivers due to noise coupling at the input pins. Input signal pulse widths narrower than 100ns will be suppressed and pulse widths greater than 350ns will be transferred to the IGBT drivers.

2.1.3 Dead Time Generator

In the half bridge driver configuration, dead time needs to be added to the incoming input signals to prevent shoot through due to overlap of the high side and low side drivers. The required dead time is programmed by the external MCU.

The IX6610 also contains a dead time circuit that adds dead time to the input signals INA and INB after the input signal interlock function. This dead time applies only if the programmed MCU dead time is shorter than the IX6610 dead time. The IX6610 dead time can be programmed by changing the external capacitors at the CA and CB terminals. **Figure 1** shows the dead time insertion.

2.1.4 Oscillator

The IX6610 includes a 200kHz internal oscillator circuit that provides a 100kHz, 47% duty cycle clock to the power converter control circuit. The oscillator circuit provides the necessary high frequency clock signals to the watchdog timer. The power converter begins operation using the internal oscillator, and switches over to the MCU CLK input once it has detected a valid clock. Note that if the MCU CLK stops, then the power converter will be clocked by the internal oscillator. **Figure 3** shows the relationship of external CLK to the power converter clock. Duty cycle of CLK pin input determines the duty cycle of the power converter operation using the following formula:

$$DutyCycle_{DC\_CLK} = 0.5 - \frac{DutyCycle_{CLK}}{2.015}$$

2.1.5 Under Voltage Lockout

The Under Voltage Lockout (UVLO) circuit holds both PWM logic control signals INA and INB low during the V_{IN} supply ramp-up. When the supply voltage rises above the UVLO upper threshold, the UVLO circuit allows the PWM inputs to control the drivers. FAULT1 output is driven high during the UVLO condition. **Figure 8** illustrates the UVLO function.

2.1.6 Over Voltage Lockout

The over voltage lockout (OVLO) circuit holds both PWM logic control signals INA and INB low and disables the power converter control block during any V_{IN} over voltage condition. When V_{IN} supply voltage falls below the OVLO threshold, the OVLO circuit allows the PWM inputs to control the drivers and enables the power converter control block. FAULT1 and FAULT2 outputs are driven high during the OVLO condition. **Figure 9** illustrates the OVLO function.

2.1.7 Signal Transformer Primary Switches and Pulse Generators

The signal transformer primary terminals are connected to high current switches. Gate drive to the high current switches is controlled by the logic input signals INA and INB, which, when active, produce a high current pulse on the rising edge and falling edge of the input signals at the TRAP (TRBP) and TRAN (TRBN) outputs respectively. Narrow pulses are used to drive the transformer switches, see **Figure 1**.

2.1.8 Signal Transformer Secondary Receive Inputs and Fault Detect

The IX6610 has four single ended receiver comparators which sense the presence of signals that are more positive than a fixed positive threshold value. A 1kΩ pull down resistor to ground is connected to each of the receiver inputs. An external low pass filter can be implemented to prevent impulse noise from triggering the receivers. Receiver comparators are high speed Schmitt Trigger buffers with 1V typical hysteresis.

Secondary side power supply faults and IGBT power stage faults are transmitted back to the IX6610 (primary side) through a pulse transformer. The FAULT1 output is used to signal power supply under voltage fault events on either the secondary side or the primary side. The FAULT2 output is used to signal a secondary side power stage fault. FAULT1 and FAULT2 outputs together signal primary and secondary side over voltage fault events.

Primary side and secondary side power supply faults are latched, and fault flags are asserted logic high.

If the FAULT1 and FAULT2 flags are set by primary side power supply or over-temp faults, then the input signals to the secondary side drivers are disabled. When the device recovers from the primary side power supply faults, the auto restart feature or external

FLTRST clears the fault flags, and normal operation resumes.

If the FAULT1 and FAULT2 flags are set by secondary side under voltage or over voltage faults, then the input signals are not disabled, and the fault flags are reset only by a logic high signal at the FLTRST input.

A secondary side IGBT power stage over current fault is latched, FAULT2 output is asserted logic high, and the input signals are not disabled. The flag is reset only by applying a logic high signal to the FLTRST input.

The MCU can continuously monitor the FAULT1 and FAULT2 flags. If the fault flags are set, then the MCU will determine the fault condition by detecting the fault signals and manipulating the FLTRST as shown in **Figure 5** through **Figure 10** and the MCU FAULT HANDLING FLOW diagram.

FAULT1	FAULT2	Operational Status
0	0	Normal operation
1	0	Primary or secondary side UVLO condition
0	1	Primary side OVLO or secondary side power stage fault condition
1	1	Primary side OVERTEMP or secondary side OVLO condition

2.1.9 Push-Pull Power Converter Control

The IX6610 contains all necessary components to implement a push-pull power converter. Push-pull topology provides a simple solution for making isolated power supplies. Push-pull converter topology allows multiple isolated outputs, stepup/stepdown and/or inverted output with low output ripple.

The circuit drives two internal high current switches connected to an external center tapped transformer providing dual isolated secondary side positive and negative voltages for the IGBT drivers in addition to an isolated bootstrapped 5V supply to the IX6610. The transformer's secondary to primary winding ratio determines the isolated output voltages.

The power converter has a startup mode and a run mode. In the startup mode, the converter operates from the internal oscillator or MCU Clock. In the startup mode, to reduce the dynamic current consumption/power dissipation, only a portion of the power switches are enabled. In the run mode, the power converter operates from the internal oscillator or MCU clock with variable duty cycle. In the run mode the entire power switch is enabled. The power converter switches from startup mode to run mode when the IX6610 has detected a reflected voltage threshold of $1.9375*V_{IN}$ on the TRDCP pin during the driver disabled period. The run mode is held off until the reflected voltage threshold detect has been valid for 128 clocks or ~1.28ms. Transmit operation is also disabled during startup mode to minimize current draw in the secondary. Once run mode begins, the IX6610 will no longer monitor the TRDCP voltage, and will continue this mode of operation until a reset occurs returning the power converter to startup mode.

2.1.10 Watchdog Timer

The internal oscillator or an external MCU provides a clock signal to the push-pull power converter. Oscillator failure or MCU clock failure can cause excessive DC current in the primary winding of the power converter. To prevent excessive power dissipation and potential failure of the IC due to clock failure, a watchdog timer is included in IX6610. Whenever the push-pull converter clock is not recognized as a valid clock, the internal clock will take over clocking of the power converter until a valid external clock is detected.

2.1.11 Thermal Shutdown (THSD)

The IX6610 contains a Thermal Shutdown circuit to protect the device against damage due to excessive die temperature. When the junction temperature exceeds 150°C, the power converter is disabled. The device resumes normal operation when the junction temperature falls below 130°C. Thermal shutdown status is transmitted via the FAULT1 and FAULT2 pins to the MCU.

2.1.12 5V Startup Regulator (V_{CC})

The IX6610 V_{CC} startup regulator provides power to the LDO when the auxiliary winding voltage is less than 4.1V. To reduce power loss and to improve efficiency, the startup regulator is connected to the auxiliary winding pin V_{AUX}. The V_{AUX} pin is sourced from the auxiliary winding when the voltage is greater than 4.1V. A large ceramic bypass capacitor is required at the V_{AUX} pin. Reference voltage to the regulator is provided by the internal chopper-stabilized bandgap voltage reference circuit.

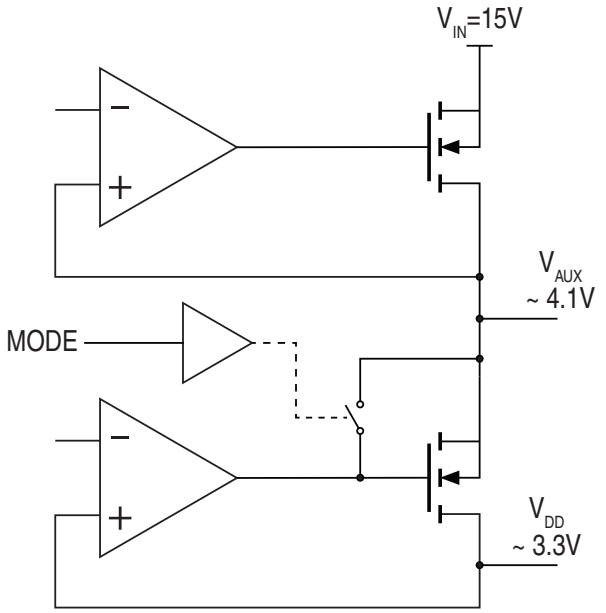
2.1.13 3.3V LDO Regulator (V_{DD})

The LDO regulator provides 3.3V power to the external MCU and most of the IX6610 internal circuits. LDO is sourced from the V_{AUX} pin, and powers up along with the startup regulator (V_{CC}). LDO is designed for a fixed external load capacitor with a predetermined ESR range.

To use the MODE control for an external V_{DD} the external power supply should be connected to the 3.3V V_{DD} output pin only after the IX6610 starts with its internal power supply and MODE pin is set logic HIGH with current limiting resistor (~1kΩ) to prevent powering logic from a signal source.

Notes on MODE feature to shut down the internal V_{DD} regulator:

- To avoid overstress to the device, it is recommended to allow the internal regulators to power up prior to connecting an external power supply via the MODE feature.
- The external supply should not exceed V_{CC} (4.1V)
- The following diagram shows the device connections of the internal regulator pass devices.



2.1.14 Dead Time Delay Capacitor Selection

Ceramic capacitors are recommended for CA and CB dead time capacitors. They should be located as close as possible to the pins and connected to a low noise ground.

2.1.15 RESET

A Logic high level at the external reset pin disables the power converter, the LDO, initiates power converter startup sequence, and resets the fault flags. Holding RESET low for sufficient time will lower the LDO voltage to a level that may initiate a POR sequence in the MCU. The RESET pin has an internal 20kΩ pull down resistor.

2.1.16 TEST

The TEST pin should be tied to ground.

3 Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Corporation classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX6610T / IX6610TR	MSL 1

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be above (T_C - 5)°C. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

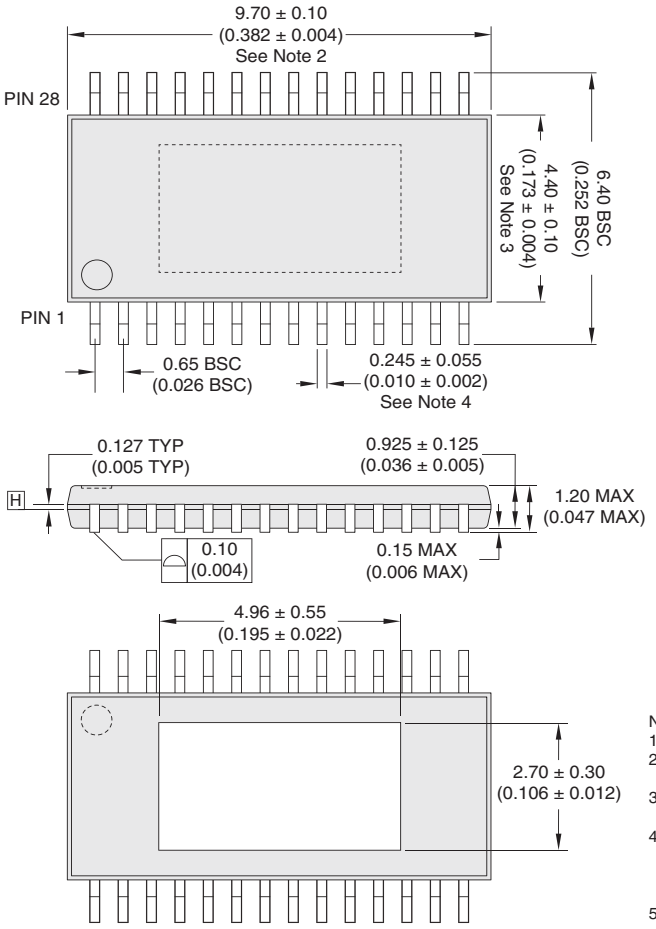
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX6610T / IX6610TR	260°C	30 seconds	3

3.4 Board Wash

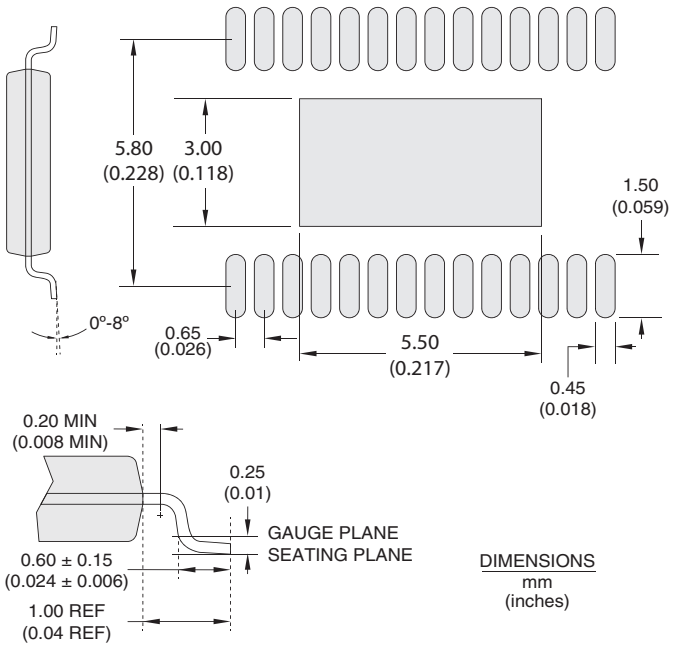
IXYS Corporation recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

3.5 Mechanical Dimensions

3.5.1 IX6610T 28-Pin TSSOP



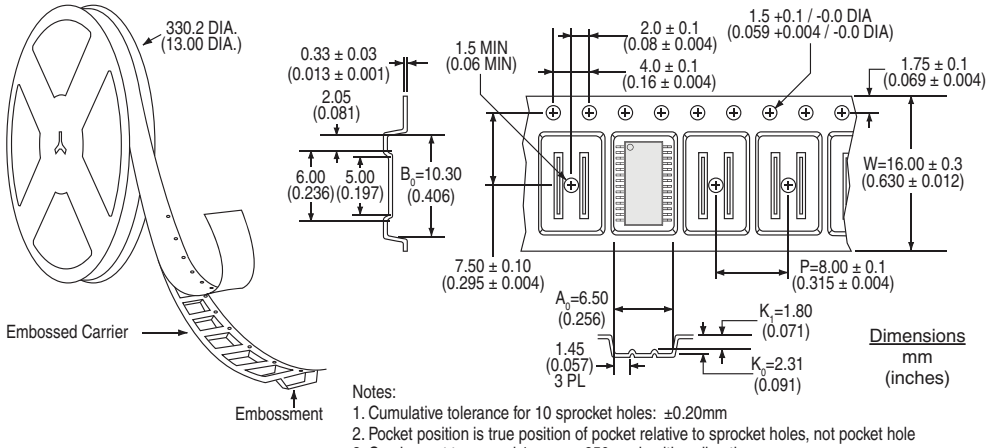
Recommended PCB Land Pattern



DIMENSIONS
mm
(inches)

NOTES:
1. JEDEC Outline: MO-153 AET Rev. F
2. Dimension does not include mold flash protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
4. Dimension does not include dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of this dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Package length and width to be determined at datum plane H.

3.5.2 IX6610T 28-Pin TSSOP Tape & Reel



Dimensions
mm
(inches)

Notes:
1. Cumulative tolerance for 10 sprocket holes: ±0.20mm
2. Pocket position is true position of pocket relative to sprocket holes, not pocket hole
3. Camber not to exceed 1mm per 250mm in either direction

For additional information please visit our website at: www.ixys.com

Specification: DS-IX6610-R00A

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