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IXA531

Preliminary Data Sheet

500mA 3-Phase Bridge Driver

Features

- Fully operational to +650V
- Tolerant of negative transient voltages
- dV/dt immune (50V/ns)
- Latch-up protected over entire operating range
- Fault-current shutdown for all drive outputs
- User selectable delay or latching function for clearing of the FAULT signal, independent user controlled clearing of the FAULT signal is also available
- UVLO protection for all drive outputs
- Enable signal capable of disabling all driver outputs
- 3 half-bridge driver pairs (independent)
- 3.3V logic compatible
- Cross-conduction prevention logic, 220 ns - 360ns Phase leg deadtime
- Peak output current: 600mA Pull-up/Source, 600mA Pull-down/Sink
- Wide operating supply voltage range: 8.0V to 35V
- Capacitive load drive capability: 1250pF in < 100ns
- Matched, low propagation delay times
- Low supply current
- Monolithic construction
- Fault monitoring is accompanied by a $\overline{FLT}$ signal indication, with programmable reset or user selectable latched protection
- Target package power dissipation capability is 2.0W.
- Full level of function available from -55°C to + 125°C
- Available in 48-Lead 7mm x 7mm MLP Quad package and 44-Lead PLCC package

General Description

The IXA531 is a monolithic, 3-phase, MOSFET/IGBT gate driver consisting of three independent, high and low side output channels. In addition to the six inputs, which are CMOS/TTL Compatible, for the three corresponding high side and three low side outputs, there are dedicated lines for FAULT, ENABLE and RESET. Overload/Short Circuit protection is implemented by sensing a voltage across a shunt or low value resistor which carries load current. Upon Overload/Short Circuit detection, all outputs are disabled. Likewise ENABLE (EN) pin, when LOW under abnormal operating conditions, affords soft shut down of outputs. FAULT(FLT) signal's status indicates that shut down has occurred either due to Overload/Short Circuit in driven MOSFET/IGBT or Under Voltage on $V_{CL.}$ Clearing of FAULT (FLT) signal and restoration of normal operation ensue automatically after a programmed delay using an RC Network wired at RST (RESET) pin. Matched propagation delays ensure proper operation even at very high switching frequencies. Absence of cross conduction in output stages removes possibility of shoot through in driven power MOSFETs or IGBTs.

Applications

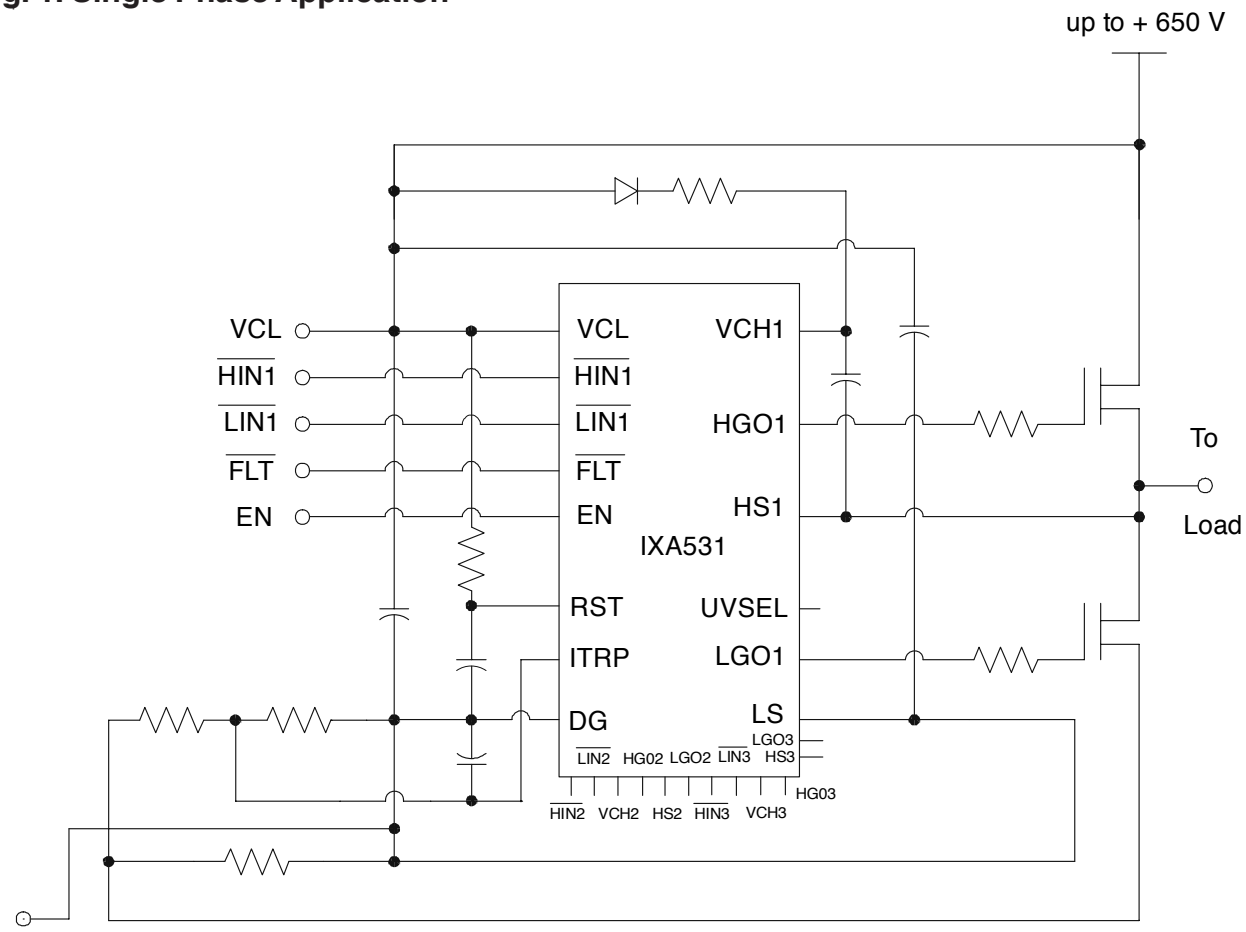
- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

Ordering Information

Part	Package
IXA531S10	48L - SSLGA
IXA531L4	44L - PLCC

Warning: The IXA531 is ESD sensitive.

Fig. 1. Single Phase Application



Pin Description And Configuration

SYMBOL	FUNCTION	DESCRIPTION
$\overline{\text{HIN1,2,3}}$	HS Input	High side Input signal, TTL or CMOS compatible; HGO1,2,3 out of phase
$\overline{\text{LIN1,2,3}}$	LS Input	Low side Input signal, TTL or CMOS compatible; LGO1,2,3 out of phase
EN	Enable	Chip enable. When driven high, both outputs go low.
DG	Ground	Logic Reference Ground
VCH1,2,3	Supply Voltage	High Side Power Supply
HGO1,2,3	Output	High side driver output
HS1,2,3	Return	High side voltage return
V_{CL}	Supply Voltage	Low side and Logic fixed power supply. This power supply provides power for all outputs. Voltage range is from 8.0 to 35V.
LGO1,2,3	Output	Low side driver output
LS	Low side return	Low side driver return
$\overline{\text{FLT}}$	Fault	Indicates Low-Side under voltage or Over Current Trip
ITRP	Trip	Input for over current shutdown
RST	Delay after trip	Externally connected RC network decide FAULT CLEAR delay.

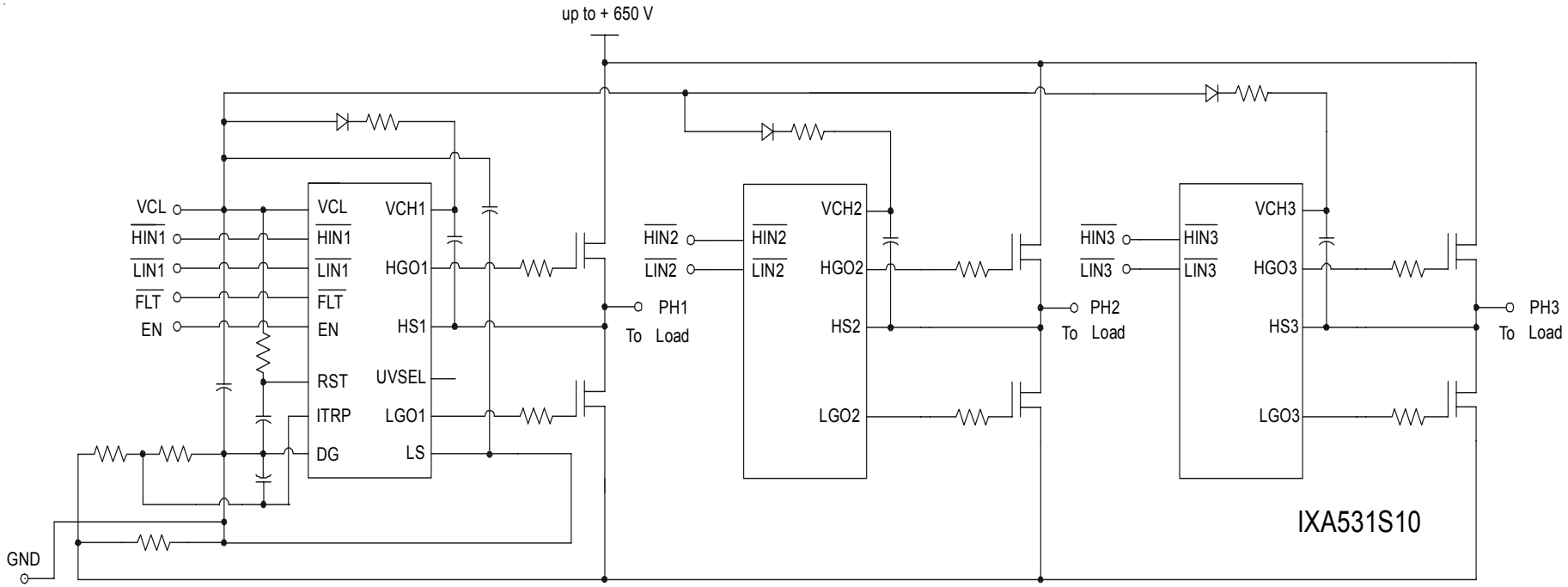


Fig. 2. 3-Phase Application for the IXA531.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to LS. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions

Symbol	Definition	Min.	Max.	Units
V_{CH}	High side floating supply voltage , ($V_{CH1,2,3}$)	-200	650	V
V_{HS}	High side floating supply offset voltage , ($V_{HS1,2,3}$)	$V_{CH1,2,3}$ - 35	$V_{CH1,2,3}$ + 0.3	V
V_{HGO}	High side floating output voltage , ($V_{HGO1,2,3}$)	$V_{HS1,2,3}$– 0.3	$V_{CH1,2,3}$ + 0.3	V
V_{CL}	Low side and logic fixed supply voltage	8.0	35	V
V_{DG}	Logic Supply offset voltage	V_{LS} - 0.7	V_{LS} + 0.7	V
V_{LGO}	Low side output voltage	- 0.3	V_{CL} + 0.3	V
V_{IN}	Input voltage $\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, ITRP, RST , EN	V_{DG} – 0.3	Lower of (V_{DG} + 35) or (V_{CL} + 0.3)	V
V_{FLT}	FAULT output voltage	V_{DG} – 0.3	V_{CL} + 0.3	V
dV/dt	Allowable offset voltage slew rate		50	V/ns
P_D	Package power dissipation@ $T_A \leq +25^oC$		2.0	W
Rth_{JA}	Thermal resistance, junction to ambient		63	K/W
T_J	Junction temperature		125	^oC
T_S	Storage temperature	-55	150	^oC
T_L	Lead temperature (soldering, 10 seconds)		300	^oC

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute values referenced to LS. The V_{HS} offset rating is tested with all supplies baised at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{CH1,2,3}$	High side floating supply voltage	$V_{HS1,2,3}$ + 12	$V_{HS1,2,3}$ + 35	V
$V_{HS1,2,3}$	High side floating supply offset voltage	- 200	650	V
$V_{HGO1,2,3}$	High side floating output voltage	$V_{HS1,2,3}$	$V_{CH1,2,3}$	V
$V_{LGO1,2,3}$	Low side output voltage	0	V_{CL}	V
V_{CL}	Low side and logic fixed supply voltage	12	35	V
V_{DG}	Logic Supply offset voltage	V_{LS} - 0.3	V_{LS} + 0.3	V
V_{FLT}	FAULT output voltage	V_{DG}	V_{CL}	V
V_{RST}	RST input voltage	V_{DG}	V_{CL}	V
V_{ITRP}	ITRP input voltage	V_{DG}	V_{CL}	V
V_{IN}	Logic input voltage $\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, EN	V_{DG} or V_{LS}	V_{CL}	V
T_A	Ambient temperature	-40	125	^oC

Static Electrical Characteristics

V_{BIAS} (V_{CL}, $V_{CH1,2,3}$) = 15V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to DG and are applicable to all six channels . The V_O and I_O parameters are referenced to LS and $V_{HS1,2,3}$ and are applicable to the respective output leads: $H_{GO1,2,3}$ and $L_{GO1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{INL}	Logic "0" input voltage $\overline{HIN1,2,3}$; $\overline{LIN1,2,3}$			0.8	V	
V_{INH}	Logic "1" input voltage $\overline{HIN1,2,3}$; $\overline{LIN1,2,3}$	3.0			V	
$V_{EN,TH+}$	EN positve going threshold			3.0	V	
$V_{EN,TH-}$	EN negative going threshold	0.8			V	
$V_{ITRP,TH+}$	ITRP positve going threshold	0.37	0.46	0.55	V	
$V_{ITRP,HYS}$	ITRP input hysteresis		.07		V	
$V_{RST,TH+}$	RST positive going threshold		8		V	
$V_{RST,HYS}$	RST input hysteresis		3		V	
$V_{OH1,2,3}$	High level output voltage, V_{CH} - V_{HGO} or V_{CL}- V_{LGO}		0.9	1.4	V	I_0=20mA
$V_{OL1,2,3}$	Low level output voltage, V_{HGO} or V_{LGO}		0.4	0.6	V	I_0=20mA
VCLUV+	VCL supply under-voltage positive going threshold	10.6	11.1	11.6	V	
V_{CHUV+}	V_{CH} supply under-voltage positive going threshold	10.6	11.1	11.6	V	
V_{CLUV-}	V_{CL} supply under-voltage negaitive going threshold	10.4	10.9	11.4	V	
V_{CHUV-}	V_{CH} supply under-voltage negaitive going threshold	10.4	10.9	11.4	V	
V_{CLUVH}	V_{CL} supply under-voltage lockout hysteresis		0.2		V	
V_{CHUVH}	V_{CH} supply under-voltage lockout hysteresis		0.2		V	
I_{LK}	Offset supply leakage current			50	µA	$V_{CH1,2,3}$= $V_{HS1,2,3}$=600 V
I_{QVCH}	Quiescent V_{CH} supply current		70	120	µA	V_{IN}=0V or 5V
I_{QVCL}	Quiescent V_{CL} supply current		1.6	2.3	mA	V_{IN}=0V or 5V
V_{IN}	Input clamp voltage (HIN,LIN,ITRP,EN)		4.9		V	I_{IN} = 100µA
I_{LIN+} or I_{IN+}	Logic "1" Input bias current for LIN1,2,3		200	300	µA	V_{LIN} = 5V
I_{LIN-} or I_{IN-}	Logic "0" Input bias current for LIN1,2,3		100	220	µA	V_{LIN} = 0V
I_{HIN+} or I_{IN+}	Logic "1" Input bias current for HIN1,2,3		200	300	µA	V_{HIN} = 5V
I_{HIN-} or I_{IN-}	Logic "0" Input bias current for HIN1,2,3		100	220	µA	V_{HIN} = 0V
I_{ITRP+}	"high" ITRP input bias current		30	100	µA	V_{ITRP} = 5V
I_{ITRP-}	"low" ITRP input bias current		0	1	µA	V_{ITRP} = 0V
I_{EN+}	"high" ENABLE input bias current		30	100	µA	V_{EN} = 5V
I_{EN-}	"low" ENABLE input bias current		0	1	µA	V_{EN} = 0V
I_{RST}	RST input bias current		0	1	µA	V_{RST} = 0Vor 15V
I_{GO+}	Output high short circuit pulsed current		600		mA	V_0=0V,PW <10 µs
I_{GO-}	Output low short circuit pulsed current		600		mA	V_0=15V,PW<10µs
$R_{ON,RST}$	RST low on resistance		50	100	Ω	
$R_{ON,FLT}$	FLT low on resistance		50	100	Ω	

Dynamic Electrical Characteristics

$V_{CL} = V_{CH} = V_{BIAS} = 15V$, $V_{HS1,2,3} = V_{DG} = V_{LS}$, $T_A = 25°C$ and $C_L = 1000pF$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conds.
t_{on}	Turn-on propagation delay	300	425	550	nS	V_{IN}=0V & 5V
t_{off}	Turn-off propagation delay	250	400	550	nS	V_{IN}=0V & 5V
t_r	Turn-on rise time		125	190	nS	----
t_f	Turn-on fall time		50	75	nS	----
t_{EN}	ENABLE low to output shutdown propagation delay	300	450	600	nS	V_{IN}, V_{EN} = 0 V or 5 V
t_{ITRP}	ITRP to output shutdown propagation delay	500	750	1000	nS	V_{ITRP}=5V
t_{bl}	ITRP blanking time	100	150		nS	V_{IN}=0V or 5V V_{ITRP} = 5V
t_{FLT}	ITRP to FAULT propagation delay	400	600	800	nS	V_{IN} = 0V or 5V V_{ITRP} = 5V
t_{FILIN}	Input filter time (HIN, LIN, EN)	100	200		nS	V_{IN} = 0V & 5V
t_{FLCLR}	FAULT clear time RST=2meg, C=1nF	1.3	1.65	2	mS	V_{IN} = 0V or 5V V_{ITRP}=0V
DT	Dead time	220	290	360	nS	V_{IN} = 0V & 5V
MT	Matching delay ON and OFF		40	75	nS	External Dead Time >400nsec
MDT	Matching delay, max (t_{on}, t_{off}) - min (t_{on}, t_{off}) (t_{on},t_{off} are applicable to all 3 channels)		25	70	nS	
PM	Output pulse width matching, PWM_{IN}-PWM_{OUT}		40	75	nS	

VCL	VCH	ITRP	ENABLE	FAULT	LGO1,2,3	HGO1,2,3
<UVCL	X	X	X	0(note 1)	0	0
15V	<UVCH	0V	15V	high imp	LIN1,2,3	0
15V	15V	0V	15V	high imp	LIN1,2,3	HIN1,2,3
15V	15V	>V_{ITRP}	15V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

Notes: A Cross Conduction logic prevents LGO1,2,3 and HGO1,2,3 for each channel from turning on simultaneously.

1. UVCL is not latched, when VCL>UVCL, FAULT returns to high impedance.
2. When ITRP < V_{ITRP}, FAULT returns to high-impedance after RST pin becomes greater then 8V (@VCL= 15V).

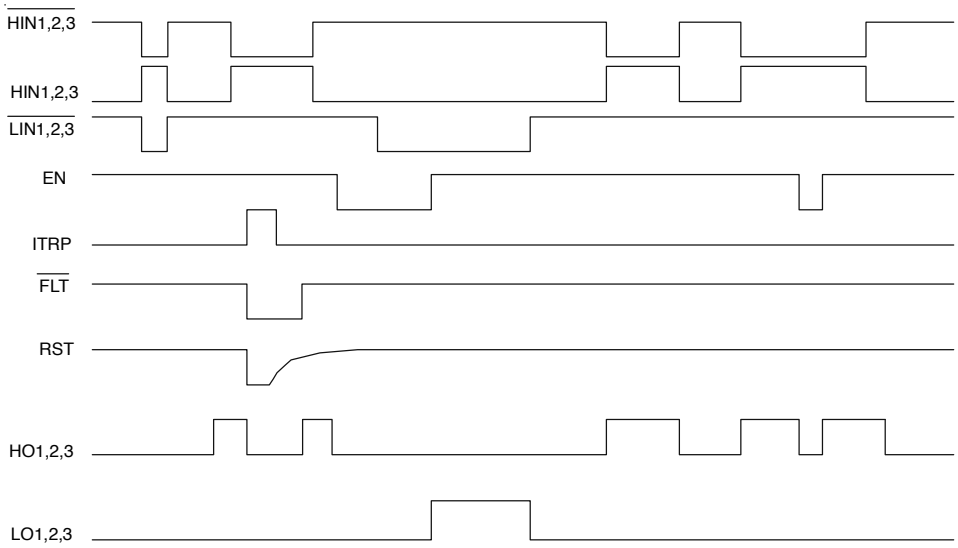


Fig. 3. Timing Diagram

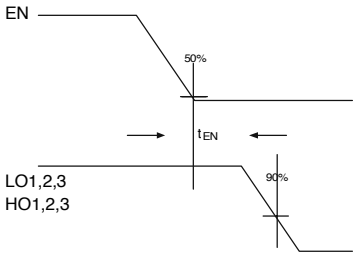


Fig. 4. ENABLE Timing Waveforms

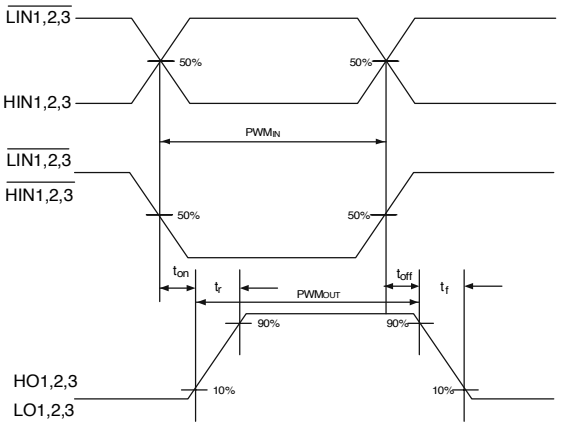


Fig. 5. Switching Time Definitions

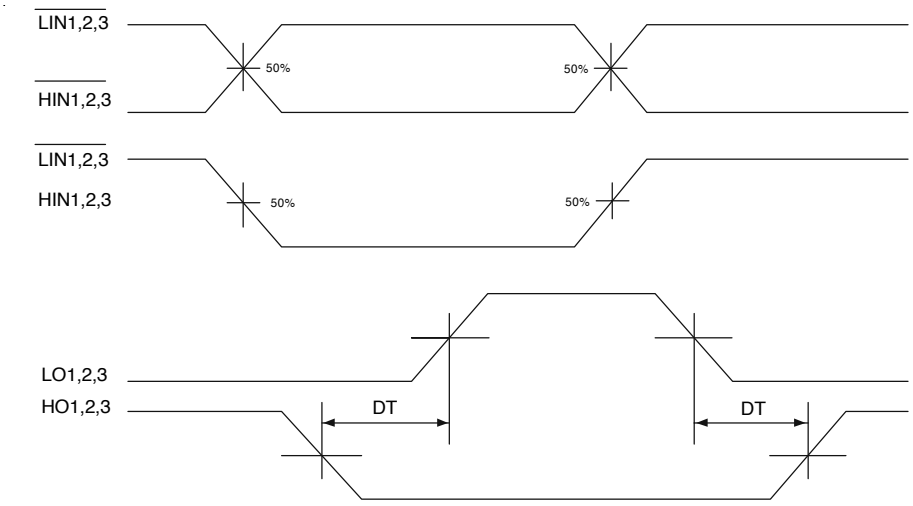


Fig. 6. Deadtime Waveforms

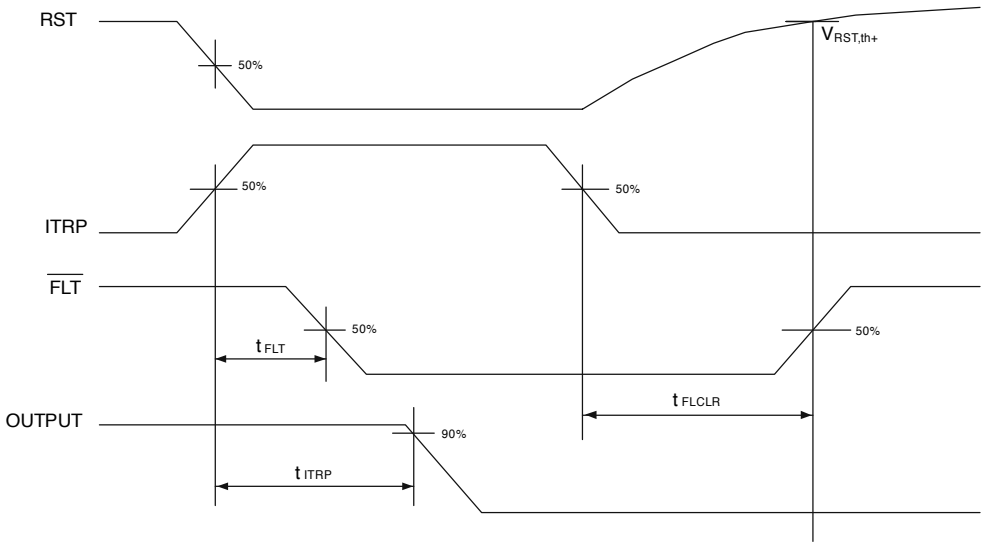


Fig. 7. ITRP / RST Waveforms

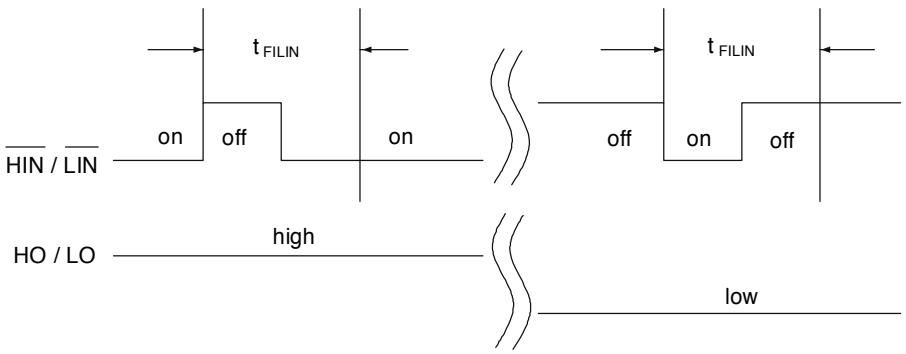


Fig. 8. ENABLE Timing Waveforms

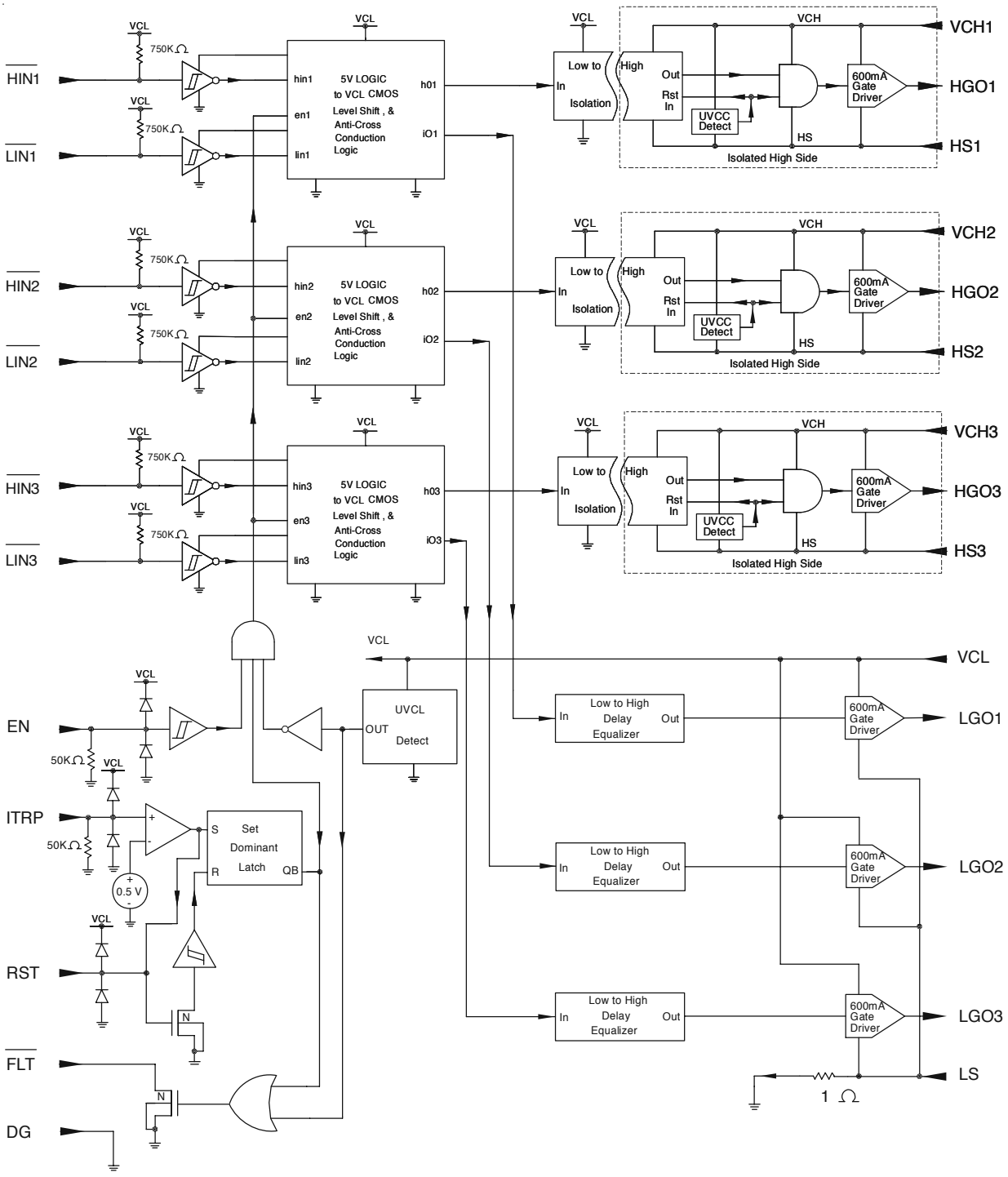


Fig. (9) IXA531 Block Diagram

Fig. 10. Pin Diagram for the IXA531S10 48-Lead MLP Quad Package

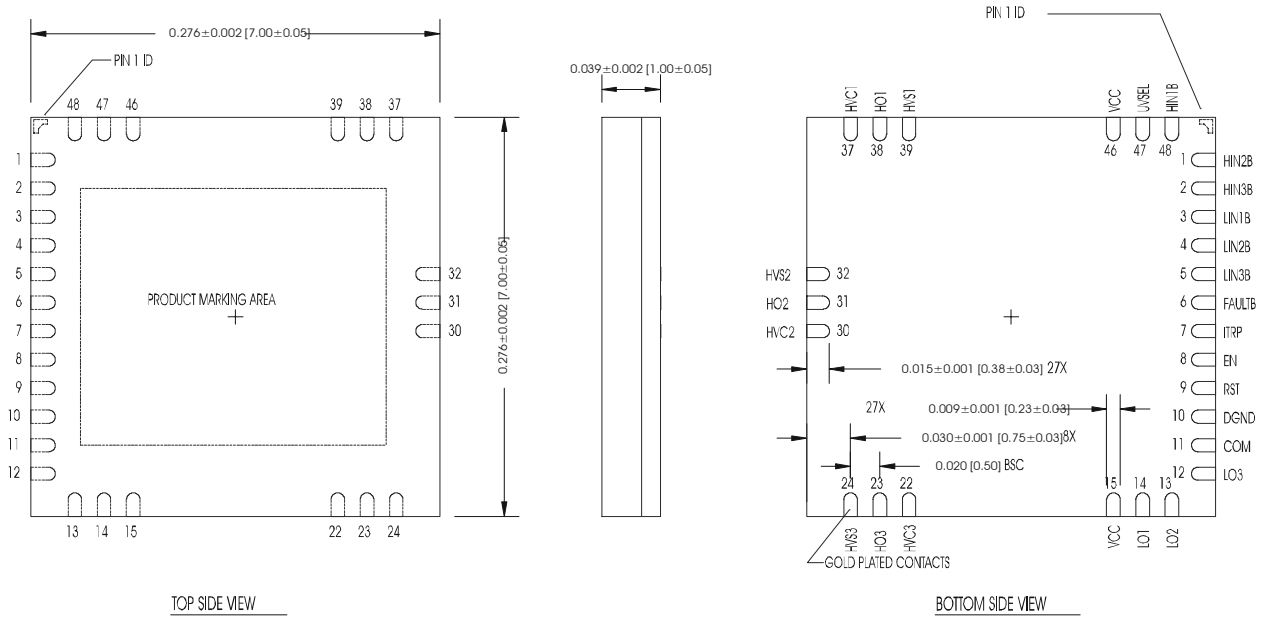


Fig. 11. Pin Diagram for the IXA531L4 44-Lead PLCC package

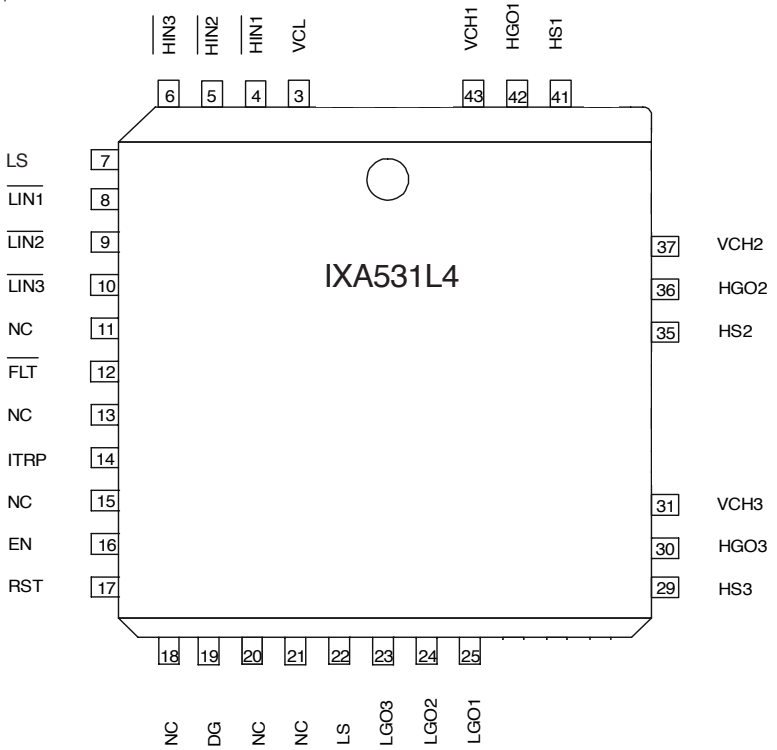
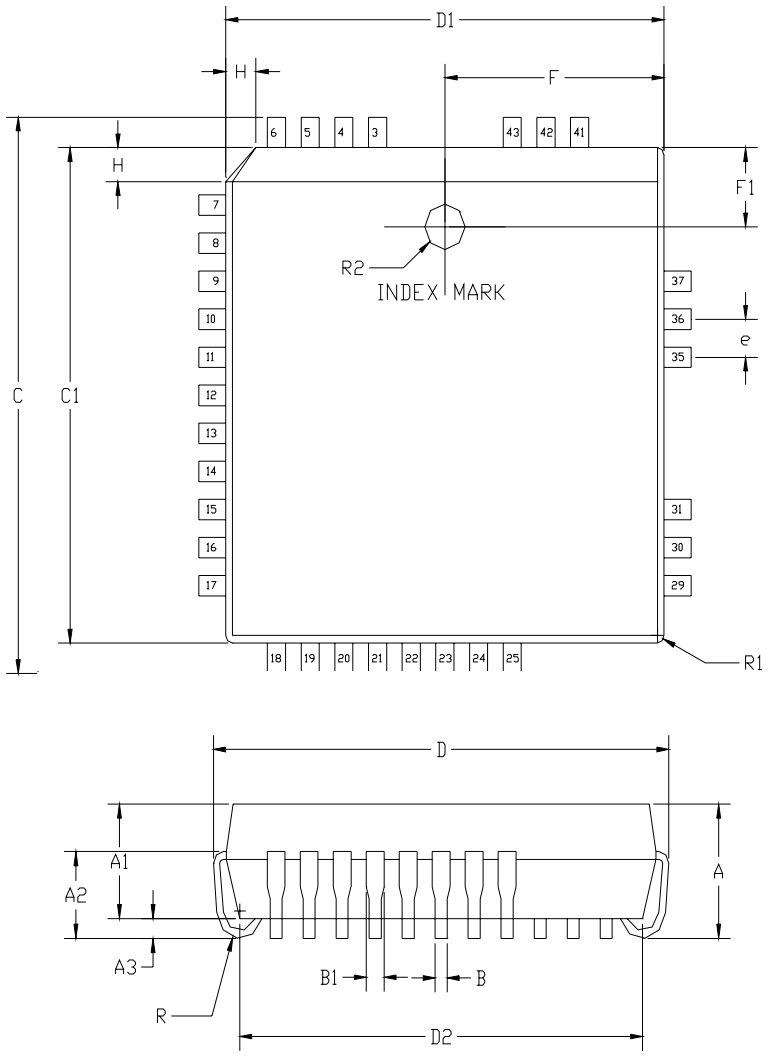


Fig. 12. 44-Lead PLCC Outline Diagram



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.27	4.37	0.168	0.172
A1	3.63	3.73	0.143	0.147
A2	2.49	2.84	0.098	0.112
A3	0.58	0.69	0.023	0.027
B	0.41	0.51	0.016	0.020
B1	0.64	0.74	0.025	0.029
C	17.48	17.58	0.688	0.692
C1	16.48	16.59	0.649	0.653
D	17.48	17.58	0.688	0.692
D1	16.48	16.59	0.649	0.653
D2	15.44	15.54	0.608	0.612
e	1.27 BSC		0.050 BSC	
F	8.22	8.32	0.3235	0.3275
F1	2.58	2.68	0.1015	0.1055
H	1.09	1.19	0.043	0.047
R	0.76	1.02	0.030	0.040
R1	0.20	0.30	0.008	0.012
R2	1.47	1.57	0.058	0.062

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