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IXYS Digital Power

30 A/4000 V HIGH VOLTAGE ISOLATED DRIVER MODULE

IXIDM1403_1505_M
Datasheet

Part Number Options

IXIDM1403_1505_M – two isolated gate drivers with 30 A gate current, 15 V positive and –5 V negative gate voltage, molded package.

Abstract

The IXIDM1403_1505_M driver module combines supreme compactness with the highest performance and reliability. It comprises a dual-channel driver core that targets medium power dual-channel IGBTs for up to 4 kV and applications such as inverters, drives & automation, UPS, renewable energy, transportation, and medical. Its parallel capability allows for an easy, high power system design.

The IXIDM1403_1505_M driver core is equipped with the IX6610/6611 chipset of application-specific integrated circuits that covers the main range of functions required to design intelligent gate drivers. IXIDM1403_1505_M is available in a 56mm x 48mm x 22mm package.

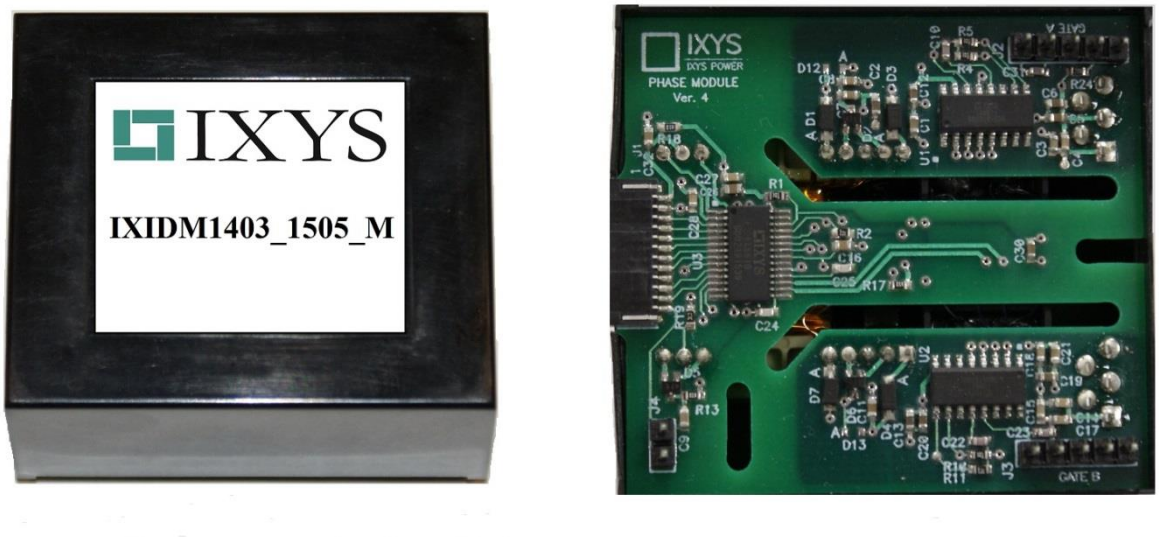

Figure 1. The IXIDM1403_1505_M Driver Module

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30 A/4000 V High Voltage Isolated Driver Module

Features

- Two isolated gate drivers for half bridge switching modules
- Internal power supply for isolated drivers with up to 2W output power per channel
- Non-overlap operation of high side and low side drivers
- TTL logic level microcontroller interface
- Single 15V power supply operation
- +15V/-5V isolated gate driver output voltage to drive IGBTs with up to 30A pulse current
- Minimum input pulse width 500 ns
- Input to output gate driver signal propagation delay 120 ns
- Gate drive pulse width distortion 20 ns
- Under– and over-voltage lockout protection
- Up to 50 mA 3.3V load capability output to drive an external MCU
- FAULT signals informing MCU about over-voltage, under-voltage, and over-current conditions at isolated gate drivers
- Latched FAULT signals from gate drivers to let MCU read fault information asynchronously
- Operating ambient temperature: –40°C～ +105°C
- Driver and internal power supply over-temperature protection with 150°C threshold and 25°C hysteresis
- Environmentally friendly: EU RoHS compliant, Pb-free

Applications

- Various appliances with motors operated by microcontrollers
- High power converters

Description

A High Voltage Isolated Module (IXIDM1403_1505_M) is developed and optimized for electronic motor control applications such as air conditioners, washing machines, refrigerators, and high power buck converters or inverters. It is a compact, high performance device in a single isolated package with a very simple design.

Based on the IX6610/11 chip set, this device enables a 3.3V microcontroller unit (MCU) to operate half-bridge-connected IGBTs through a 4kV isolation barrier providing PWM pulses as short as 500 ns, and no lower limit on switching frequency.

Internal power supply provides up to 2W per channel of isolated power to drive upper and lower IGBTs, effectively isolating the MCU from high power circuitry. Operating from a single polarity 15 V power source, this device provides +15V/–5V to operate IGBT gates and +3.3V at 50 mA to power the MCU from the same source.

Built-in under-voltage and over-voltage protection prevents the IGBT from operating at gate voltages outside the optimal window and informs the MCU about such conditions irrespective of the source of the problem, which may be on either low or high side IGBT behind the isolation barrier or on primary side before the isolation barrier.

Over-current protection with 300mV threshold may utilize either the current sense resistor or IGBT de-saturation event. Over-current protection turns the IGBT off immediately after the collector current exceeds the value set by the customer, informing the MCU about every such event to enable it to make appropriate decisions.

Built-in dead time delay circuitry prevents turning on of both IGBTs simultaneously with channel A priority. If channel B is active and channel A is forced into the ON state, channel B becomes disabled immediately and the channel A IGBT turns on with a delay time of ~0.4 µs. After channel A becomes inactive, channel B, if active, turns on with the same delay time. If channel A is active and channel B is forced into the ON state, this command will be ignored as long as channel A remains active. If channel A becomes inactive before the command activating channel B

expires, channel B becomes active with a delay time of ~400 ns after channel A becomes inactive.

Over-temperature protection disables IGBTs if the temperature of any of the internal chips exceeds 150°C and resumes normal operations when the temperature falls below 125°C.

If IGBT assembly is equipped with a temperature sensor, IXIDM1403_1505_M is able to translate its signal to the MCU for monitoring.

The IXIDM1403_1505_M device is available in a 56mm x 48mm x 22mm package with a 12-pin 1mm pitch FFC connector to communicate with the MCU, two 5-pin 2.54mm pitch headers to provide signals to/from IGBTs and one 2-pin 2.54mm pitch header to translate the signal from the IGBT's assembly temperature sensor.

Typical Application Circuits

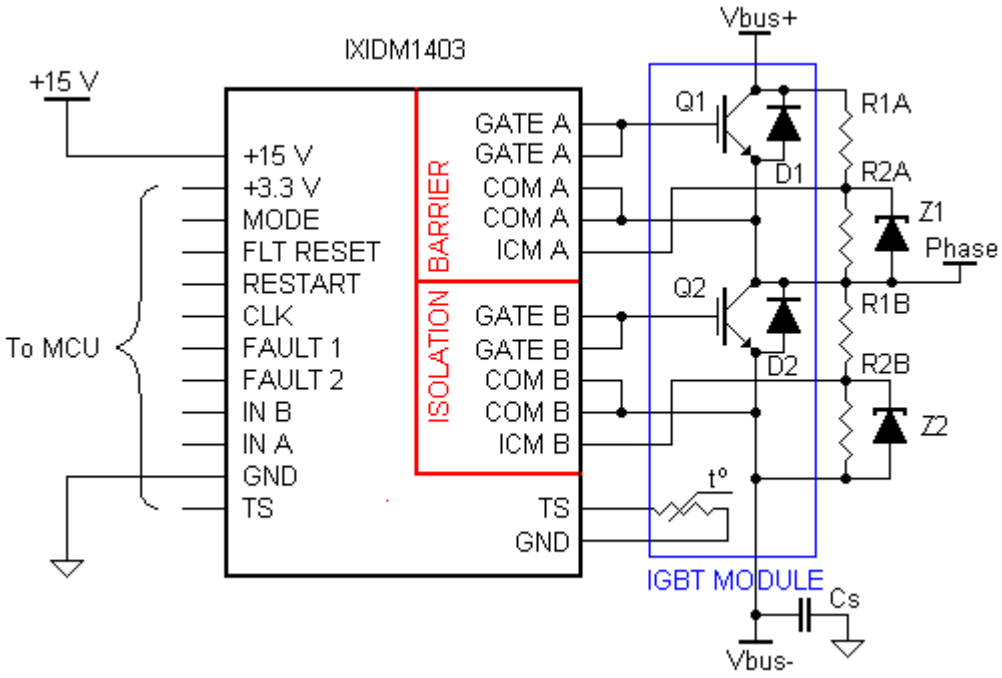


Figure 2. Typical Application Circuit with Half-bridge IGBT Module and De-saturation Over-current Protection

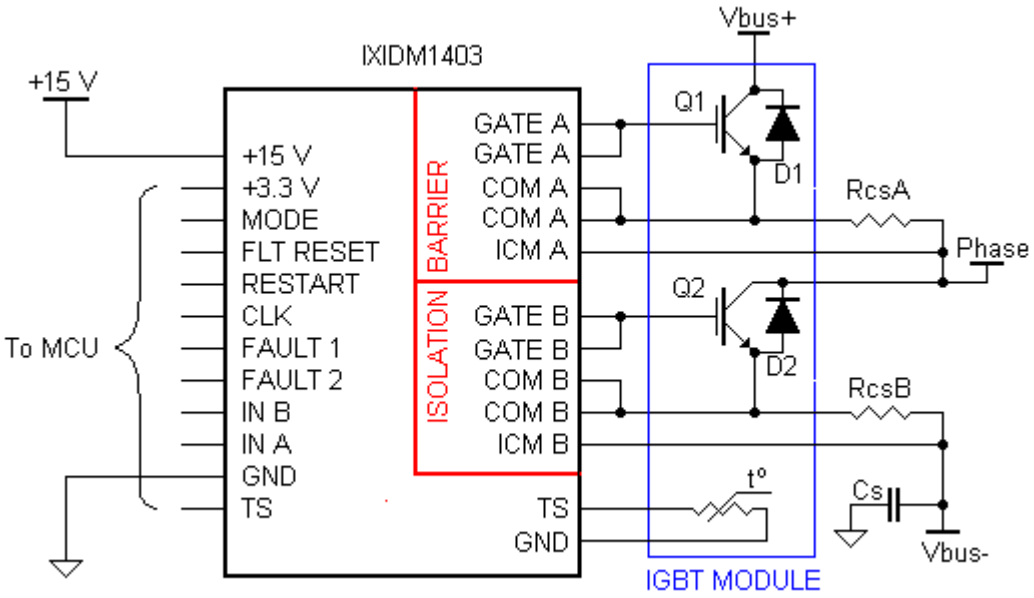


Figure 3. Typical Application Circuit with Half-bridge IGBT Module and Over-current Protection Utilizing Current Sense Resistors

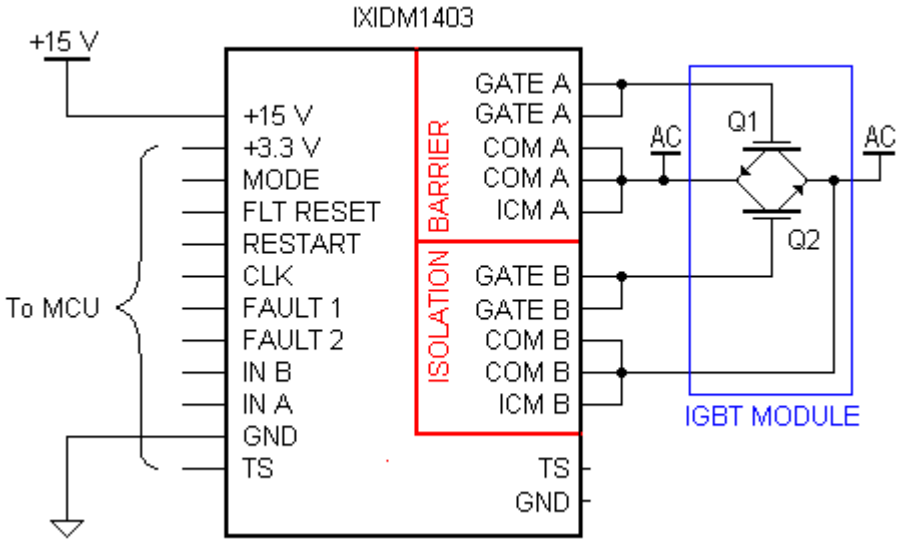


Figure 4. AC Switch with Two RB IGBTs

Absolute Maximum Ratings

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage (+15V)	V_{SUPM}	– 0.3 ~ +18	V
MCU Supply Voltage (+3.3V output)	V_{MCUM}	– 0.3 ~ +6	V
Logic Pin Voltages (INA, INB, FLT_RESET, RESTART, MODE, FAULT1, FAULT2)	V_{LG}	– 0.3 ~ +6	V
ACL Pin Voltage[1)]	V_{ACL}	V_{EE} – 0.3 ~ V_{EE} + 6	V
ICM Pin Voltage[1)]	V_{ICM}	– 0.3 ~+6[)]	V
GATE Pin Voltage[1)]	V_G	V_{EE}– 0.3 ~ +28	V
Operating Temperature Range	T_{OPR}	– 40 ~ + 105	°C
Storage Temperature Range	T_{STG}	– 55 ~ +125	°C

Note:
1) With respect to the COM Pin of the particular driver

Electrical Operating Characteristics

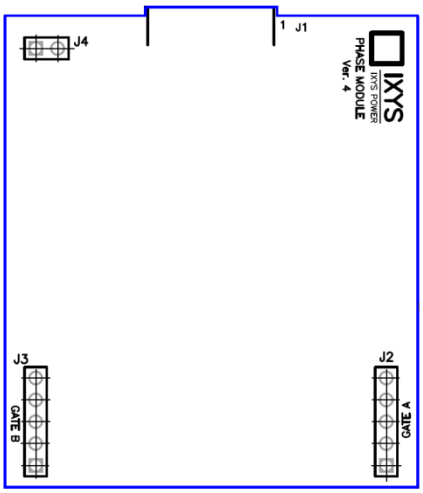
Unless otherwise specified, Ta = 25 ^{0}C

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Normal Operating Power Supply Voltage Range		V_{SUP}		14.0		16.0	V
Under-voltage Lockout Threshold		$UVLO_{TR}$		10	11	12	V
Under-voltage Lockout Hysteresis		$UVLO_{HYS}$			0.5		V
Over-voltage Lockout Threshold		$OVLO_{TR}$		16,5	17,25	18	V
Over-voltage Lockout Hysteresis		$OVLO_{HYS}$			0.5		V
Power Supply Current		I_{SUP}	V_{INA}=V_{INB}=V_{MODE} = 0 V, V_{FLT_RST}= $V_{RESTART}$ =V_{CLK}=V_{FAULT1}=V_{FAULT2} =$V_{+3.3V}$=OPEN			20	mA
MCU Supply Voltage (+3.3 V output)		V_{MCU}	C_{OUT} = 22 µF	3.0	3.3	3.6	V
MCU Supply Voltage Load Regulation		ΔV_{MCU_LR}	I_{MCU} = 1 mA to 50 mA			50	mV
MCU Supply Short Circuit Current						100	mA
MCU Supply Bypass Capacitance ESR		C_{OUT_ESR}		0.3			Ω
Logic Inputs Leakage Current		I_{INLKG}	V_{CLK}=$V_{RESTART}$=V_{INA}=V_{INB}=V_{MODE} =0 V	-1		1	µA
Logic Inputs Pull-down Resistance			CLK, RESTART, INA, INB		25		kΩ
			MODE, FLT_RESET		10		
Logic Inputs Leakage Current		I_{FLT_RESET}	V_{FLT_RESET} = 0 or V_{FLT_RESET}= 3.3 V	-1		1	µA
Logic Inputs High Level		V_{LGH}	CLK, RESTART, INA, INB, MODE, FLT_RESET	2.0			V
Logic Inputs Low Level			CLK, RESTART, INA, INB, MODE, FLT_RESET			0.8	V
Logic Inputs INA, INB Frequency		F_{INA}, F_{INB}		0		250	kHz
Logic Inputs INA, INB Pulse Width[1)]		τ_{INA}, τ_{INB}		350			ns
INA vs. INB Pulse Width Distortion		t_{DST}			20		ns
Logic Inputs INA, INB Dead Time		t_{DEAD}			420		ns
RESTART Pulse Width		t_{RESET}		200			ns
FLT_RESET Pulse Width		t_{FLT_RESET}		200			ns
External Clock		F_{CLK}	Input From MCU	180	200	220	kHz
External Clock Duty Cycle		D_{CLK}		10		50	%
External Clock Watchdog Timeout		T_{DOG}	Information parameter only		40		µs
FAULT1, FAULT2 Output High Voltage		V_{FLTH}	I_{OUT} = 10 mA	V_{MCU}-0.20			V
FAULT1, FAULT2 Output Low Voltage		V_{FLTL}	I_{OUT} = 10 mA			0.20	V
ICM Comparator Threshold[2)]		V_{ICM_TR}		240	300	360	
ICM Comparator Blanking Time[3)]		T_{ICM_BL}		2	3.5	5	µs
ICM Comparator Response Time		T_{ICM_R}			150	250	ns
ICM Comparator Input Series Resistor		R_{ICM}		1	2	3	kΩ
IGBT Driver Output Voltage	High Level	V_{GH}			15		V
	Low Level	V_{GL}			-5		V
IGBT Driver Output Peak Sink/Source Current		I_G			±30		A
IGBT Driver Propagation Delay[5)]		T_{DPR}			365		ns
IGBT Driver Propagation Delay Time Mismatch[6)]		T_{DPR}			20		ns
Isolation Voltage Between Ground Pin and COM A Pin		V_{IS_GCA}		4			kV
Isolation Voltage Between Ground Pin and COM B Pin		V_{IS_GCB}		4			kV
Isolation Voltage Between COM A Pin and COM B Pin		V_{IS_CACB}		4			kV

Note:

1. INA signal overrides INB and τ_{INB} is reduced by t_{INDEAD} when INA overlaps INB
2. With respect to COM pin
3. Time from IGBT driver turn-on to turn-off measured with ICM terminal set at 500 mV with respect to COM pin
4. With respect to VEE pin of the appropriate driver
5. Measured as delay time between INA and INB activated/deactivated respectively to response by IGBT driver

Pin Configuration



Pin Assignment

CONNECTOR	PIN NUMBER	PIN NAME	FUNCTIONS
J1	1	+15 V	Supply voltage. Connect positive terminal of the +15 V supply source
	2	+3.3 V	Output voltage to drive external MCU. It can be disabled by the MODE pin set at logic high level, if the MCU is powered from a source other than module. In this case, the same external source should be used to drive IXIDM1403_1505_M internal logic.
	3	MODE	MODE = 0 V or left open activates internal +3.3 V voltage source. MODE pin set above +2.5 V disables internal source and an external source connected to +3.3 V pin will be used to operate internal logic[1)].
	4	FLT_RESET	Positive logic pulse at this pin resets flip-flops holding information about FAULT1 and FAULT2 conditions
	5	RESTART	Positive logic pulse at this input restarts module
	6	CLK	Logic input to provide external clock in case synchronization between internal power supplies of different modules is required. If no external clock is applied, internal clock will be used
	7	FAULT1	FAULT1 signal logic output
	8	FAULT2	FAULT1 signal logic output
	9	GROUND	Ground terminal for all power supplies and logic signals
	10	INB	Channel B gate driver logic input. If INB =1 and INA is active, complimentary pulses will be generated at GATE B output with a dead time ~400 ns.
	11	INA	Channel A gate driver logic input
	12	TS	Terminal to translate thermo sensor information from IGBT module to MCU. It is a direct connect to pin #1 of the connector J4
J2	1	GATE A	Gate driver A output. Connect to the gate of the IGBT A
	2		
	3	COM	Common terminal of the Gate driver A, Connect to IGBT A emitter or low potential terminal of the current sense resistor
	4		
	5	ICM	Over-current comparator's input. Connect to the high potential terminal of the current sense resistor/IGBT emitter. Connect to COM pin if unused
J3	1	GATE B	Gate driver B output. Connect to the gate of the IGBT B
	2		
	3	COM	Common terminal of the Gate driver B. Connect to IGBT B emitter or low potential terminal of the current sense resistor
	4		
	5	ICM	Over-current comparator's input. Connect to the high potential terminal of the current sense resistor/IGBT emitter. Connect to COM pin if unused
J4	1	TS	Terminal to translate thermo sensor information from IGBT module to MCU. Direct connect to pin #12 of the connector J1
	2	GND	Ground terminal for thermo sensor connection

Note:

1) If external +3.3 V supply is used to drive internal IX6610 logic, the power-up sequence should be implemented. Internal +3.3 V power supply should be active before the MODE pin is used to disable it, and only after that should the external voltage be applied to the +3.3 V pin. Power down sequence requires external +3.3 V removed first, after which the MODE pin should be set to logic zero or left open. The +15 V source can then be removed from IXIDM1403_1505_M.

Block Diagram

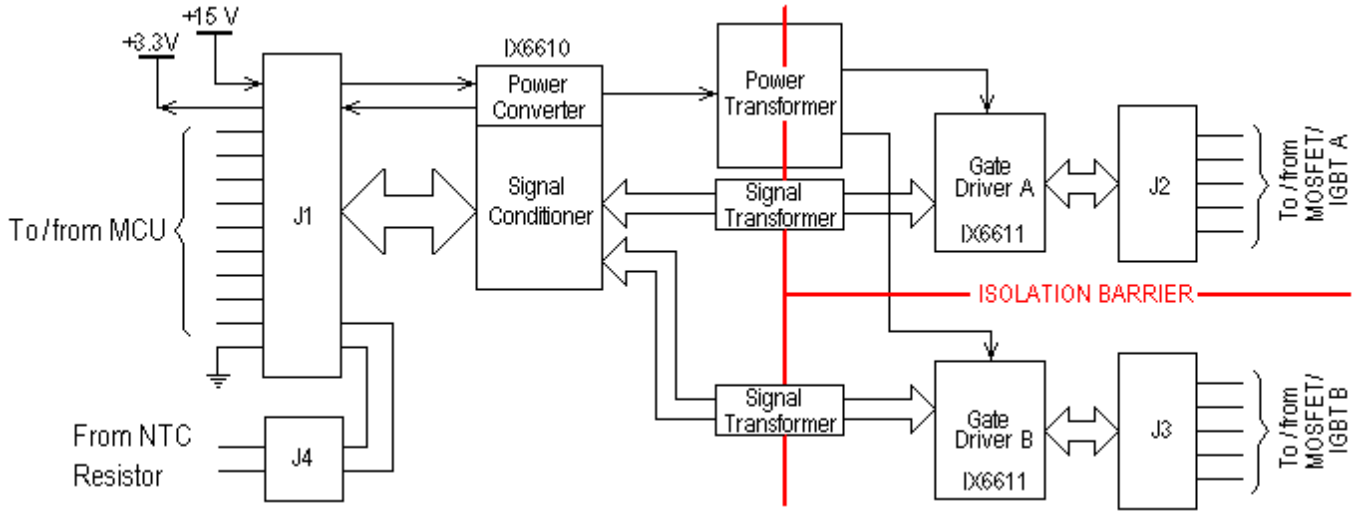


Figure 5. IXIDM1403_1505_M Block Diagram

Basic Operation

The IXIDM1403_1505_M device is based on the IX6610/IX6611 chipset, which enables the creation of an isolated IGBT driver with a high voltage isolation barrier between the primary and secondary side and between secondary side drivers. This creates a very flexible architecture, which can be used for 3-phase motor driver, half-bridge switches, push-pull converters, or other applications which require isolation between the primary and secondary side and/or between secondary side drivers.

This device contains the necessary circuit blocks to operate a bidirectional interface between the primary and secondary side and provide the power required to drive isolated gate drivers and the MCU from a single +15V power source, maintaining up to 4kV isolation between the MCU and gate drivers and also between gate drivers.

The IXIDM1403_1505_M module implements monitoring/protection functions such as +15V supply under-/over-voltage lockout, under-/over-voltage lockout on secondary side, and thermal shutdown. It also provides over-current protection on the secondary side and sends information to the MCU about such events to allow the MCU to make appropriate decisions.

The IX6610 is located on the primary side and implements a dual-channel bidirectional transformer interface, which transmits the primary side input commands from the MCU to the secondary side, and information from the secondary side to the MCU. Asynchronous data transmission is implemented by narrow pulses to prevent the transformer's core saturation. The IX6610 also contains all the blocks required to implement a power converter that supplies isolated power to the secondary side IGBT drivers. The IX6610 utilizes built-in inter-lock and dead time control.

Interface

TTL level compatible input signals INA and INB from an external MCU are used to operate secondary side drivers. These input signals are fed through the Schmitt trigger buffers to improve noise immunity. An input signal interlock function is implemented to prevent the simultaneous conduction of the secondary side IGBTs, with priority for the INA signal. If the INA signal is active (logic one), the INB signal is ignored irrespective of its logic state until the INA signal becomes logic zero and dead time expires.

This feature enables the generation of complimentary signals at Gate A and Gate B outputs using only one signal source applied to INA input, while INB input is set to logic high. Dead time between pulses at Gate A and Gate B outputs is hardware programmed to ~420 ns.

A narrow pulse detector is implemented in the IX6610 to prevent transmission of very narrow false PWM input signals to the drivers due to noise coupling at the input pins. Input signal pulses with width narrower than 100 ns are suppressed and pulses with width greater than 350 ns are transferred to the drivers.

In the half bridge driver configuration, dead time should be added to the incoming input signals, to prevent shoot through current due to overlap of the conducting state for high and low side IGBTs. If the dead time required to operate a particular IGBT is more than that implemented in IXIDM1403_1505_M, it should be programmed by the MCU. IX6610 also contains a dead time circuit that adds dead time to the input signals INA and INB after the input signal interlock function. This dead time is used as a precaution only in the instance of a software failure and it applies if the dead time programmed by the MCU is shorter than the dead time set by IXIDM1403_1505_M.

To avoid limitations to a transmitted maximum pulse width, IX6610 only transmits short pulses representing rising/falling edges of the INA (INB) signal, while IX6611 restores the original INA (INB) pulse width on the secondary side (see Figure 6).

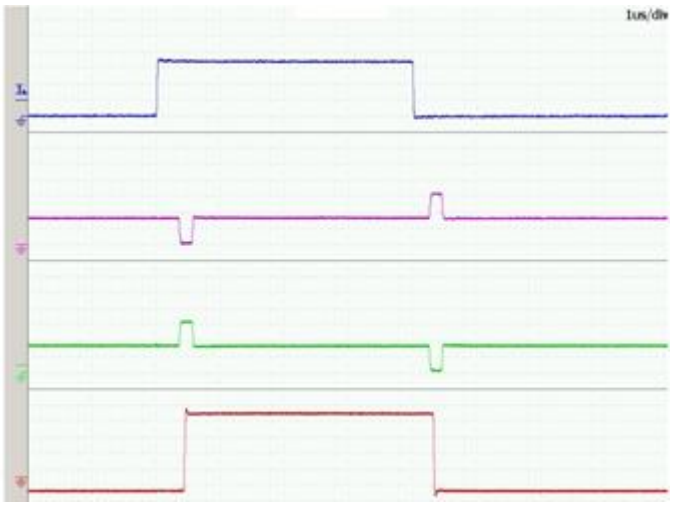


Figure 6. PWM Signal Transmission

Legend:

Channel 1 (blue) input signal (INA/INB) from MCU
Channel 2 (magenta) and Channel 3 (green) – IX6610 outputs
Channel 4 (red) – IGBT gate pulse at IX6611 output

The secondary side power supply faults and IGBT power stage faults are transmitted back to the IX6610 (primary side) through a pulse transformer. IX6610 has four single-ended receiver comparators which sense the presence of signals that are more positive than a fixed positive threshold value. Receiver comparators are high speed Schmitt Trigger buffers with 1 V typical hysteresis.

The truth table for Fault signals is listed in Table 1.

Table 1. Fault Signals Truth Table

Before FAULT RESET			After FAULT RESET			
FAULT1	FAULT2	Synchronized	FAULT1	FAULT2	SOURCE	SIGNAL
1	0	no	1	0	IX6610	Under-voltage
0	1	no	0	1	IX6610	Over-voltage
1	1	no	1	1	IX6610	Over-temperature
1	0	yes	0	0	IX6611	Under-voltage
0	1	yes	0	0	IX6611	Over-voltage
0	1	no	0	0	IX6611	Over-current

Fault signals generated by IX6610 are not synchronized with INA (INB) signals and cannot be reset by the MCU applying the FAULT RESET signal. They remain active so long as the fault condition exists. However, when the fault condition disappears, the FAULT flag remains active as .long as the MCU does not reset it.

Fault signals generated by IX6611 representing over-voltage and under-voltage conditions are synchronized with INA (INB) signals and are an echo of these signals, which appear at FAULT outputs immediately after an attempt to transmit the INA (INB) signal when a fault condition on the secondary side exists. Fault flags representing these faults can be reset by the MCU, but they reappear at the next attempt to transmit the INA (INB) signal, until the fault condition disappears. This allows the MCU to determine the source of the fault signals. The fault signal from IX6611 representing an over-current condition is not synchronized with the INA (INB) signal; however, the fault flag representing this condition can be reset by the MCU. It is reactivated if the over-current fault occurs at the next PWM cycle.

All fault conditions for IX6610 stop execution of the PWM cycle at both drivers. All fault conditions for IX6611 stop the PWM cycle at the affected driver only. Therefore, it is up to the MCU programmer to determine the next steps if a fault condition occurs. If fault conditions appear before the start of the PWM cycle, the PWM cycle will be ignored for the duration that fault conditions exist.

Power Block

The IXIDM1403_1505_M power block is designed to provide up to 2W of power to drive two IX6611 isolated gate drivers and an external MCU from a single +15V supply. IX6610 utilizes push-pull converter topology, which allows multiple isolated outputs, step-up/step-down and/or inverted outputs with low output ripple. The circuit drives two internal high current switches connected to an external center-tapped transformer providing dual isolated secondary side positive and negative voltages for the IGBT drivers and an isolated 5V supply to IX6610.

The power converter has a start-up mode and a run mode. In the start-up mode, the converter operates from the internal oscillator and activates only a portion of the power switches to reduce the dynamic current consumption/power dissipation. After start-up, the converter activates the power switches and goes into run mode. The run mode is held off ~1.28 ms. The transmit operation is also disabled during start-up mode to minimize current draw in the secondary. After run mode begins, it continues until a restart occurs, which returns the power converter to start-up mode. In the run mode, the power converter operates either from an internal or external MCU clock, if it exists. An external clock may be used to minimize noise interference between IXIDM1403_1505_M devices for multiphase applications such as motor drivers.

The Push-pull block repeats the duty cycle of the external clock that allows slight adjustment of secondary output voltage in case of over/under-voltage by varying the duty cycle. It is not recommended to use an external clock with DC_{EXT} greater than 0.5.

To prevent excessive power dissipation and potential failure of the IC due to fault clock, a watchdog timer is included. Whenever the external clock period exceeds the watchdog timeout (40 µs), the converter switches to the internal clock. IX6610 contains an internal LDO regulator with 3.3V output voltage to drive the MCU. The maximum load current at 50mA for 100 ms allows for easy MCU initialization.

If an external 3.3 V source is used to drive the MCU, the internal LDO regulator should be disabled by applying logic level to the MODE pin to prevent competition between regulators; however, an external 3.3 V should be used in this instance to drive IX6610 internal logic circuitry. The Mode pin has an internal pull-down resistor and can be left open with internal LDO active.

A logic high level at the RESTART pin disables the power converter, the LDO, initiates the power converter start-up sequence, and resets the fault flags. Holding RESTART low for a sufficient amount of time will lower the LDO voltage to a level that may initiate a POR sequence in the MCU. The RESTART pin has an internal 20 kΩ pull down resistor.

Gate Driver

The IX6611 used on the secondary side of IXIDM1403_1505_M is designed to provide gate drive for high power IGBTs, converting the incoming PWM logic signals into a +15 V/–5 V (with respect to COMMON) bipolar gate drive signal. Additional amplifying stage with the IXN630 driver is used to provide 30 A peak drive current capability.

Over-Current Protection

IX6611 contains an Over Current Comparator (OC COMP) with a 300 mV threshold with respect to the COMMON pin. IGBT over-current protection can be implemented either by using a low value current sense resistor, an IGBT with a secondary current sense output, or utilizing a de-saturation event (See Figures 2 and 3).

If an IGBT over-current fault occurs, the IGBT driver output is forced low for the remainder of the cycle. Normal operation resumes at the beginning of the next PWM gate drive cycle. A noise filter at the current sense input may be required due to low sense voltage. The IXIMD1403_1505_M ICM input has an internal 100 pF capacitor connected in parallel to the ICM; therefore, only a serial resistor can be added to create such a filter.

An IGBT over-current fault event can occur any time during the ON time of the gate drive signal. When an over-current event occurs, the Output Faults Pulse Generator creates a narrow 200 ns pulse that is used by the Fault Control Logic to communicate the fault condition to the MCU.

The OC comparator's input is grounded during the off time of the IGBT and remains grounded for 3.5 µs immediately after the IGBT turns on to prevent false tripping.

Traditional de-saturation protection can also be implemented using a large ratio resistive divider across the collector to emitter (See Figure 2). Resistive divider R1/R2 has two limitations regarding its value. Voltage drop across R2 should be above 300 mV to trigger the ICM comparator if the IGBT de-saturation event occurs and it should not exceed V_{CC} voltage, when IGBT is in OFF state. If it is physically impossible, a Zener diode should be used to prevent ICM comparator damage as shown in Figure 2, Z1.

Secondary Side Under–/Over-voltage Protection

IX6611 contains Under– and Over-voltage Lockout Comparators (UVLO and OVLO respectively) that monitor the positive power supply terminal. If, at the beginning of the PWM pulse, positive power supply voltage is below the UVLO threshold or above the OVLO threshold, the gate driver output is driven low and it skips that PWM pulse. However, if UVLO or OVLO conditions occur after PWM pulse start, these conditions are ignored until the next PWM pulse.

If the positive power supply recovers from the fault condition, normal operation resumes on the next PWM pulse. Fault information is communicated to the MCU as narrow pulses. Based on the type of fault, the fault control logic selects narrow pulses either from the input interface or from the output fault pulse generator.

A UVLO fault condition is communicated to the MCU as an FLT1 pulse that is an input interface pulse representing the leading edge of the PWM pulse delayed by IX6611 propagation delay time. The OVLO fault condition is communicated to the MCU as an FLT2 pulse that is an input interface pulse representing the trailing edge of the PWM pulse, also delayed by the IX6611 propagation delay time. The IGBT over-current condition is communicated

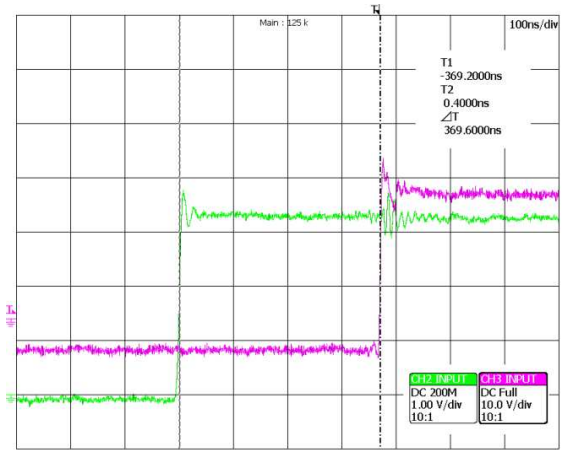
to the MCU as an FLT2 pulse from the internal output fault pulse generator, which is synchronized with an over-current event, but not leading/trailing edges of the input PWM signal.

Layout and Use Considerations

- Place external components as close to the package as possible and use thick, short connecting traces to reduce the circuit impedance.
- Pay special attention to the separation of isolated circuits to implement creepage distance limits for high voltage applications.
- Switching noise, which occurs from the GND, may cause instability; therefore, position blocking capacitors at the +15 V source as close to IXIMD1403_1505_M as possible.
- The absolute maximum ratings of the module and external components should not be exceeded.
- The thermal sensor's inputs are not isolated from the primary side and its ground terminal is a direct connection to the IXIMD1403_1505_M ground terminal.
- To prevent ESD damage to the module, install a 220 pF–470 pF ceramic capacitor with breakdown voltage above the isolation barrier voltage between the primary and secondary side ground terminals.

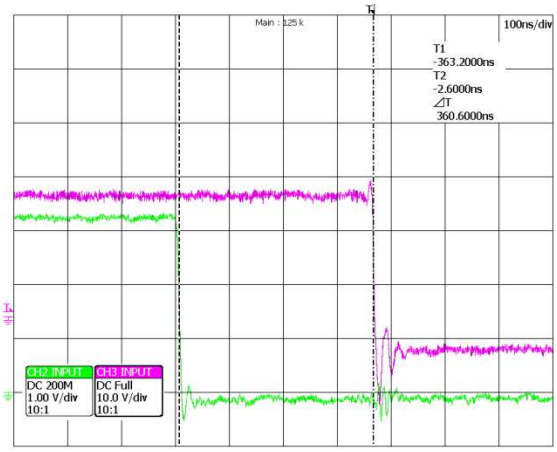
Typical Performance Characteristics

Figure 7 (a). Channel A Propagation Delay Time Rising Edge



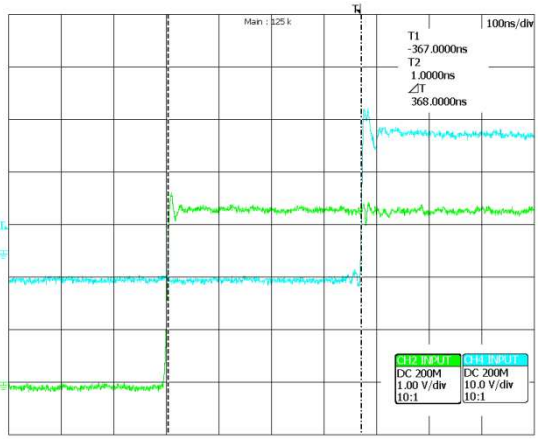
Channel 1– INA signal, Chaanel2 – Gate A signal

Figure 7 (b). Channel A Propagation Delay Time Falling Edge



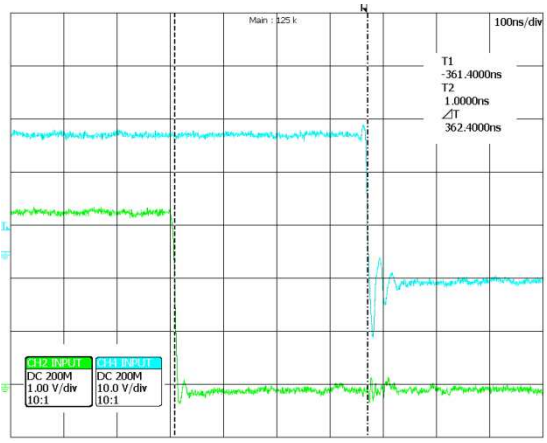
Channel 1– INA signal, Chaanel2 – Gate A signal

Figure 8 (a). Channel B Propagation Delay Time Rising Edge



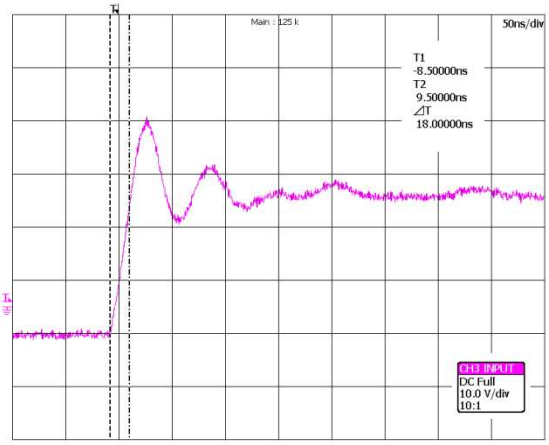
Channel 1– INB signal, Chaanel3 – Gate B signal

Figure 8 (b). Channel B Propagation Delay Time Falling Edge



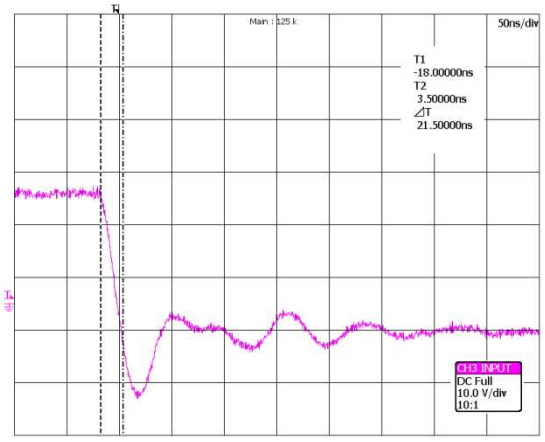
Channel 1– INB signal, Chaanel3 – Gate B signal

Figure 9 (a). Channel A Rising Time from 0 V to Vcc



Rgate = 1 Ohm, Cgs = 10 nF

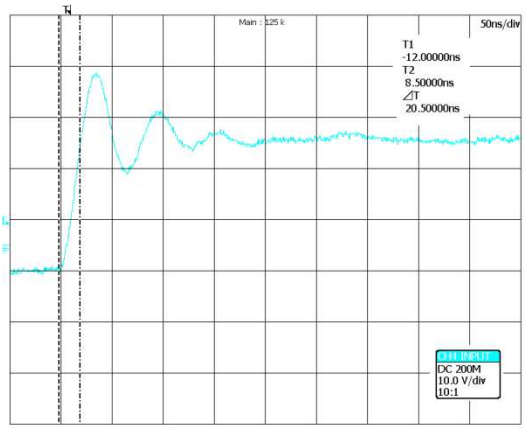
Figure 9 (b). Channel A Falling Time from Vcc to 0 V



Rgate = 1 Ohm, Cgs = 10 nF

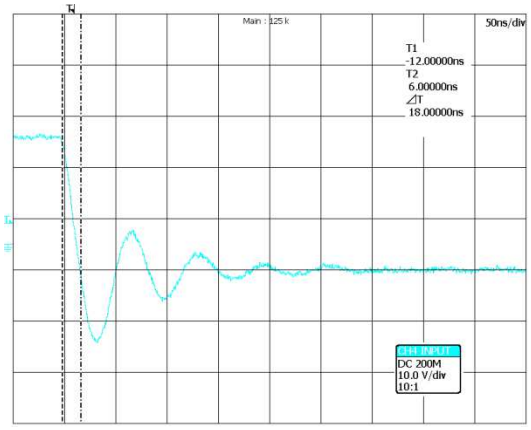
Typical Performance Characteristics (Continued)

Figure 10 (a). Channel B Rising Time from 0 V to Vcc



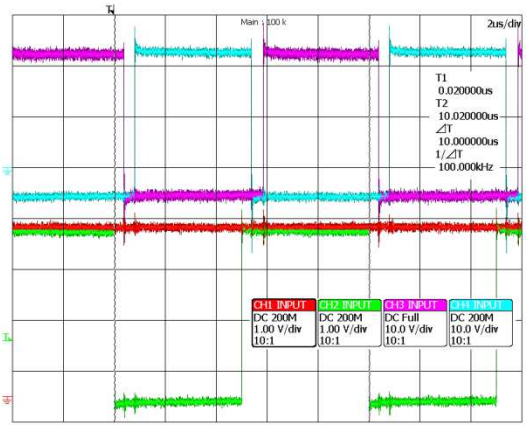
Rgate = 1 Ohm, Cgs = 10 nF

Figure 10 (b). Channel B Falling Time from Vcc to 0 V



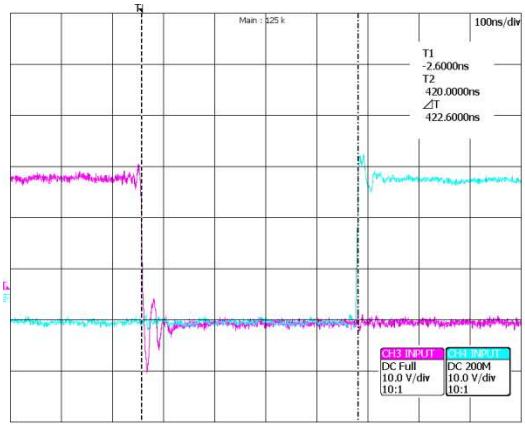
Rgate = 1 Ohm, Cgs = 10 nF

Figure 11 (a). Complementary Signal at Channel B with Both Channels Active



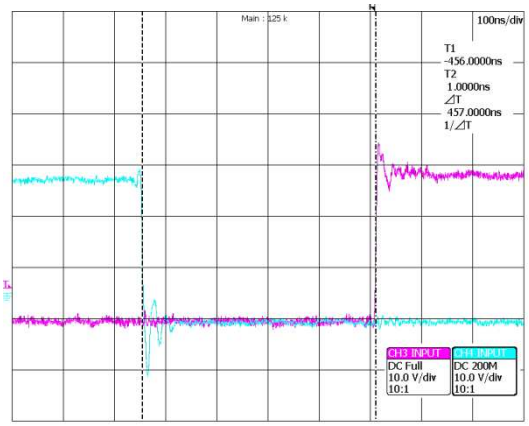
f_{sw} = 100 kHz, DC = 50%, INB = HIGH
Channel 2– Gate A signal, Channel 3 – Gate B signal

Figure 11 (b). Complementary Signal Dead Time Channel A to Channel B



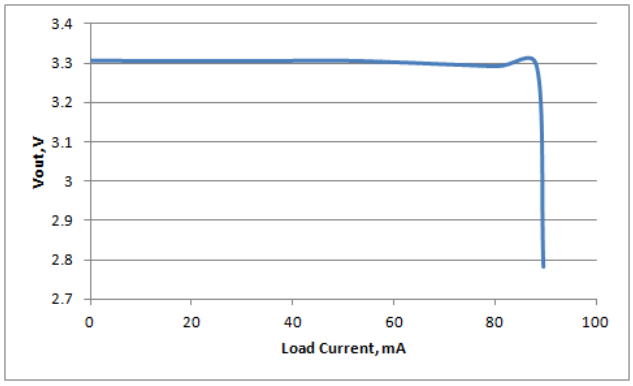
f_{sw} = 100 kHz, DC = 50%, INB = HIGH
Channel 2 – Gate A signal, Channel 3 – Gate B signal

Figure 12. Complementary Signal Dead Time Channel B to Channel A



f_{sw} = 100 kHz, DC = 50%, INB = HIGH
Channel 2 – Gate A signal, Channel 3 – Gate B signal

Figure 13. 3.3 V Supply Power Capability



Typical Performance Characteristics (Continued)

Figure 14. Gate Logic 1 Voltage vs. Switching Frequency

DC = 50%, Rgate = 1 Ohm, C_{GS} = 10 nF

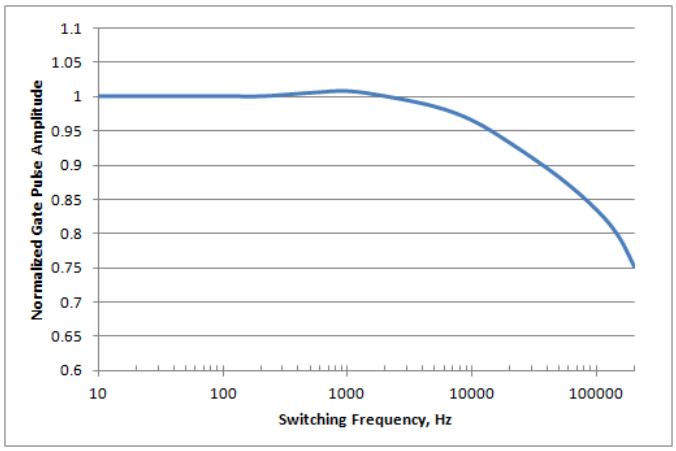


Figure 15. Gate Logic 0 Voltage vs. Switching Frequency

DC = 50%, Rgate = 1 Ohm, C_{GS} = 10 nF

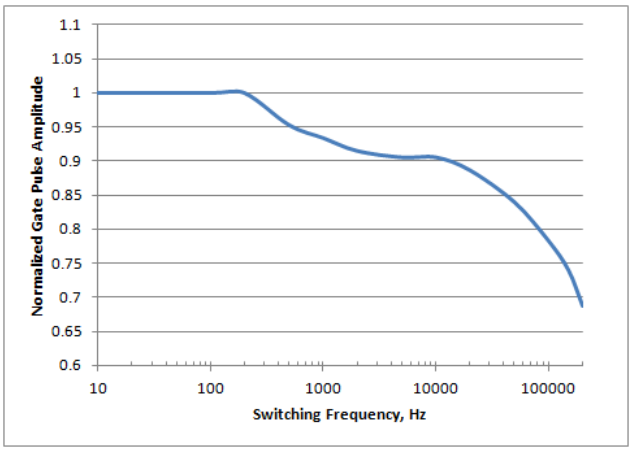


Figure 16. Gate Logic 1 Voltage vs. Power Supply Voltage

f_{sw} = 100 Hz DC = 50%, Rgate = 1 Ohm, C_{GS} = 10 nF

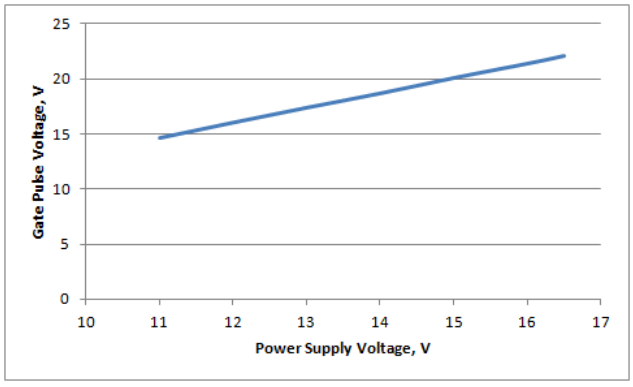
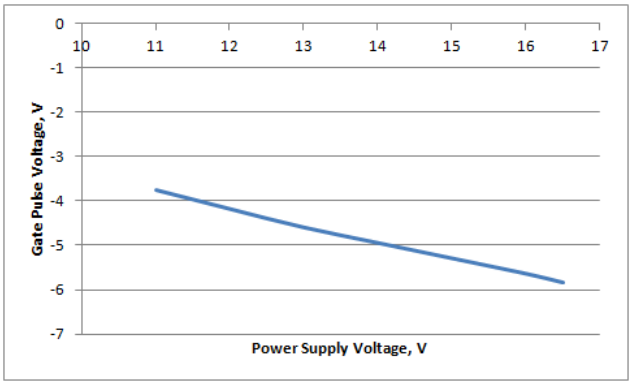


Figure 17. Gate Logic 0 Voltage vs. Power Supply Voltage

f_{sw} = 100 Hz DC = 50%, Rgate = 1 Ohm, C_{GS} = 10 nF



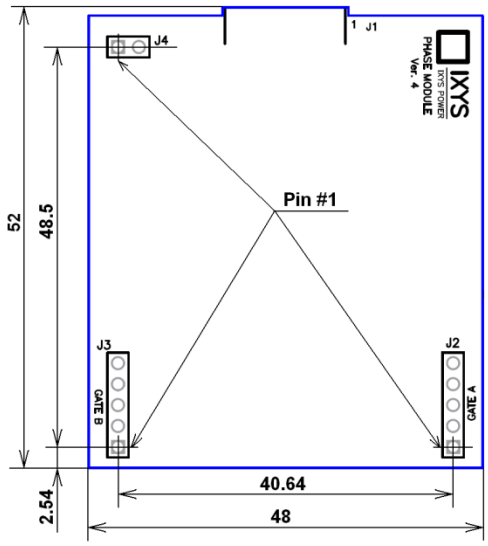
Ordering Information

IXIDM①②③④_⑤⑥⑦⑧_⑨

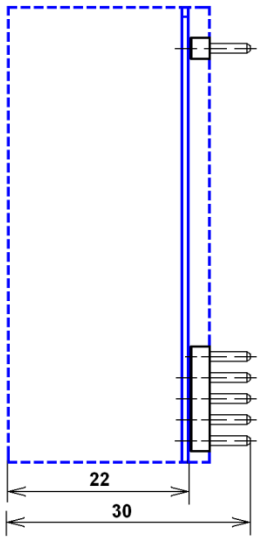
DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Module Configuration	1	Two Isolated Gate Drivers
②③	Isolation Voltage	40	4.0kV
④	Gate Current	3	30A
⑤⑥	Positive Gate Voltage	15	15V
⑦⑧	Negative Gate Voltage	05	– 5V
⑦⑧	Negative Gate Voltage	15	– 15V
⑨	Package Information		O – Open Frame; M – Molded

Package Drawing and Dimensions

Units: mm

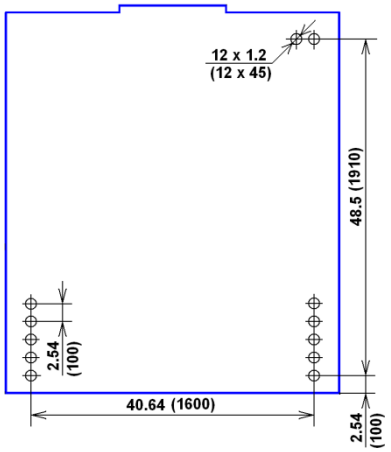


Bottom View



Side View

Units: mm (mil)



Recommended Footprint (Component Side View)

Marking

IXYS POWER

IXIDM1403_1505_M

XXYYWW

XX - Represents production lot number

YY – Represents production year

WW – Represents work week

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