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High Power Digital Inrush Current Controller

Reference Design
IXRD100201-1015

Overview

This High Power Digital Inrush Current Controller reference design extends IXYS' Digital Power Control technology to high current levels and introduces high current MOSFETs with current mirror sensors. The concept of digital inrush current control is discussed in an earlier reference design (IXRD1001, available on ixys.net and zilog.com). High power digital inrush current control is also based on Zilog's 8-bit Z8F3281 microcontroller, a member of the Z8 Encore! XP F6482 Series of MCUs, and IXYS power transistors and rectifiers.

The primary differentiator between these two reference designs is the development-specific timing for pre-charging of the capacitor and the use of high-current IXYS transistors and rectifiers in the High Power Digital Inrush Current Controller reference design. The capacitor is charged according to a time-dependent pulse train. Pulses are designed to provide substantially equal voltage increment applied to the capacitor to maintain peak charging current at approximately the same value at each cycle. The number of cycles depends on the capacitor value and limitations to charge current. For higher load current, the capacitor value is larger to provide the desired amplitude of ripples; therefore, pre-charge may be longer to maintain the charge current within limits.

This High Power Digital Inrush Current Controller reference design is suitable for load currents up to 10A. The load current may be substantially increased, considering that the MOSFETs used are rated at 120A DC and a serial sensor resistor is not present. The main components to be changed include a bridge rectifier, an inductor with the appropriate current rating, and a current mirror sensor resistor.

This reference design features programmable overload protection and the Power Good status signal. Optionally, the Power Good signal may be used to connect/disconnect the load using N-channel MOSFET. The controller is not sensitive to power outages, brownouts, and ambient temperature variations. This reference design has the ability to operate within an input voltage range of 80 V–240 V AC. Overload protection is programmable and is set to 12 A. The entire operation process and essential values are fully programmable. The controller may be programmed to 50 Hz, 60 Hz, or any other line input frequency operation.

The High Power Digital Inrush Current Controller reference design is relevant for high power loads with tens of amperes of current at normal operation. It allows users to optimize performance, maximize efficiency across the load range, and reduce the design time to market. IXYS power components handle the pre-charge of load capacitors at these values, while limiting inrush current to controlled values.

Note: The source code file associated with this reference design, IXRD1002-SC01.zip, is available free for download from the IXYS Power and Zilog websites (www.ixyspower.com and www.zilog.com). This source code is tested with ZDS II – Z8 Encore! v5.2.0. Subsequent releases of ZDS II may require you to modify the code supplied with this reference design.

Features

The High Power Digital Inrush Current Controller reference design offers the following features:

- Input voltage range from 80 V to 240 V RMS
- Steady load current up to 10 A
- Programmable overload protection
- Power Good status signal High endurance
- Not sensitive to power outage or brownout
- Not sensitive to ambient temperature variations
- Voltage ripples 12% at 10 A load current and output capacitance of 3000 µF

Potential Applications

This reference design provides a basis for developing a variety of power management applications using IXYS power devices and an MCU, including the following applications:

- High Current AC– DC Rectifier
- High Current AC– DC PFC Converter

Principles of Operation

The principles of operation are fully described in the basic reference design, IXRD1001. The High Power reference design is differentiated by the use of components with higher power ratings and an appropriate change in the pulse train controlling the pre-charge of load capacitors. The pulse train is designed to limit pre-charge current to a level acceptable to ratings of used components. The limiting component in this particular design is the inductor AGP4233-223ME rated to 35.4 A at 20% inductance drop.

As shown in IXRD1001, the following equation was used to determine the timing position of each pre-charging pulse:

$$T_{on(i)} = \frac{T}{\pi/2}\,\mathbf{asin}\,(i/N), \quad \textit{where } i = 1 \ldots N \qquad (1)$$

Increments in the timing position of adjacent pulses define the amplitude of the charging voltage applied to the bulk capacitor. Increasing the number of pulses N reduces the charging voltage, thereby reducing the steps in the charging voltage. In the above example, N = 255, resulting in current limitation to 34 A with a capacitor value of 3000 uF.

The capacitor's voltage and charging current graphs are shown in Figure 1. The amplitude of the pre-charge current drops to the end of the charging cycle, while the capacitor's voltage rises linearly. It is determined by the timing position of current pulses in respect to the half sine waveform of the rectified voltage. At the end of the charging cycle, the duration of the pre-charging pulse is longer, with lesser current amplitude, which creates the same charge at the bulk capacitor as at the start and results in identical capacitor voltage steps during the entire cycle.

Figure 2 and Figure 3 show different waveforms of pre-charging current. Figure 2 depicts pre-charging current at the beginning of the charging train, while Figure 3 depicts pre-charging current at its end.

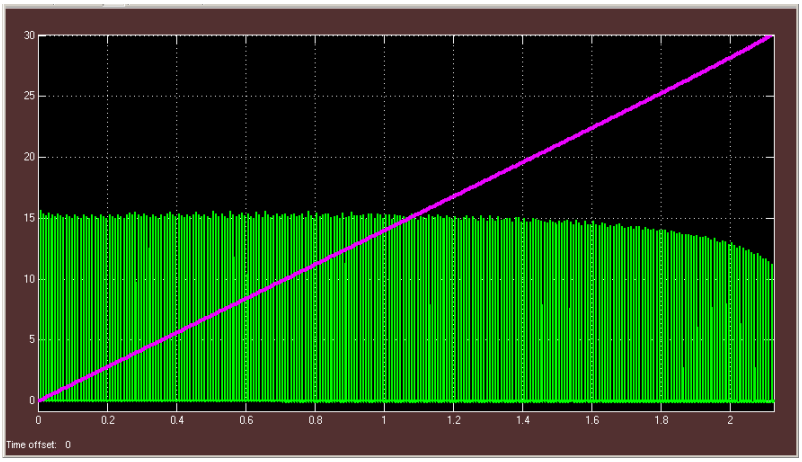

Figure 1: Voltage on the Capacitor and Charging Current

Legend: (Not to scale)
Magenta – Voltage on the capacitor
Green – Pre-charging current

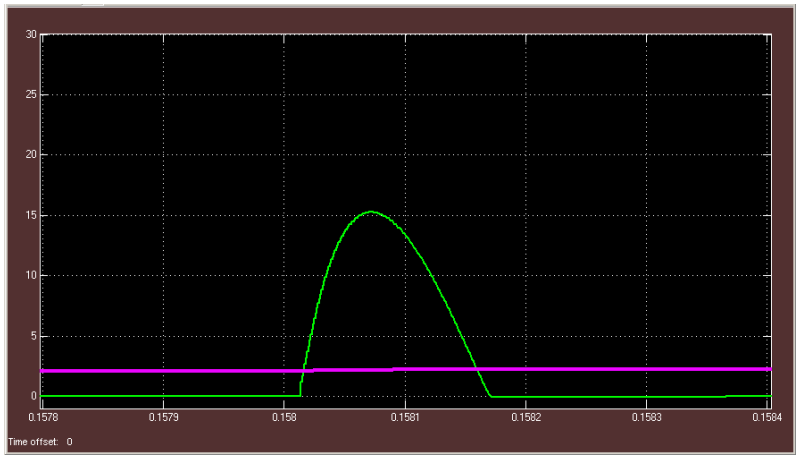

Figure 2. Pre-charge Current at the Start of the Charging Cycle

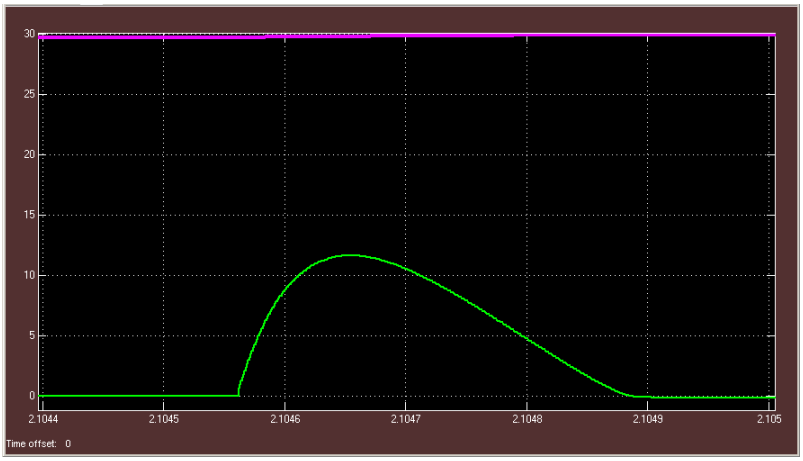

Figure 3. Pre-charge Current at the End of the Charging Cycle

Service Functions

This reference design displays the capabilities of IXYS power components by featuring a Load ON/OFF switch U2 (see Figure 8), Overload Protection functionality, and Power Good status output. Load switch activation is programmable, and is enabled after the capacitor C pre-charge is completed. Load Switch is activated with Power Good status signal in this reference design.

Overload Protection is an important feature to protect a device from being destroyed when an overload occurs. The overload threshold is programmable, and is set to 12A in this reference design. If overload is detected by a comparator, the MCU disconnects the load by turning U2 and U3 off.

Overload protection can be programmed in one of the following ways:

- Immediately shut down the device and wait for user action
- Allow the device to restart after the short circuit is removed, for a predetermined number of short circuit occurrences.

When the device is allowed to restart, the delay between restarts and the number of restarts is programmable. In this reference design, delay time is set to 1.5 seconds and the number of restarts is set to 4.

Power Good status activation is programmable. In this reference design, it is delayed by one AC voltage period after the capacitor's pre-charge is completed. The Power Good status is not set if overload is detected.

Hardware Implementation

The IXYS High Power Digital Inrush Current Controller, which consists of an MCU Module and a Main Power Board, is shown in Figure 4. The detailed circuit schematics are included in Appendix A. The MCU Module is implemented as an add-on device. This module comprises of a connector for MCU programming. The MCU should be programmed before powering the entire system. The MCU Module is powered by an auxiliary power supply (+3.3V for the MCU and 12V for the gate driver applied to the connector J4 on the Main Power Board).

The Main Power Board is a two-layer surface-mount device that provides easy access to test points. Diode Bridge BR1 (see Appendix A for schematic) and MOSFETs U2 and U3 are mounted on the main power board. Power dissipated on these MOSFETs is less than 5 W at a 3000 W output power. This board may be powered from a 50 Hz or 60 Hz 120 V or 240 V AC source.

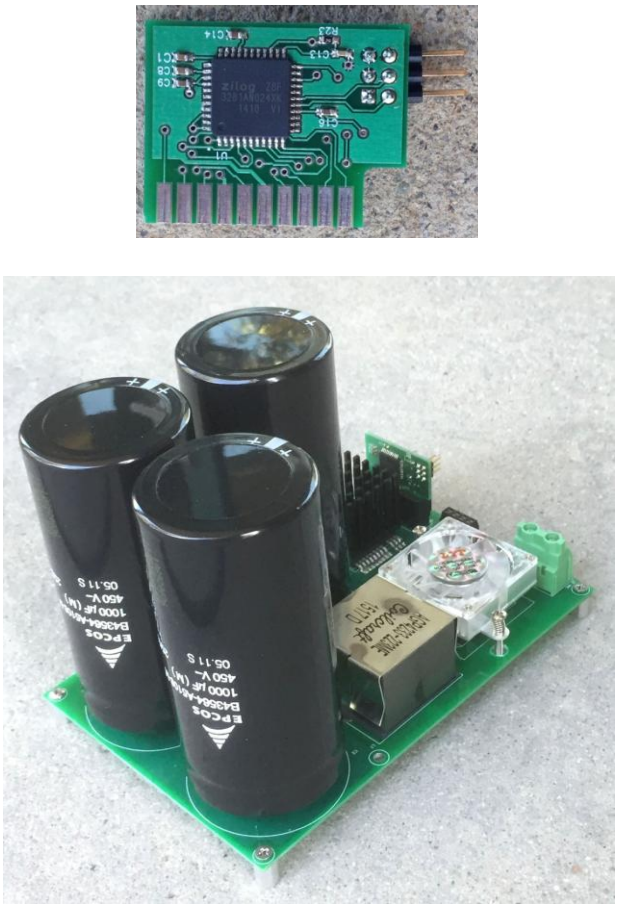

Figure 4. MCU Module and Main Power Board with MCU Module

Setup and Test Results

This reference design was programmed and its performance verified on a test bench, as shown in Figure 5. The AC line input was fed through a 2 kW isolation transformer for test equipment and operator's protection. The load was set to consume 10A during normal operation. To test overload conditions, an additional load was used to add 2A current. An instantaneous connection of additional load was enough to

trigger overload protection. Continuous overload results in multiple attempts to restart the device with immediate interruption after load current meets the 12A threshold.

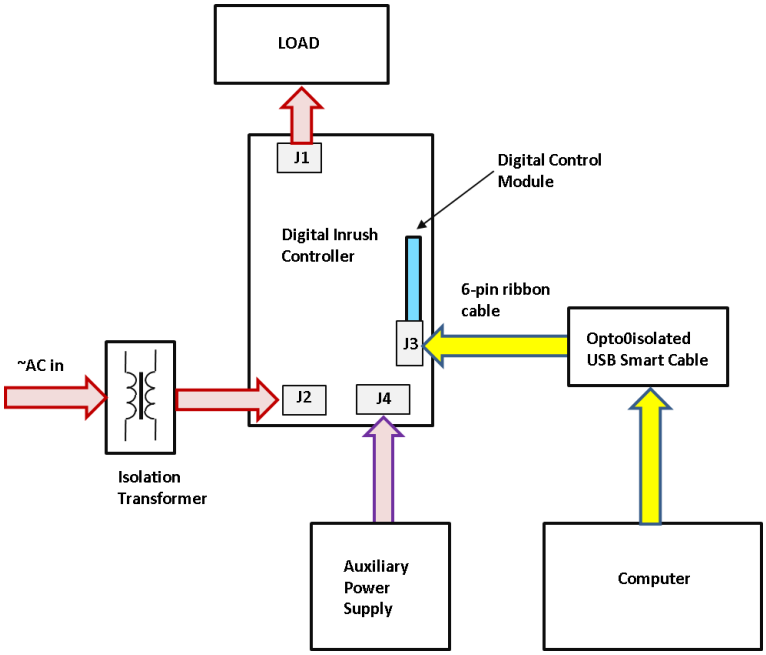

Figure 5. Digital Inrush Controller Setup

The auxiliary power supply should be turned ON after the AC power is ON. After a power-on reset and initialization, the MCU analyzes the power line, sets an appropriate timing, and begins pre-charging the bulk capacitor. Actual waveforms taken from a scope at the normal operation are depicted in Figure 6.

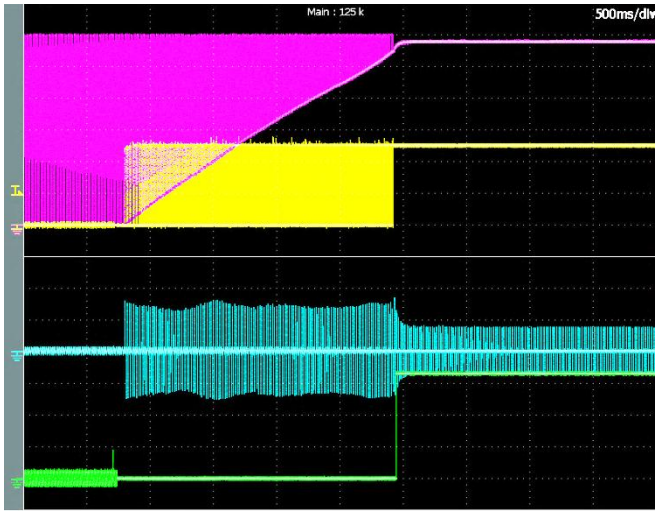

Figure 6. Scope Snapshot of the Digital Inrush Current Control

Legend (Not to scale):

Blue – Power line current (10A/div)
Red – Load voltage (50V/div)
Yellow – U2 control signal
Green – Power Good status signal (1V/div)

The inrush current (blue line) is limited to 16 A. The yellow line shows the signal at the U2 gate. After the inrush procedure is completed, the gate is set to a high level for U2 to continue conducting. The load is then connected to the pre-charged capacitor. A drop in the rectified voltage after the load is connected occurs due to the impedance of the isolation transformer and power grid.

Performance at Overload Conditions

Normal operation starts with pre-charging the bulk capacitor. If an overload condition is detected by the MCU, the normal operation is interrupted and the U2 and U3 switches are turned off. An attempt to restart the device is initiated in 1.5 second intervals. If the overload condition persists, the device is shut down again. The number of restart attempts is programmable and is initially set to 4 in this design.

Efficiency

The efficiency of the High Power Digital Inrush Current Controller is estimated, starting after the diode rectifier to the load. At a load power of 1000 W, the power loss is 6 W, which equates to an efficiency of 99.4%.

Device Configuration and Control Setup

This reference design can be configured for different parameters such as input voltage and frequency range, overload threshold, overload recovery time, number of overload events before shutdown, and time position for Power Good status signal.

The firmware that controls the operations of this High Power Digital Inrush Current Controller reference design was developed using Zilog's Development Studio II (ZDS II – Z8 Encore! version 5.2.0). The following hardware components were used during the development of this reference design:

- USB SmartCable – provides communication with ZDS II – Z8 Encore! version 5.2.0, debugging and downloading code into the F3281 MCU
- Connector J5 2x3, straight male header

Note: When connecting either device to the Reference Design Board, always ensure that pin 1 of the programming cable and pin 1 of the connector on the Digital Control Module are lined up.

Software Implementation

The source code for this application, IXYS_IXRD1002.zip, is available free for download from the Zilog website. This section describes the programs included in the source code.

Main.c file:

To limit the inrush current upon system power up, this program utilizes Look-up Tables (LUT) containing values based on characterization from a simulation model to charge the bulk capacitor which is connected to the load after the capacitor charging process has completed.

If an overcurrent condition occurs, the comparator shuts down the system and restarts the inrush current control after the expiry of a user-defined period of time. In this reference design, the waiting time is set to 1.5 seconds. If the overcurrent condition persists after the specified number of restart attempts, the system is held in the OFF state.

The program implements a comparator and three timers to generate the current limiting pulse trains, which consist of on and off times that are based on these LUT values. Each of these on/off pulses is applied to the U2 switch of the inrush current limit circuit, thereby limiting the current of the circuit. The main purpose of the comparators and timers is to place the current limiting pulse train so that the pulses are aligned to a certain position of the rectified power input sine wave.

The pulse train alignment is achieved by the use of a comparator and a timer which measures the zero crossing events of the input power sine wave. The pulse train is then synchronized with the zero crossing events and is located toward the falling slope of the rectified sine wave.

Upon power up, the first user-definable sine wave cycles are ignored to allow the system to stabilize before measuring the sine wave periods and zero-crossings. The next two sine wave periods are measured using the comparator's falling edge and multichannel Timer 1 and stored as the variable, T_period. However, this variable is not implemented; instead, a macro containing the ideal value for either 50 Hz or 60 Hz is used. The macro can be changed so that the measured values can be implemented if required.

The next four input power sine cycles are used to determine the zero crossing events by measuring the time period from the sine's falling slope to the sine's rising slope at a 0.7 V comparator interrupt threshold. Multichannel Timer 1 is used to measure the lapsed time between the two comparator interrupt events. When the measurement is completed, the zero crossing is determined to be half of the measured time.

After the above information is collected, timer1 and timer2 are configured in triggered one-shot mode. Timer 2 is loaded with the power input sine period value minus the *inrushCurrentOffTime* value from the LUT, minus the measured zero-cross time and a zero-cross compensation value. This result becomes the *on-time*. The zero-cross compensation value is used to "fine-adjust" the pulse train alignment with the power input sine wave. Timer 2 is triggered upon the comparator's rising edge interrupt. Upon expiry of Timer 2, the gate of the input switch MOSFET is enabled and timer1 is triggered. Upon expiry of timer1, the input switch MOSFET is disabled again.

This process repeats until all the values from the LUT have been used. Up to this point, the capacitors have been charged, while the actual load remains disconnected. After the inrush current process for the capacitors is completed, the actual load is activated one input power sine cycle later. A Power Good signal is generated after the procedure for charging of bulk capacitor is completed.

Main.h file

This file contains the function prototypes, structures, and macro definitions. The inrush current limit can be selected for 120 V/60 Hz, 240 V/60 Hz, and 220 V/50 Hz systems.

Power is selected by commenting and un-commenting macros in the following manner:

- If the ONEHUNDRED_TWENTY macro is uncommented, then 120 V/60 Hz is selected.
- If the ONEHUNDRED_TWENTY and TWOHUNDRED_TWENTY_VOLT_50HZ macros are commented out, then 240 V/60 Hz is selected, else 220 V/60 Hz is selected.

The LUT size and values depend on the load capacitor's value. The user is provided with a formula to calculate new LUT values if the load capacitor is changed. These new values should be loaded in the look-up table instead of using the default values. However, the size of the new table may differ from the original size; therefore, the INDEX macro must be adjusted to reflect the new LUT size.

The RC_DLY_OFFSET_50HZ macro is used to fine-adjust the pulse train to the left on the x-axis of the input power sine wave to achieve a more linear charging characteristic.

Initialization.c file

This file contains the peripheral setup for:

- System clock
- Operational amplifier
- ADC
- Multichannel timers
- General purpose timers
- Comparators

Equipment Used

The following equipment was used to build and test this reference design:

- Laboratory DC Power Supply – GPS-4303
- Scope – Yokogawa DL9140
- Multimeter – FLUKE-179
- Isolation Transformer – 2000W

See Appendix C. Bill of Materials for a list of materials used to build this reference design.

Kit Contents

This High Power Digital Inrush Controller Reference Design Kit contains the following items:

- Digital Inrush Current Controller Reference Design Block
- Opto-isolated USB SmartCable
- Digital Inrush Current Controller Reference Design Kit Insert (FL0182)

Ordering Information

The products associated with this Digital Inrush Controller Reference Design can be ordered from the IXYS Store or the Zilog Store using the part number listed below.

Part Number	Description	Store Product ID
IXRD1002	High Power Digital Inrush Controller Reference Design Kit	RD10042

Results

Testing of this design confirmed that the inrush current is limited to a predefined value and the performance of the limiter is quite close to the simulation results. The measured efficiency of the inrush control path is 99.4%. The device is capable of working with a wide range of input voltages from 80 V to 240 V. The tested power line frequency range was 60 Hz. A dedicated control pulse train was developed for 240 V input line voltage and load capacitance of 3000 uF. The inrush current is limited to 15A when maximum of input voltage is applied.

Overload protection is based on continuous monitoring of dynamic current from the bulk capacitor. When overload occurs, the current drawn from the capacitor instantly increases and triples the comparator, thereby initiating a system overload mode. The values for overload current threshold, number of overload instances, and period between overload events are programmable. The option to turn the load ON/OFF helps the overload mode of operation by disconnecting the load. Power Good status is not available in overload conditions. The digital overload protection device is not sensitive to power interruptions, brownouts, and temperature variations.

The primary features of the system include:

- Inrush current is limited to a predefined value
- High efficiency in the range of 99.4%
- Wide input voltage range – 80 V to 240 V
- Wide input frequency range – 50/60/400Hz
- Option to turn the load ON/OFF
  - Load current is 12 A
  - Overload current is set to 12 A
- Programmable overload protection – overload current threshold, number of overload instances, period between overload events
- Power Good status; not available during overload conditions
- Not sensitive to power interruptions or brownouts
- Not sensitive to temperature variations
- High endurance

Summary

This High Power Digital Inrush Current Controller is the second digital power device based on Zilog's Z8 Encore! XP F6482 Series of MCUs that offers flexibility in implementing a unique control algorithm to help development of efficient power systems. This reference design achieves a high level of efficiency, increased stability, and reliable performance across a wide range of loads. Use of a switching transistor with current mirror for current measurement algorithm allows for implementation of current measurement without a sensor resistor in the main current path. Users can optimize the device for a wide range of input voltages and frequencies. This design provides instant overcurrent protection, followed by an intervention by the MCU for corrective action.

This device can be used as part of an AC-DC rectifier or can be expanded to higher level devices such as a PFC converter. Digital control can be used to build a user interface that would allow users to change device parameters, gather statistics, add a communication interface, remotely monitor performance, or change parameters.

Related Documentation

Documents associated with this reference design are listed below. Each of the linked documents in this table can be obtained from the IXYS or Zilog websites by clicking the link associated with its Document Number.

Document Number	Document Description
IXRD1002	This High Power Digital Inrush Current Controller Reference Design document
IXRD1002-SC01	Source code for this High Power Digital Inrush Current Controller Reference Design
IXRD1001	Digital Inrush Current Controller Reference Design document
IXRD1001-SC01	Source code for the Digital Inrush Current Controller Reference Design
PS0294	F6482 Series General-Purpose Flash Microcontroller Product Specification
UM0263	F6482 Series Development Kit User Manual
UM0181	USB SmartCable User Manual
RM0064	F6482 Series API Programmer's Reference Manual

Appendix A. Schematic Diagrams

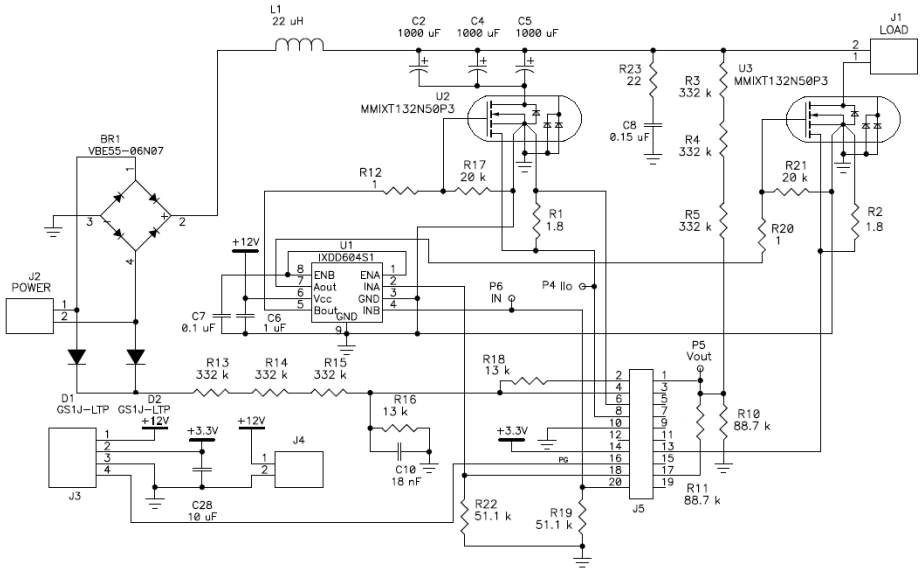

Figure 7. Schematic Diagram of the Digital Inrush Controller Main Board

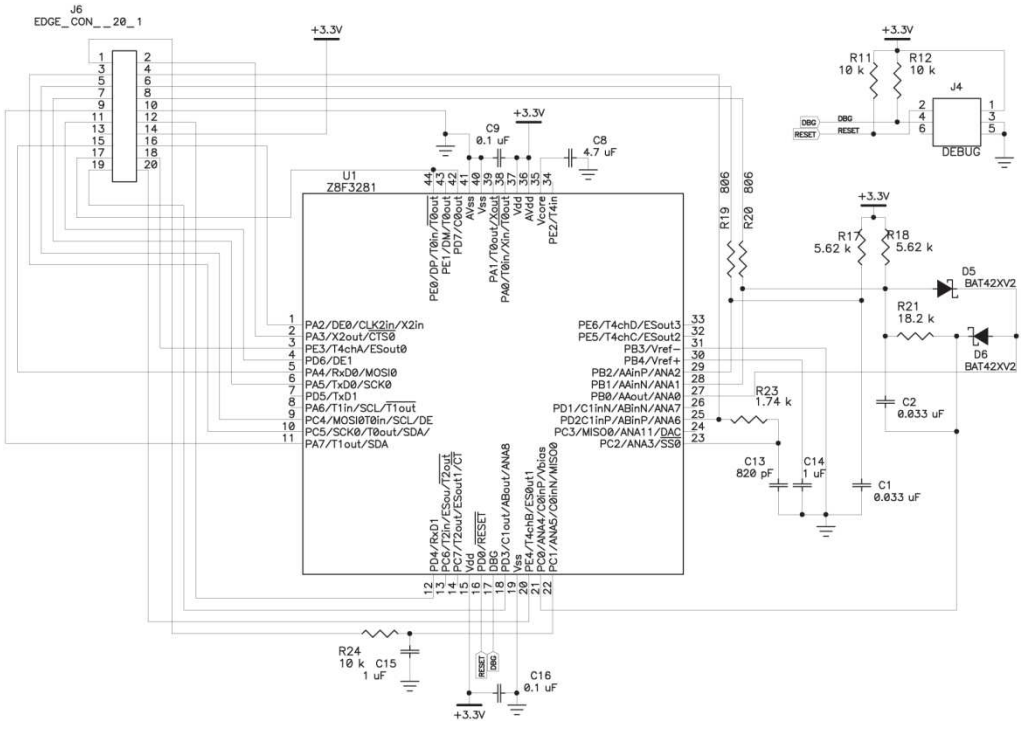

Figure 8. Schematic Diagram of the Digital Control Module

Appendix B. Board Components

Figure 9 displays the location of the components on the Digital Inrush Controller Reference Design Board. Figure 10. Layout of Digital Control Module (Top and Bottom Layers)Figure 10 indicates the location of power components and the MCU on the Board.

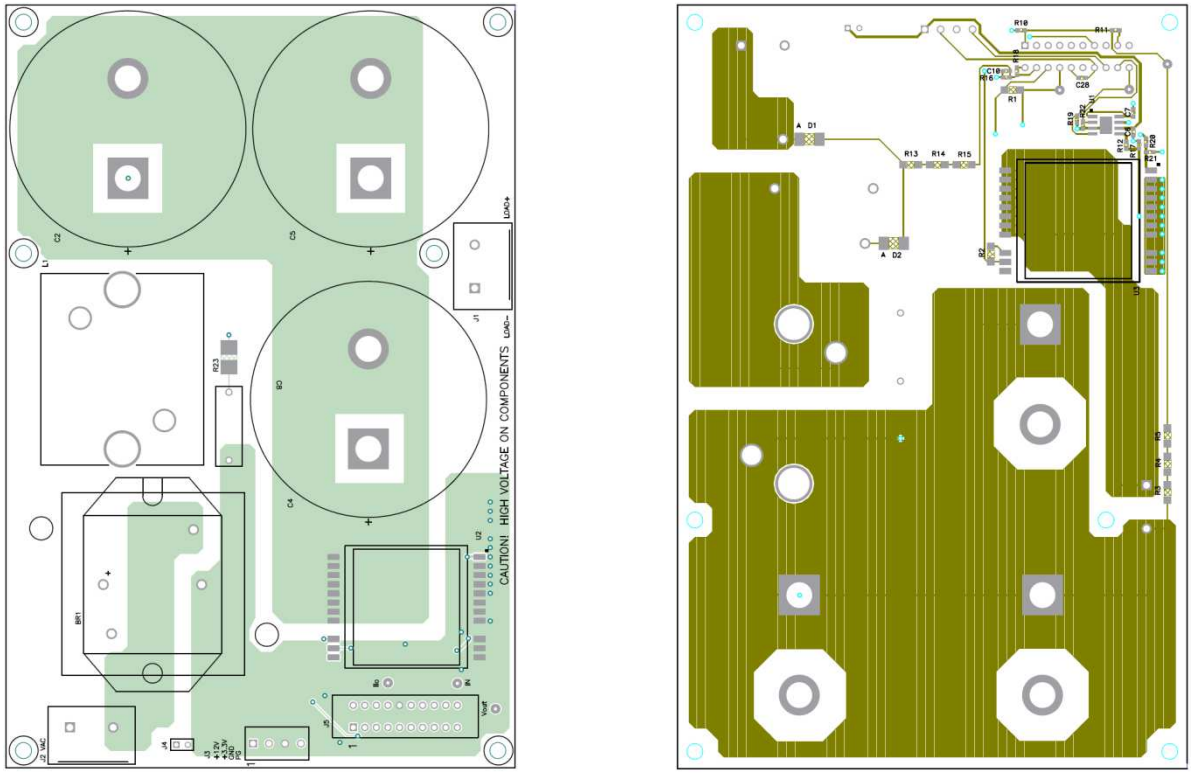

Figure 9. Main Board Layout (Top and Bottom Layers)

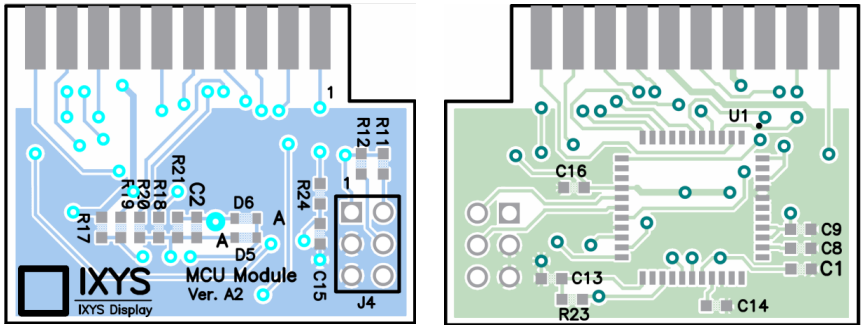

Figure 10. Layout of Digital Control Module (Top and Bottom Layers)

Appendix C. Bill of Materials

Table 1 and Table 2 list the components used to build this reference design.

Table 1. Main Board Components

Count	Reference Designator	Value	Description	Manufacturer
1	BR1	VBE55-06N07	VBE55-06N07 with heatsink VGA Card GPU Cooler	IXYS Corp
3	C2, C4, C5	1000 µF	B43564A5108M	EPCOS (TDK)
1	C8	0.15 uF	R46KI315000M2K	Kemet
1	C7	0.1 uF	CL10B104KA8NNNC	Samsung
1	C6	1 uF	TMK107B7105KA-T	Taiyo Yuden
1	C28	10 uF	CL10A106MA8NRNC	Samsung
1	C10	33 nF	C1608X7R2A333K080AA	TDK Corporation
2	D1, D2	GS1J-LTP	GS1J-LTP	Micro Commercial Co
1	J4		Header BBL-102-GE	Samtec
1	J1	LOAD	1714971	Phoenix Contact
1	J2	POWER	1714971	Phoenix Contact
1	J3		Terminal Block 39357-0004	Molex
1	L1	22 uH	AGP4233-223ME	Coilcraft
1	U1	IXDD604S1	IXDD604S1	IXYS Corp
2	U2	MMIXT132N50P3	MMIXT132N50P3	IXYS Corp
	U3	MMIXT132N50P3	MMIXT132N50P3	IXYS Corp
3	P4, P5, P6		1001-0-15-01-30-02-04-0	Mill-Max
2	R12, R20	1	RMCF0603FT1R00	Stackpole Electronics Inc
2	R16, R18	13 k	RMCF0603FT13K0	Stackpole Electronics Inc
2	R17, R21	20 k	RMCF0603FT20K0	Stackpole Electronics Inc
2	R19, R22	51.1 k	RMCF0603FT51K1	Stackpole Electronics Inc
2	R10, R11	88.7 k	RMCF0603FT88K7	Stackpole Electronics Inc
2	R1, R2	1.8	RMCF1206FT1R80	Stackpole Electronics Inc
6	R3, R4, R5, R13, R14, R15	332 k	RMCF1206FT332K	Stackpole Electronics Inc
1	R23	22	CRM2512-JW_220LFCT	
1	J5		5-5530843-0	TE Connectivity
1		Bridge Heatsink	40 mm 2 pin Video Graphics VGA Card GPU Cooler	

Table 2. Components of Digital Control Module

Count	Reference Designator	Value	Description	Manufacturer
2	C1, C2	0.033 µF	C0603C333K4RACTU	Kemet
2	C9, C16	0.1 µF	CL10B105KA8NNNC	Samsung
2	C14, C15	1 µF	CL10B106KA8NNNC	Samsung
1	C8	4.7 µF	CL10A475KA8NQNC	Samsung
1	C13	820 pF	TMK107B7821KA-T	Taiyo Yuden
2	D5, D6	BAT42XV2	BAT42XV2	Diodes Inc.
1	J6		Board Layout	
1	J4		Header 67996-406HLF	FCI
1	R23	1.74 k	RMCF0603FT1K74	Stackpole Electronics Inc
2	R17, R18	5.62 k	RMCF0603FT5K62	Stackpole Electronics Inc
3	R11, R12, R24	10 k	RMCF0603FT10K0	Stackpole Electronics Inc
1	R21	18.2 k	RMCF0603FT18K2	Stackpole Electronics Inc
2	R19, R20	806	RMCF0603FT806R	Stackpole Electronics Inc
1	U1	Z8F3281	Z8F3281AN024XK	Zilog

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