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JF2 Hardware User Guide

1vv0300985 Rev.4 – 2013-04-09

Making machines talk.

APPLICABILITY TABLE

PRODUCT
JF2

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Contents

1. Introduction

1.1. Scope

The JF2 is an 11mm by 11mm integrated GPS receiver module using SiRFstar IV technology. This document expands upon the data sheet(s) to highlight particular areas to allow the hardware engineer to achieve a successful design implementation.

1.2. Audience

This document is intended for helping customer in the integration of the Telit SE868 GPS module.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters (sample):

"Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

"Chapter 2: "Powering the JF2" gives an overview about power supply.

"Chapter 3: "Example Implementations" describes examples on how to implement the JF2.

"Chapter 4: "Updating Firmware" describes the SW updating procedure for Flash version.

"Chapter 5: "Updating Patch code" describes how to apply patch code to ROM version.

"Chapter 6: "ROM2.2 Features" describes the new ROM2.2 features.

"Chapter 7: "Main Serial Interface" describes the possible serial interfaces of the JF2.

"Chapter 8: "MEMS sensor and EEPROM Interface" describes the DR I2C interface.

"Chapter 9: "RF Front End Design" describes in details the characteristics of the Front end.

"Chapter 10: "Reference Design" gives an overview about the reference design.

"Chapter 11: "Firmware configuration" describes the configuration settings.

"Chapter 12: "Handling and soldering" describes packaging and soldering of the module.

"Chapter 13: "PCB layout details" describes the mechanical design of the module.

"Chapter 14: "Document History" describes the history of the present product.

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- JF2 Product Description,
- JF2 EVK User Guide,

2. Powering the JF2

2.1. 1.8V Supply Voltage

Unlike older GPS receiver modules, the JF2 requires a single always on supply voltage of 1.8 volts. Rather than having a "split" power supply design of main and backup, the JF2 manages all of its power modes internally. The JF2 will normally power up into the lowest power "hibernate" state upon initial application of power. Upon pulsing the ON-OFF signal, the JF2 will transition to the "operate" state. Pulsing the ON-OFF signal a second time will transition the JF2 back into the "hibernate" state.
The current power state of the JF2 can be determined by monitoring the "SYSTEM-ON" signal. A logic low indicates the module is in "hibernate", whereas logic high indicates the module is in "operate" state.
If the 1.8 volt DC supply is removed from the JF2 (regardless of power state) it will lose current RTC time and will lose the contents of the internal SRAM. To prevent improper startup, once power is removed, keep the power removed for approximately 10 seconds so the internal SRAM contents can clear reliably.
The JF2 monitors the 1.8 volt supply and issues an internal hardware reset if the supply drops below 1.7 volts. This reset protects the memory from accidental writes during a power down condition. However, the reset also clears the RTC time and forces the JF2 into a hibernate state.
To prevent this, the 1.8 volt supply must be regulated to be within ±50 mV of nominal voltage inclusive of load regulation and power supply noise and ripple. Noise and ripple outside of these limits can affect GPS sensitivity and also risk tripping the internal voltage supervisors, thereby shutting down the JF2 unexpectedly. Regulators with very good load regulation are strongly recommended along with adequate power supply filtering to prevent power supply glitches as the JF2 transitions between power states.
The power supply voltage, noise and ripple must be between 1.75V and 1.85V for all frequencies up to 3MHz. Above 3MHz, the noise and ripple component must not exceed ±16mV. To help meet these requirements, a separate LDO for the JF2 is suggested.

2.1.1. Capacitance

Aluminum electrolytic capacitors are not recommended at the input to the JF2 due to their high ESR. Tantalum capacitors are recommended with a minimum value of 10uF in parallel with a 0.1uF ceramic capacitor. Ceramic capacitors alone can be used, but make sure the LDO is stable with such capacitors tied to the output.

2.2. Implementing Pseudo Battery Back-up

As mentioned above, the JF2 cannot tolerate removal of the 1.8 volt supply without losing RTC time and SRAM data. The main supply voltage can be switched to a backup supply external to the JF2 provided the receiver is allowed time to enter the hibernate state. This can be accomplished by monitoring the status of the SYSTEM-ON line, which will be low whenever the JF2 is in the hibernate state. At this point, the main supply can be safely switched over to the backup supply provided the 1.8 volt supply stays within specification. Similarly, the switch back to the main supply must occur prior to placing the JF2 into full power mode.

If the product containing the JF2 needs to support abrupt removal of power, then the module will require a cold start reset upon reapplication of power.

2.3. Understanding ON-OFF and SYSTEM-ON

ON-OFF: Input control
SYSTEM-ON: Output indicator

The JF2 power is controlled by a state machine. This state machine is clocked by the internal 32 KHz RTC clock, and is controlled by internal signals as well as the ON-OFF and NRESET signals. The SYSTEM-ON signal reflects the power state of the JF2: logic low for hibernate mode, and logic high for full power mode.
When power is first applied to the JF2, the internal RTC must start up before the state machine can begin operating. ON-OFF signals applied before the state machine is ready for them will be ignored. The JF2 signals the readiness to accept ON-OFF signals by outputting a pulse on the SYSTEM-ON line after power is first applied. This pulse is only output upon application of power, and is not output when the receiver is in hibernate or full power mode.
The ON-OFF signal is normally low. When it transitions high, it should stay high for a time equivalent to a minimum of 3 RTC clock cycles. The signal may then transition low and remain low until the next change in power state is desired.
A single OR gate with one input being SYSTEM-ON and the other being an external pulse will allow the module to be turned back on with a suitable pulse, but it will not be possible to use a second pulse as it is blocked with the SYSTEM-ON signal. The only option to place the module in hibernate state is to issue the serial command.
If full ON-OFF control is desired along with having SYSTEM-ON auto-start the receiver, then additional logic is needed to detect the first falling edge of SYSTEM-ON and using this detection to gate off the SYSTEM-ON signal to the ON-OFF signal.
If GPIO8 is pulled to logic 1, then the ON-OFF input is modified to be just an ON input. It would not be possible to place the JF2 into hibernate by pulsing ON-OFF in this case.

2.3.1. Auto-ON Configuration (GPIO8 Control)

The JF2 powers up directly into the hibernate state. It is possible to have the module automatically transition to the full power state by tying the SYSTEM-ON output to the ON-OFF input. GPIO8 should also be tied high, which changes the ON-OFF signal to just an ON signal. However, this implementation eliminates the possibility of using the ON-OFF signal to change power states and eliminates the SiRFAware™ and Push-to-Fix™ power modes. If the serial command to place the JF2 in hibernate mode is issued, the module will transition to the hibernate state with no way other than removal and reapplication of power (with resulting RTC and SRAM data loss) to force the module to power up. For some users, this may be all that is required if time and data retention are not important during a power down situation.

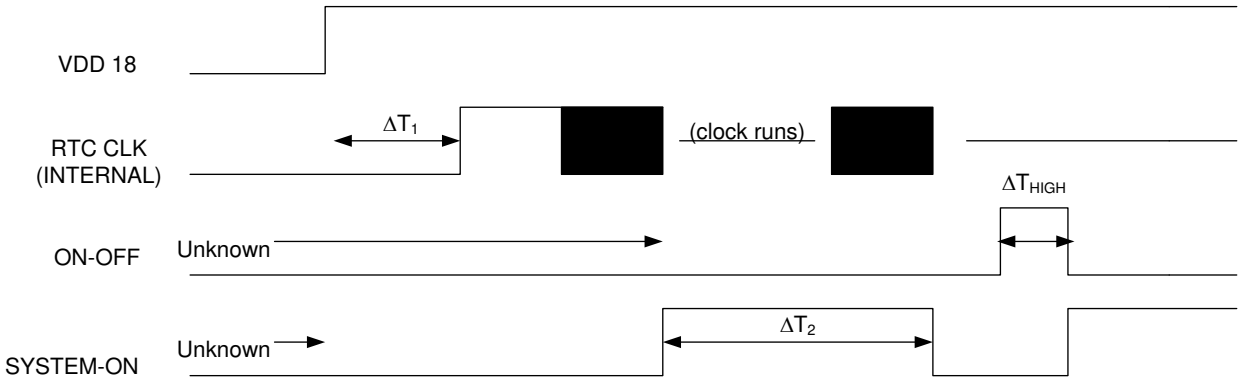

Figure 1 – Initial Application of Main Power

Timed Parameter	Prior Event/State	Symbol	Min	Typ	Max	Unit
RTC startup time	First power applied	T_1	0	299	1000	ms
FSM Ready pulse	RTC running	T_2		10		T_{RTC}
Min ON-OFF high		T_{HIGH}	3			T_{RTC}
T_{RTC} is equivalent to one RTC (32.678KHz) clock cycle.						

Table 1 – Power State Timing

The host system can determine if the J-F2 is "ready" as follows

- A short pulse on SYSTEM_ON output line indicates to a host that the J-F2 is ready and armed to accept an ON_OFF pulse.
- The host can wait a fixed duration. Wait at minimum 5 seconds before sending an ON_OFF pulse. Note that Telit recommends monitoring SYSTEM_ON.
- The host can issue ON_OFF pulses repeatedly every 100ms and monitor for JF-2 SYSTEM_ON output to go HIGH. Note that issuing an ON_OFF pulse once the system is running may cause the firmware to initiate the shutdown process
- The host can issue ON_OFF repeatedly every one second and wait for serial messages to be output within the one second. Note that issuing an ON_OFF pulse once the system is running may cause the firmware to initiate the shutdown process

2.4. Reset Design Details

The JF2 NRESET pin is normally connected to a 0.33uF ceramic capacitor. The JF2 will generate an internal reset as appropriate. No external reset signal needs to be applied to the JF2.

If an external reset is desired, the signal must be either open collector or open drain without any form of pullup. Do not pull this line high with either a pullup or a driven logic one. When this line is pulled low, the JF2 will immediately drop into hibernate mode with some loss of data.

When the external reset is released, the JF2 will go through its normal power up sequence provided the VCC_IN supply is within specifications.

3. Example Implementations

This section illustrates the implementations that meet the rules for the JF2. Telit recommends assessing the risks when making implementation decisions

3.1. Normal Operation Startup and Shutdown

To start the JF2:

Send a voltage pulse (tolerant to 3.6V) to the ON-OFF input.

To go into the shutdown sequence of the JF2 from full power state :

Send a voltage pulse (tolerant to 3.6V) to the ON-OFF input

or

Issue an NMEA ($PSRF117) or OSP (MID 205) serial command.

3.2. Self-Start Operation

For self-start operation, the SYSTEM-ON output is connected to the ON-OFF input. The JF2 then goes into full power run state when the supply voltage is first applied. GPIO8 must be pulled HIGH in this case to set the ON-OFF input to an ON only signal.

4. Updating the Firmware: Flash Module (ONLY)

During normal operations, the BOOT signal should be tied to ground through a 100K pulldown resistor. This will ensure the GPS module executes the code out of the internal flash memory.
However, if the internal flash memory needs to be updated, the following steps should be performed to place the JF2 module into a state suitable for programming the internal flash memory.

1. Either remove all power to the module, or force the module into hibernate state by pulsing the ON-OFF signal. Verify the state of the module by monitoring the SYSTEM-ON signal.
2. Pull the BOOT signal high through a 10K pull up resistor to +1.8 volts.
3. Apply main power if not already applied.
4. Pulse the ON-OFF signal to place the JF2 module into BOOT mode.
5. Run the software utility to re-flash the JF2 module. Clearing the entire flash memory is strongly recommended prior to programming.
6. Upon successful completion of re-flashing, remove main power to the module for a minimum of 10 seconds.
7. Pull the BOOT signal low through a 100K pull down resistor to GND.
8. Apply main power to the JF2.
9. Pulse the ON-OFF signal to place the JF2 into the normal operating state.

5. Updating Patch Code: EEPROM and ROM modules with Host Memory

Modules with EEPROM and ROM-only designs using external Host memory support firmware patching. Firmware patches for the EEPROM module are stored inside the I2C serial EEPROM device. Firmware patches for the ROM-only module are stored externally using Host memory.

At power up, patches are retrieved from EEPROM and loaded into patch RAM. Firmware patches are accumulated into patch data files, which in turn are made available with descriptions of their contents and applicability. A patch data file is cumulative in that it includes firmware improvements and enhancements made available in previous patches. It may also include configuration settings that differ from the ROM defaults, as in the default UART baud rate, for example. The desired patch data file must be distributed to the end-user device where it may be accessed by the Host processor.

The Host processor in the end-user device is required to run software that sends patch data from the patch file to the module using OSP Patch Protocol messages over the host serial port. Example source code to assist in the implementation of a patch downloader on the Host processor is available. Note that the module must be operating in full power mode during the patching process. The patch contents are loaded into patch RAM on the module, where they remain as long as main power is maintained. This avoids the reloading of patches into patch RAM when the system resumes normal operation from a low power state such as hibernate. At the end of the patching process the module performs an internal reset and restart.

If main power is lost on the ROM-only module, the Host processor must re-send the patch data over the host serial port after the module is powered up. The Host processor can determine whether patch data must be sent to the module by polling the software version, which reflects the currently applied patch file version.

6. ROM2.2 Features

6.1. SPI Flash Support

SPI flash provides external storage for features such as patches, SGEE, CGEE, broadcast ephemeris data, and data logging.

This feature is only supported by the JF2 ROM2.2 variant.

6.1.1. Hardware Interface

The SPI flash is connected through the following four GPIO pins

- GPIO0 as MISO
- GPIO1 as the SPI clock
- GPIO3 as slave chip select
- GPIO4 as MOSI

These four pins above form the standard SPI interface. The following features also use the same GPIOs as the SPI flash interface, therefore, only one feature can be used at a time:

- MEMS sensors
- I2C EEPROM
- Antenna sensing
- Baud Rate Detection

The SPI interface clocking and data transport are completely controlled by software and are not at a fixed rate.
Because of the methods used to access the SPI flash, the time required to store or retrieve data in the device is highly variable

6.1.2. Supported SPI Flash Chips

A limited number of SPI flash chips are supported by the firmware with the ROM 2.2 release. The table below lists the supported SPI flash chips in ROM 2.2 devices.

Manufacturer	Part Number	Storage Capacity
SST	SST25WF040	4Mb
SST	SST25WF020	2Mb
EON	EN25S40	4Mb
EON	EN25S20	2Mb

Table 2 Supported SPI Flash Chips in ROM 2.2

7. Main Serial Interface

The JF2 has the capability to operate in serial UART mode, SPI mode or I2C mode depending upon how the JF2 GPIO6 and GPIO7 pins are strapped at power up. Either leave the pin floating, apply a 10K resistor to +1.8V (PU) or apply a 10K resistor to GND (PD). Reference the JF2 SPI_UART_I2C Application Note for additional details on Serial Interface configuration and operation.

Mode	GPIO6 (internal pull-down)	GPIO7 (internal pull-up)
UART	PU	Leave floating or PU
I2C	Leave floating or PD	PD
SPI	Leave floating	Leave floating

Table 3 – Interface Operating Modes

7.1. UART Mode

The GPIO6 pin should be pulled high through a 10K resistor to the 1.8 volt supply. The GPIO7 pin can be left open or pulled high. Upon power up, the JF2 will communicate using a standard asynchronous 8 bit protocol with messages appearing on the TX line, and commands and data being entered on the RX line. Note the GPIO6 and GPIO7 lines are read at power up or reset only and are not used afterwards. In particular, no flow control operations are performed.

7.2. I2C Mode

The GPIO7 pin should be pulled low through a 10K resistor to GND. The GPIO6 pin can be left open or pulled low. Upon power, the JF2 acts as a master transmitter and a slave receiver. Pull-ups to a 1.8V to 3.6V power supply in the range of 1K to 2.2K are required on the RXA and TXA lines when used in I2C mode. In this mode, the pins are defined below:

Signal Name	I2C Function
RXA	I2C Data (DIO)
TXA	I2C Clock (CLK)

Table 4 – I2C Pin Assignments

Bit rates to 400K are achievable. Note the GPIO6 and GPIO7 lines are read at power up or reset only and are not used afterwards.

The operation of the I2C with a master transmit and slave receive mimics a UART operation, where both JF2 and host can independently freely transmit. It is possible to enable the master transmit and slave receive at the same time, as the I2C bus allows for contention resolution between JF2 and a host vying for the bus.

Note: This I2C port should not be confused with the secondary I2C port on the JF2 which is reserved for external serial EEPROM and MEMS sensors.

7.3. SPI Mode

If both the GPIO6 and GPIO7 pins are left floating, the JF2 will power up in slave SPI mode, supporting both SPI and Microwire formats. In this mode, the four pins are defined below:

Signal Name	SPI Function
GPIO7	SPI Chip Select (CS#)
GPIO6	SPI Clock (CLK)
RXA	SPI Data In (MOSI)
TXA	SPI Data Out (MISO)

Table 5 – SPI Mode Pin Assignments

NOTE:
Data rates of 6.8 MHz are achievable.

8. MEMS Sensor/EEPROM Interface

The DR I2C port is used for connecting to MEMS sensors, such as accelerometer or magnetometer. Pullup resistors of approximately 2.2Kohm to 1.8 volts are required on the DR I2C CLK and DR I2C IO lines for proper operation.

Only an approved accelerometer (KIONIX part number KXTF9-4100, 3 x 3mm LGA 1.8V 3 axis accelerometer and FREESCALE part number MMA8450Q) can be used. The interrupt output of the accelerometer must be connected to GPIO4 of the JF2.

Data for the approved magnetic sensor (Aichi Steel part number AIM304, 3.5 x 4.0mm 3V 3 axis magnetometer) is output in OSP message 72.

9. RF Front End Design

The JF2 contains an integrated LNA and pre-select SAW filter. This allows the JF2 to work well with a passive GPS antenna. If the antenna cannot be located near the JF2, then an active antenna (that is, an antenna with a low noise amplifier built in) can be used. The following items will be discussed in turn to assist in designing the "RF front end".

1. RF signal requirements
2. GPS antenna polarization
3. GPS antenna gain
4. System noise floor
5. Active versus passive antenna
6. RF trace losses
7. Implications of the pre-select SAW filter
8. External LNA gain and Noise Figure
9. Powering the external LNA (active antenna)
10. RF interference
11. Shielding

9.1. RF Signal Requirements

The JF2 can achieve Cold Start acquisition with a signal level of -147 dBm at its input. This means the JF2 can find the necessary satellites, download the necessary ephemeris data and compute the location within a 5 minute period. In the GPS signal acquisition process, downloading and decoding the data is the most difficult task, which is why Cold Start acquisition requires a higher signal level than navigation or tracking signal levels. For the purposes of this discussion, autonomous operation is assumed, which makes the Cold Start acquisition level the important design constraint. If assistance data in the form of time or ephemeris aiding is available, then even lower signal levels can be used to compute a navigation solution.

The GPS signal is defined by IS-GPS-200E. This document states that the signal level received by a linearly polarized antenna having 3 dBi gain will be a minimum of -130 dBm when the antenna is in the worst orientation and the satellite is 5 degrees or more above the horizon.

In actual practice, the GPS satellites are outputting slightly more power than specified by IS-GPS-200E, and the signal level typically goes higher as the satellites have higher elevation angles.

The JF2 will display a reported C/No of 40 dB-Hz for a signal level of -130 dBm into the RF input.

Each GPS satellite presents its own signal to the JF2, and best performance is obtained when the signal levels are between -125 dBm and -117 dBm. These received signal levels are determined by

- GPS satellite transmit power
- GPS satellite elevation and azimuth
- Free space path loss
- Extraneous path loss such as rain
- Partial or total path blockage such as foliage or building
- Multipath caused by signal reflection
- GPS antenna
- Signal path after the GPS antenna

The first three items in the list above are specified in IS-GPS-200E, readily available multiple sources online. IS-GPS-200E specifies a signal level minimum of -130 dBm will be presented to the receiver when using a linearly polarized antenna with 3 dBi gain.
The GPS signal is relatively immune to rainfall attenuation and does not really need to be considered.
However, the GPS signal is heavily influence by attenuation due to foliage, such as tree canopies, etc. as well as outright blockage caused by building, terrain or other items in the line of sight to the specific GPS satellite. This variable attenuation is highly dependent upon GPS satellite location. If enough satellites are blocked, say at a lower elevation, or all in a general direction, the geometry of the remaining satellites will result is a lower accuracy of position. The JF2 reports this geometry in the form of PDOP, HDOP and VDOP.
For example, in a vehicular application, the GPS antenna may be placed embedded into the dashboard or rear package tray of an automobile. The metal roof of the vehicle will cause significant blockage, plus any thermal coating applied to the vehicle glass can attenuate the GPS signal by as much as 15 dB. Again, both of these factors will affect the performance of the receiver.
Multipath is a phenomena where the signal from a particular satellite is reflected and is received by the GPS antenna in addition to or in place of the original line of sight signal. The multipath signal has a path length that is longer than the original line of sight path and can either attenuate the original signal, or if received in place of the original signal add additional error is determining a solution because the distance to the particular GPS satellite is actually longer than expected. It is this phenomena that makes GPS navigation in urban canyons (narrow roads surround by high rise buildings) so challenging. In general, the reflecting of the GPS signal causes the polarization to reverse. The implications of this are covered in the next section.

9.2. GPS Antenna Polarization

The GPS signal as broadcast is a right hand circularly polarized signal. The best antenna to receive the GPS signal is a right hand circularly (RHCP) polarized antenna. Remember that IS-GPS-200E specifies the receive power level with a linearly polarized antenna. A linearly polarized antenna will have 3 dB loss as compared to an RHCP antenna assuming the same antenna gain (specified in dBi and dBic respectively).
An RHCP antenna is better at rejecting multipath than a linearly polarized antenna. This is because the reflected signal changes polarization to LHCP, which would be rejected by the RHCP antenna by typically 20 dB or so. If the multipath signal is attenuating the line of sight signal, then the RHCP antenna would show a higher signal level than a linearly polarized antenna because the interfering signal is rejected.
However, in the case where the multipath signal is replacing the line of sight signal, such as in an urban canyon environment, then the number of satellites in view could drop below that needed to determine a 3D solution. This is a case where a bad signal may be better than no signal. The system designer needs to make tradeoffs in their application to determine what is the better choice.

9.3. GPS Antenna Gain

Antenna gain is defined as the extra signal power from the antenna as compared to a theoretical isotropic antenna (equally sensitive in all directions).
For example, a 25mm by 25m square patch antenna on a reference ground plane (usually 70mm by 70mm) will give an antenna gain at zenith of 5 dBic. A smaller 18mm by 18mm square patch on a reference ground plane (usually 50mm by 50mm) will give an antenna gain at zenith of 2 dBic.
While an antenna vendor will specify a nominal antenna gain (usually at zenith, or directly overhead) they should supply antenna pattern curves specifying gain as a function of elevation, and gain at a fixed elevation as a function of azimuth. Pay careful attention to the requirement to meet these specifications, such as ground plane required and any external matching components. Failure to follow these requirements could result in very poor antenna performance.
It is important to note that GPS antenna gain is not the same thing as external LNA gain. Most antenna vendors will specify these numbers separately, but some combine them into a single number. It is important to know both numbers when designing and evaluating the front end of a GPS receiver.
For example, antenna X has an antenna gain of 5 dBiC at azimuth and an LNA gain of 20 dB for a combined total of 25 dB. Antenna Y has an antenna gain of -5 dBiC at azimuth and an LNA gain of 30 dB for a combined total of 25 dB. However, in the system, antenna X will outperform antenna Y by about 10 dB (refer to Section 9.4 for more details on system noise floor).
An antenna with higher gain will generally outperform an antenna with lower gain. Once the signals are above about -130 dBm for a particular satellite, no improvement in performance would be gained. However, for those satellite that are below about -125 dBm, a higher gain antenna would improve the gain and improve the performance of the GPS receiver. In the case of really weak signals, a good antenna could mean the difference between being able to use a particular satellite signal or not.

9.4. System Noise Floor

As mentioned earlier, the JF2 will display a reported C/No of 40 dB-Hz for an input signal level of -130 dBm. The C/No number means the carrier (or signal) is 40 dB greater than the noise floor measured in a one Hz bandwidth. This is a standard method of measuring GPS receiver performance.
Thermal noise is -174 dBm/Hz at around room temperature. From this we can compute a system noise figure of 4 dB for the JF2. This noise figure consists of the loss of the pre-select SAW filter, the noise figure of the LNA as well as implementation losses within the digital signal processing unit.
If a good quality external LNA is used with the JF2, then the noise figure of that LNA (typically better than 1dB) could reduce the overall system noise figure of the JF2 from 4 dB to around 2 dB. Some of the factors in the system noise figure are implementation losses due to quantization and other factors and don't scale with improved front end noise figure.

9.5. Active versus Passive Antenna

If the GPS antenna is placed near the JF2 and the RF traces losses are not excessive (nominally 1 dB), then a passive antenna can be used. This would normally be the lowest cost option and most of the time the simplest to use. However, if the antenna needs to be located away from the JF2 then an active antenna may be required to obtain the best system performance. The active antenna has its own built in low noise amplifier to overcome RF trace or cable losses after the active antenna.
However, an active antenna has a low noise amplifier (LNA) with associated gain and noise figure. In addition, many active antenna have either a pre-select filter, a post-select filter or both.

9.6. RF Trace Losses

RF Trace losses are difficult to estimate on a PCB without having the appropriate tables or RF simulation software to estimate what the losses would be. A good rule of thumb would be to keep the RF traces as short as possible, make sure they are 50 ohms impedance and don't contain any sharp bends.