Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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Manufacturers of World Class Discrete Semiconductors

J174
J175
J176
J177

P CHANNEL JUNCTION FET

JEDEC TO-92 CASE

DESCRIPTION

The CENTRAL SEMICONDUCTOR J174 Series types are Silicon P Channel Junction Field Effect Transistors designed for switching applications.

MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

	SYMBOL		UNIT
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	V
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Operating and Storage Junction Temperature	T_J,T_{STG}	-65 TO +150	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

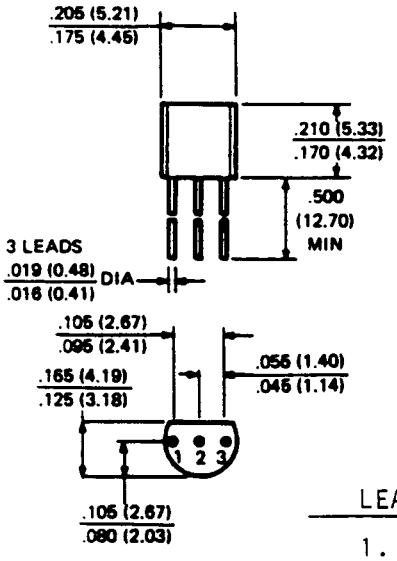
		J174		J175		J176		J177		
SYMBOL	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
I_{GSS}	V_{GS}=20V		1.0		1.0		1.0		1.0	nA
I_{DSS}	V_{DS}=15V	20	100	7	60	2	25	1.5	20	mA
BV_{GSS}	I_G=1.0μA	30		30		30		30		V
$V_{GS(OFF)}$	V_{DS}=15V, I_D=10nA	5	10	3	6	1	4	0.8	2.25	V
$r_{DS(ON)}$	V_{DS}=0.1V		85		125		250		300	Ω
$I_{D(OFF)}$	V_{GS}=10V, V_{DS}=15V		1.0		1.0		1.0		1.0	nA
$C_{dg(OFF)}$	V_{GS}=10V, V_{DS}=0, f=1.0MHz	5.5 TYP		5.5 TYP		5.5 TYP		5.5 TYP		pF
$C_{sg(OFF)}$	V_{GS}=10V, V_{DS}=0, f=1.0MHz	5.5 TYP		5.5 TYP		5.5 TYP		5.5 TYP		pF
$C_{dg(ON)}$	V_{GS}=0, V_{DS}=0, f=1.0MHz	40 TYP		40 TYP		40 TYP		40 TYP		pF
$C_{sg(ON)}$	V_{GS}=0, V_{DS}=0, f=1.0MHz	40 TYP		40 TYP		40 TYP		40 TYP		pF
$t_{d(ON)}$	*	2.0 TYP		5.0 TYP		15 TYP		20 TYP		ns
t_r	*	5.0 TYP		10 TYP		20 TYP		25 TYP		ns
$t_{d(OFF)}$	*	5.0 TYP		10 TYP		15 TYP		20 TYP		ns
t_f	*	10 TYP		20 TYP		20 TYP		25 TYP		ns

*TEST CONDITIONS:

J174	V_{DD}=10V, $V_{GS(ON)}$=0, R_L=560Ω, $V_{GS(OFF)}$=12V
J175	V_{DD}=6.0V, $V_{GS(ON)}$=0, R_L=12kΩ, $V_{GS(OFF)}$=8.0V
J176	V_{DD}=6.0V, $V_{GS(ON)}$=0, R_L=5.6kΩ, $V_{GS(OFF)}$=6.0V
J177	V_{DD}=6.0V, $V_{GS(ON)}$=0, R_L=10kΩ, $V_{GS(OFF)}$=3.0V

SEE REVERSE FOR OUTLINE DRAWING

OUTLINE DRAWING



LEAD CODE

1. DRAIN
2. GATE
3. SOURCE

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