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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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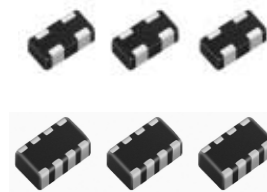
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アレイ形積層セラミックコンデンサ ARRAY TYPE MULTILAYER CERAMIC CAPACITOR



リフロー／REFLOW

	code	Temp.characteristics	operating Temp. range
OPERATING TEMP.	BJ	B	- 25~+85°C
		X5R	- 55~+85°C
		X7R	- 55~+125°C
	CH	C0H	- 55~+125°C

特長 FEATURES

- ・2125形状で4回路構成であるため、より高密度、高効率な実装を実現
- ・1回路あたりの容量は1 μ Fの大容量
- ・内部電極には、信頼性とコストパフォーマンスに優れたNiを使用しています。
- ・4 circuits in 2125 package allows higher placement density and efficiency
- ・The capacitance in each circuit, F or B dielectric, is 1 μ F
- ・Internal electrode is nickel for increased cost performance and reliability

用途 APPLICATIONS

- ・一般電子機器用
- ・通信機器用(携帯電話、PHS、コードレス電話etc)
- ・General electronic equipment
- ・Communication equipment (mobile phone, PHS, cordless phone, etc.)

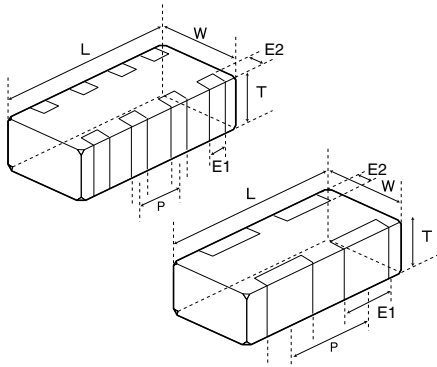
形名表記法 ORDERING CODE

1 定格電圧 (VDC)	J 6.3 L 10 E 16 T 25 U 50	3 端子電極	K メッキ品	5 温度特性	BJ ± 10 [%] CH 0 ± 60 [ppm/°C]	7 容量許容差	M ± 20 % K ± 10 % F ± 1 pF	9 個別仕様	- 標準
2 シリーズ名	4 4 連積層コンデンサ 2 2 連積層コンデンサ	4 形状寸法 (EIA) L×W(mm)	110(0504) 1.4×1.0 212(0805) 2.0×1.25 316(1206) 3.2×1.6	6 公称静電容量 (pF)	例 104 100,000 105 1,000,000	8 製品厚み (mm)	B 0.6 A 0.8 D 0.85 F 1.15	10 包装	T リールテーピング
								11 当社管理記号	Δ 標準品 Δ = スペース



1 Rated voltage(VDC)	J 6.3 L 10 E 16 T 25 U 50	3 End termination	K Plated	5 Temperature characteristics code	BJ X5R -55~+85°C ± 15 % X7R -55~+125°C ± 15 % CH C0H 0 ± 60 [ppm/°C]	7 Capacitance tolerances(%)	M ± 20 K ± 10 F ± 1 pF	9 Special code	- Standard products
2 Series name	4 4 circuit multilayer capacitors 2 2 circuit multilayer capacitors	4 Dimensions(case size)(mm)	110(0504) 1.4×1.0 212(0805) 2.0×1.25 316(1206) 3.2×1.6	6 Nominal capacitance(pF)	example 104 100,000 105 1,000,000	8 Thickness(mm)	B 0.6 A 0.8 D 0.85 F 1.15	10 Packaging	T Tape & reel
								11 Internal code	Δ Standard products Δ = Blank space

外形寸法 EXTERNAL DIMENSIONS



Type(EIA)	L	W	E1	E2	P	T	
□2K110 (0504)	1.37±0.07 (0.054±0.003)	1.00±0.08 (0.039±0.003)	0.36±0.10 (0.014±0.004)	0.20±0.10 (0.008±0.004)	0.64±0.10 (0.025±0.004)	B	0.60±0.06 (0.024±0.003)
						A	0.80±0.08 (0.031±0.003)
□4K212 (0805)	2.00±0.10 (0.079±0.004)	1.25±0.10 (0.049±0.004)	0.25±0.10 (0.010±0.004)	0.25±0.15 (0.010±0.006)	0.50±0.10 (0.020±0.004)	D	0.85±0.10 (0.033±0.004)
□2K212 (0805)	2.00±0.10 (0.079±0.004)	1.25±0.10 (0.049±0.004)	0.50±0.20 (0.020±0.008)	0.25±0.15 (0.010±0.006)	1.00±0.10 (0.039±0.004)	D	0.85±0.10 (0.033±0.004)
□4K316 (1206)	3.20±0.15 (0.126±0.006)	1.60±0.15 (0.063±0.006)	0.40±0.20 (0.016±0.008)	0.30±0.20 (0.012±0.008)	0.80±0.10 (0.031±0.004)	F	1.15±0.15 (0.045±0.006)

Unit : mm (inch)

概略バリエーション AVAILABLE CAPACITANCE RANGE

BJ/ X7R, BJ/ X5R

Cap [μF]	Type Temp.Char VDC [pF:3digits]	1410 2連 □2K110				2125 2連 □2K212		2125 4連 □4K212				3216 4連 □4K316		
		BJ/ X7R		BJ/ X5R		BJ/ X5R		BJ/ X5R				BJ/ X5R		
		25V	16V	10V	6.3V	10V	6.3V	25V	16V	10V	6.3V	16V	10V	6.3V
0.01	103	B												
0.022	223	B												
0.047	473		B											
0.1	104		B				D	D						
0.22	224			B					D					
0.47	474			A						D				
1.0	105				A	D					D	F	F	F
2.2	225						D							

※グラフ記号は製品厚みを表します。 Letters inside the shaded boxes indicate thickness.

CH/ C0H

Cap [pF]	Type Temp.Char VDC [pF:3digits]	1410 2連 □2K110	
		CH / C0H	50V
		10	100
12	120	B	
15	150	B	
18	180	B	
22	220	B	
27	270	B	
33	330	B	
39	390	B	
47	470	B	
56	560	B	
68	680	B	
82	820	B	
100	101	B	

※グラフ記号は製品厚みを表します。 Letters inside the shaded boxes indicate thickness.

温度特性コード Temp. char.Code	温度特性 Temperature characteristics					静電容量許容差(%) Capacitance tolerance	tanδ(%) Dissipation factor
	準拠規格 Applicable standard		温度範囲(°C) Temperature range	基準温度(°C) Ref. Temp.	静電容量変化率 Capacitance change		
	BJ	JIS	B	-25~85	20		
	EIA	X5R	-55~85	25	±15[%]		
	EIA	X7R	-55~125	25	±15[%]		
CH	JIS	CH	-55~125	20	±60[ppm/c]	±10(K)	0.1%max.**
	EIA	C0H	-55~125	25	±60[ppm/c]		

* 10% : J2K110, J4K212 3.5% : 110type C<0.1μF

** 27pF以下 Q≥400+20・C 30pF以上 Q≥1000

セレクションガイド
Selection Guide

アイテム一覧
Part Numbers

特性図
Electrical Characteristics

梱包
Packaging

信頼性
Reliability Data

使用上の注意
Precautions



etc

アイテム一覧 PART NUMBERS

■1410TYPE (0504 case size) 2連タイプ (2 circuit type)

定格電圧 Rated Voltage	形名 Ordering code	公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tan δ Dissipation factor[%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロ- Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm](inch)
25V	T2K110 BJ103□B	0.01	B/X7R	3.5	R	±20%[M] ±10%[K]	0.6±0.06 (0.024±0.002)
	T2K110 BJ223□B	0.022					
	T2K110 BJ104□B	0.1					
16V	E2K110 BJ473□B	0.047	B/X7R	3.5			
	E2K110 BJ104□B	0.1					
10V	L2K110 BJ224□B	0.22	B/X5R	5			
	L2K110 BJ474□A	0.47					
6.3V	J2K110 BJ105□A*	1.0	BJ/X5R	10			0.8±0.08 (0.031±0.003)
	J2K110 BJ225□A*	2.2					

定格電圧 Rated Voltage	形名 Ordering code	公称静電容量 Capacitance [pF]	温度特性 Temperature characteristics	Q symbol	実装条件 Soldering method R:リフロー Reflow soldering W:フロ- Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm](inch)
50V	U2K110 CH100FB	10	CH	400+20・C	R	±10%[K]	0.6±0.06 (0.024±0.002)
	U2K110 CH120KB	12					
	U2K110 CH150KB	15					
	U2K110 CH180KB	18					
	U2K110 CH220KB	22					
	U2K110 CH270KB	27					
	U2K110 CH330KB	33		1000 (0.1%)			
	U2K110 CH390KB	39					
	U2K110 CH470KB	47					
	U2K110 CH560KB	56					
	U2K110 CH680KB	68					
	U2K110 CH820KB	82					
	U2K110 CH101KB	100					

■2125TYPE (0805 case size) 4連タイプ (4 circuit type)

定格電圧 Rated Voltage	形名 Ordering code	公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tan δ Dissipation factor[%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロ- Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm](inch)
25V	T4K212 BJ104□D	0.1	B/X5R	5	R	±20%[M] ±10%[K]	0.85±0.1 (0.033±0.004)
16V	E4K212 BJ104□D	0.1					
10V	L4K212 BJ224□D	0.22					
	L4K212 BJ474□D	0.47					
6.3V	J4K212 BJ105□D*	1.0	X5R	10			

■2125TYPE (0805 case size) 2連タイプ (2 circuit type)

定格電圧 Rated Voltage	形名 Ordering code	公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tan δ Dissipation factor[%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロ- Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm](inch)
25V	T2K212 BJ105□D	1.0	B/X5R	5	R	±20%[M] ±10%[K]	0.85±0.1 (0.033±0.004)
16V	E2K212 BJ105□D	1.0					
10V	L2K212 BJ105MD	1.0					
6.3V	J2K212 BJ225MD*	2.2	X5R	10			

■3216TYPE (1206 case size) 4連タイプ (4 circuit type)

定格電圧 Rated Voltage	形名 Ordering code	公称静電容量 Capacitance [μF]	温度特性 Temperature characteristics	tan δ Dissipation factor[%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロ- Wave soldering	静電容量許容差 Capacitance tolerance	厚み Thickness [mm](inch)
16V	E4K316 BJ105□F*	1.0	B/X5R	5	R	±20%[M] ±10%[K]	1.15±0.15 (0.045±0.006)
10V	L4K316 BJ105□F						
6.3V	J4K316 BJ105□F						

形名の□には静電容量許容差記号が入ります。

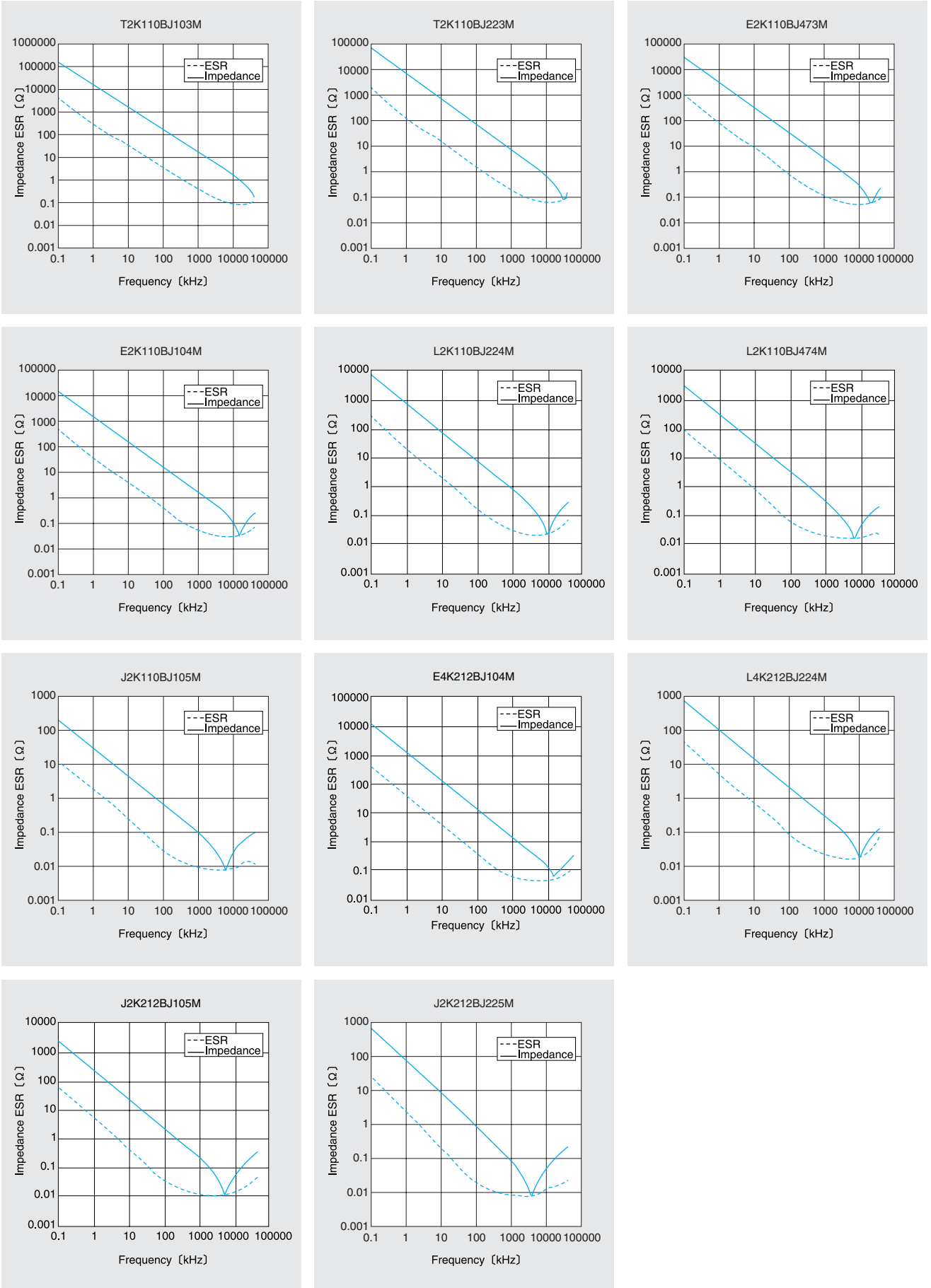
□ Please specify the capacitance tolerance code.

*高温負荷試験の試験電圧は定格電圧の1.5倍

*Test voltage of Loading at high temperature test is 1.5 time of the rated voltage.

インピーダンス・ESR-周波数特性例 Example of Impedance ESR vs. Frequency characteristics

・当社積層セラミックコンデンサ例 (Taiyo Yuden multilayer ceramic capacitor)



梱包 PACKAGING

①最小受注単位数 Minimum Quantity

■袋づめ梱包 Bulk packaging

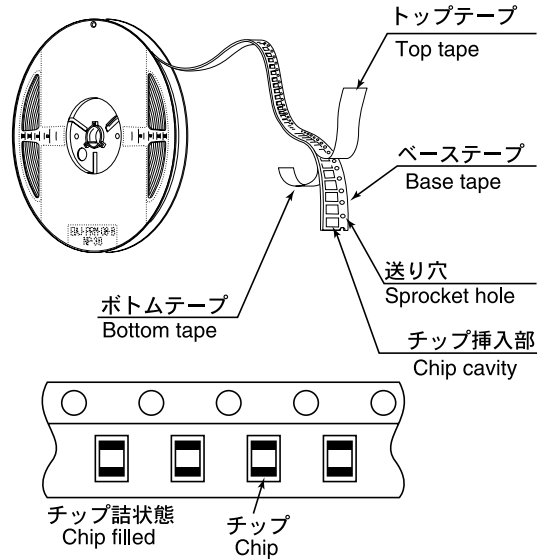
形式(EIA) Type	製品厚み Thickness		標準数量 Standard quantity [pcs]
	mm(inch)	code	
□MK105(0402)	0.5 (0.020)	V, W	1000
□VK105(0402)		W	
□MK107(0603)	0.8 (0.031)	A	
		Z	
□2K110(0504)	0.8 (0.031)	A	
	0.6 (0.024)	B	
	0.85 (0.033)	D	
□MK212(0805)	1.25 (0.049)	G	
□4K212(0805)	0.85 (0.033)	D	
□2K212(0805)	0.85 (0.033)	D	
□MK316(1206)	0.85 (0.033)	D	
	1.15 (0.045)	F	
	1.25 (0.049)	G	
	1.6 (0.063)	L	
□MK325(1210)	0.85 (0.033)	D	
	1.15 (0.045)	F	
	1.5 (0.059)	H	
	1.9 (0.075)	N	
	2.0max (0.079)	Y	
	2.5 (0.098)	M	

■テーピング梱包 Taped packaging

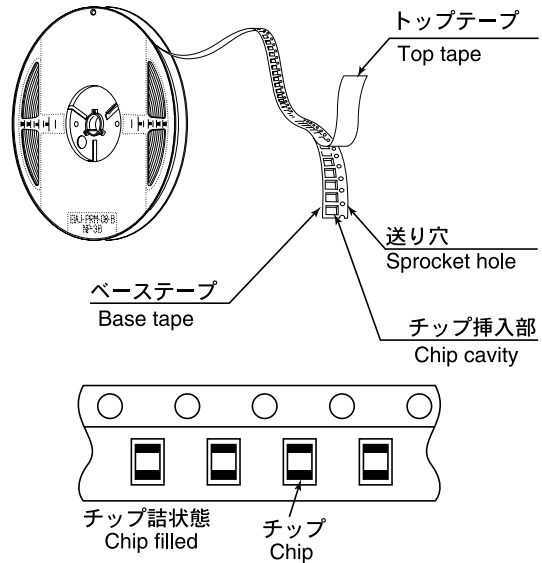
形式(EIA) Type	製品厚み Thickness		標準数量 Standard quantity [pcs]	
	mm(inch)	code	紙テープ paper	エンボステープ Embossed tape
□MK063(0201)	0.3 (0.012)	P	15000	—
□MK105(0402)	0.5 (0.020)	V, W	10000	—
□VK105(0402)		W		
□MK107(0603)	0.5 (0.020)	V	4000	—
	0.45 (0.018)	K	4000	—
	0.8 (0.031)	A	4000	—
□2K110(0504)	0.8 (0.031)	Z	4000	—
	0.8 (0.031)	A	4000	—
□2K110(0504)	0.6 (0.024)	B	4000	—
	0.45 (0.018)	K	4000	—
□MK212(0805)	0.85 (0.033)	D	4000	—
	1.25 (0.049)	G	—	3000
□4K212(0805)	0.85 (0.033)	D	4000	—
□2K212(0805)	0.85 (0.033)	D	4000	—
□MK316(1206)	0.85 (0.033)	D	4000	—
	1.15 (0.045)	F	—	3000
	1.25 (0.049)	G	—	3000
□4K316(1206)	1.6 (0.063)	L	—	2000
	0.85 (0.033)	D	—	2000
	1.15 (0.045)	F	—	2000
	1.5 (0.059)	H	—	2000
□MK325(1210)	1.9 (0.075)	N	—	2000
	2.0max (0.079)	Y	—	2000
	2.5 (0.098)	M	—	500
	1.9 (0.075)	Y	—	1000
□MK432(1812)	2.5 (0.098)	M	—	500
	3.2 (0.125)	U	—	500

②テーピング材質 Taping material

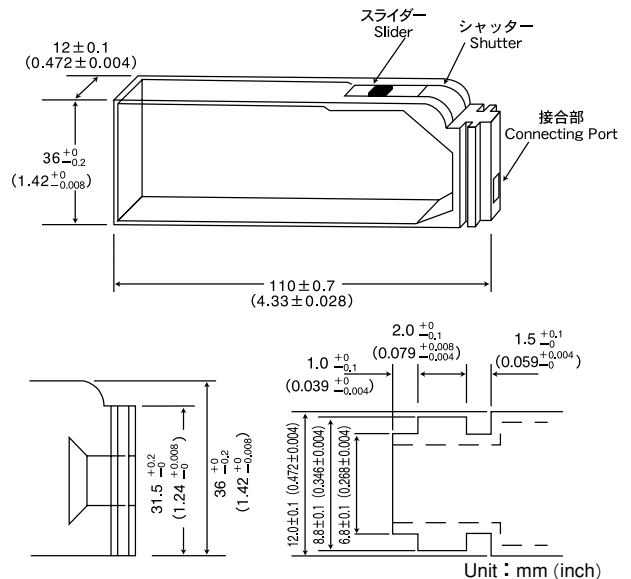
紙テープ
Card board carrier tape



エンボステープ
Embossed Tape

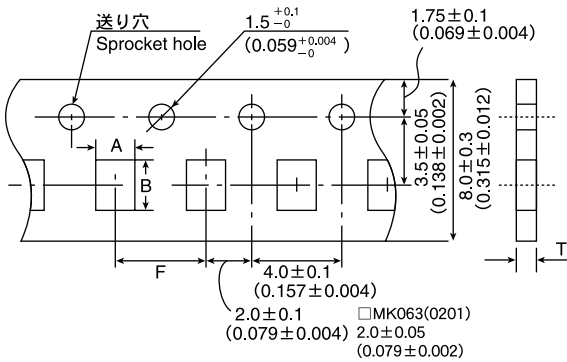


③バルクカセット Bulk Cassette



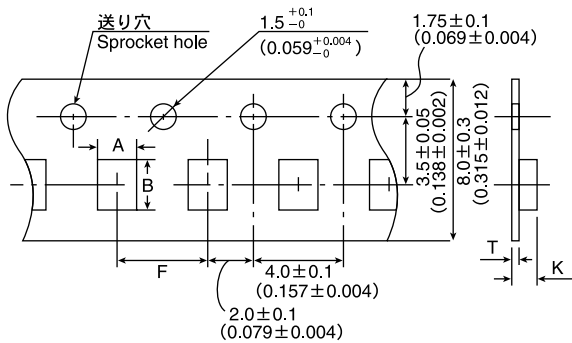
105, 107, 212形状で個別対応致しますのでお問い合わせ下さい。
Please contact any of our offices for accepting your requirement according to dimensions 0402, 0603, 0805.(inch)

③テーピング寸法 Taping dimensions
紙テープ Paper Tape (8mm幅) (0.315inches wide)



Type (EIA)	チップ挿入部 Chip Cavity		挿入ピッチ Insertion Pitch F	テープ厚み Tape Thickness T	
	A	B		K	T
□MK063(0201)	0.37±0.06 (0.06±0.002)	0.67±0.06 (0.027±0.002)	2.0±0.05 (0.079±0.002)	0.45max. (0.018max.)	
□MK105(0402)	0.65±0.1 (0.026±0.004)	1.15±0.1 (0.045±0.004)	2.0±0.05 (0.079±0.002)	0.8max. (0.031max.)	
□VK105(0402)					
□MK107(0603)	1.0±0.2 (0.039±0.008)	1.8±0.2 (0.071±0.008)	4.0±0.1 (0.157±0.004)	1.1max. (0.043max.)	
□2K110(0504)	1.15±0.2 (0.045±0.008)	1.55±0.2 (0.061±0.008)	4.0±0.1 (0.157±0.004)	1.0max. (0.039max.)	
□MK212(0805)	1.65±0.2 (0.065±0.008)	2.4±0.2 (0.094±0.008)	4.0±0.1 (0.157±0.004)	1.1max. (0.043max.)	
□4K212(0805)					
□2K212(0805)					
□MK316(1206)	2.0±0.2 (0.079±0.008)	3.6±0.2 (0.142±0.008)			

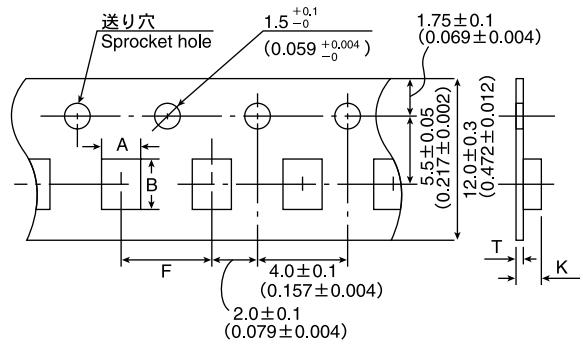
エンボステープ Embossed tape (8mm幅) (0.315inches wide)



Type (EIA)	チップ挿入部 Chip cavity		挿入ピッチ Insertion Pitch F	テープ厚み Tape Thickness	
	A	B		K	T
□MK212(0805)	1.65±0.2 (0.065±0.008)	2.4±0.2 (0.094±0.008)	4.0±0.1 (0.157±0.004)		
□MK316(1206)	2.0±0.2 (0.079±0.008)	3.6±0.2 (0.142±0.008)		2.5max.	0.6max
□4K316(1206)					
□MK325(1210)	2.8±0.2 (0.110±0.008)	3.6±0.2 (0.142±0.008)		3.4max. (0.134max.)	

Unit : mm(inch)

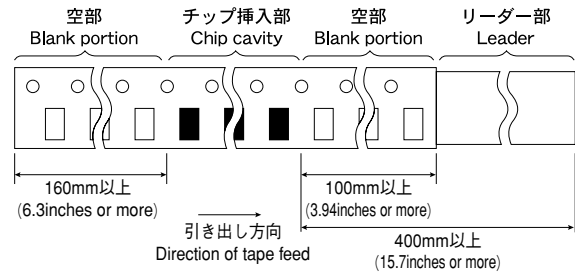
エンボステープ Embossed tape (12mm幅) (0.472inches wide)



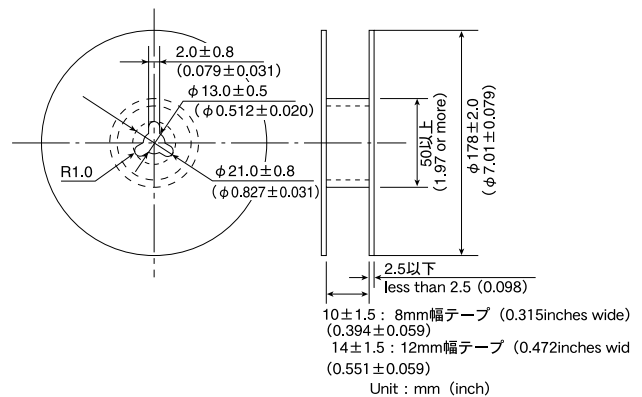
Type (EIA)	チップ挿入部 Chip cavity		挿入ピッチ Insertion Pitch F	テープ厚み Tape Thickness	
	A	B		K	T
□MK432(1812)	3.7±0.2 (0.146±0.008)	4.9±0.2 (0.193±0.008)	8.0±0.1 (0.315±0.004)	4.0max. (0.157max.)	0.6max. (0.024max.)

Unit : mm(inch)

④リーダー部/空部 Leader and Blank portion

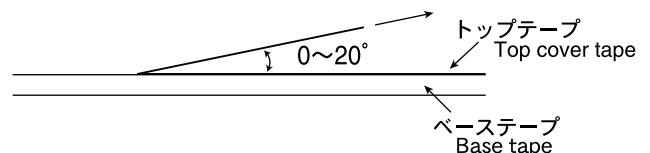


⑤リール寸法 Reel size

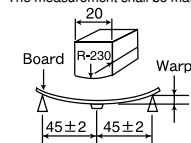


⑥トップテープ強度 Top Tape Strength

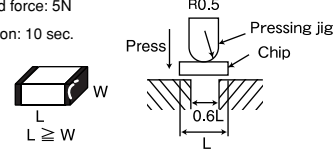
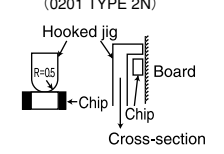
トップテープのはがし力は下図矢印方向にて0.1~0.7Nとなります。
The top tape requires a peel-off force of 0.1~0.7N in the direction of the arrow as illustrated below.



Multilayer Ceramic Capacitor Chips

Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permittivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
1. Operating Temperature Range	-55 to +125°C		B : -55 to +125°C F : -25 to +85°C	-25 to +85°C	High Capacitance Type BJ(X7R) : -55~+125°C, BJ(X5R) : -55~+85°C C(X5S) : -55~+85°C, C(X6S) : -55~+105°C E(Y5U) : -30~+85°C, F(Y5V) : -30~+85°C
2. Storage Temperature Range	-55 to +125°C		B : -55 to +125°C F : -25 to +85°C	-25 to +85°C	High Capacitance Type BJ(X7R) : -55~+125°C, BJ(X5R) : -55~+85°C C(X5S) : -55~+85°C, C(X6S) : -55~+105°C E(Y5U) : -30~+85°C, F(Y5V) : -30~+85°C
3. Rated Voltage	50VDC, 25VDC, 16VDC	16VDC 50VDC	50VDC, 25VDC	50VDC, 35VDC, 25VDC 16VDC, 10VDC, 6.3VDC 4DVC	
4. Withstanding Voltage Between terminals	No breakdown or damage	No abnormality	No breakdown or damage		Applied voltage: Rated voltage×3 (Class 1) Rated voltage×2.5 (Class 2) Duration: 1 to 5 sec. Charge/discharge current: 50mA max. (Class 1,2)
5. Insulation Resistance	10000 MΩ min.		500 MΩ μF. or 10000 MΩ., whichever is the smaller. Note 5		Applied voltage: Rated voltage Duration: 60±5 sec. Charge/discharge current: 50mA max.
6. Capacitance (Tolerance)	0.5 to 5 pF: ±0.25 pF 1 to 10pF: ±0.5 pF 5 to 10 pF: ±1 pF 11 pF or over: ± 5% ±10% 105TYPERSΔ, SΔ, TΔ, UΔ only 0.5~2pF: ±0.1pF 2.2~20pF: ±5%	0.5 to 2 pF : ±0.1 pF 2.2 to 5.1 pF : ±5%	B: ±10%, ±20% F: $\begin{matrix} +80 \\ -20 \end{matrix}$ %	B : ±10%、±20% C : ±10%、±20% E : -20%/+80% F : -20%/+80%	Measuring frequency : Class 1 : 1MHz±10%(C≤1000pF) 1 k Hz±10%(C>1000pF) Class 2 : 1 k Hz±10%(C≤22μF) 120Hz±10Hz(C>22μF) Measuring voltage : Class 1 : 0.5~5Vrms(C≤1000pF) 1±0.2Vrms(C>1000pF) Class 2 : 1±0.2Vrms(C≤22μF) 0.5±0.1Vrms(C>22μF) Bias application: None
7. Q or Tangent of Loss Angle (tan δ)	Under 30 pF : Q≥400 + 20C 30 pF or over : Q≥1000 C= Nominal capacitance	Refer to detailed specification	B: 2.5% max. (50V, 25V) F: 5.0% max. (50V, 25V)	B : 2.5% max. C、E、F : 7% max. Note 4	Multilayer: Measuring frequency : Class 1 : 1MHz±10%(C≤1000pF) 1 k Hz±10%(C>1000pF) Class 2 : 1 k Hz±10%(C≤22μF) 120Hz±10Hz(C>22μF) Measuring voltage : Class 1 : 0.5~5Vrms(C≤1000pF) 1±0.2Vrms(C>1000pF) Class 2 : 1±0.2Vrms(C≤22μF) 0.5±0.1Vrms(C>22μF) Bias application: None High-Frequency-Multilayer: Measuring frequency: 1GHz Measuring equipment: HP4291A Measuring jig: HP16192A
8. Temperature Characteristic of Capacitance	(Without voltage application) CK : 0±250 CJ : 0±120 CH : 0±60 CG : 0±30 PK : -150±250 PJ : -150±120 PH : -150±60 RK : -220±250 RJ : -220±120 RH : -220±60 SK : -330±250 SJ : -330±120 SH : -330±60 TK : -470±250 TJ : -470±120 TH : -470±60 UK : -750±250 UJ : -750±120 SL : +350 to -1000 (ppm/°C)	CH : 0±60 RH : -220±60 (ppm/°C)	B : ±10%(-25~85°C) F : $\begin{matrix} +30 \\ -80 \end{matrix}$ %(-25~85°C) B(X7R) : ±15% F(Y5V) : $\begin{matrix} +22 \\ -82 \end{matrix}$ %	B : ±10% (-25~+85°C) C : ±20% (-25~+85°C) E : +20%/ -55% (-25~+85°C) F : +30%/ -80% (-25~+85°C) B(X7R、X5R) : ±15% C(X5S、X6S) : ±22% E(Y5U) : +22%/ -56% F(Y5V) : +22%/ -82%	According to JIS C 5102 clause 7.12. Temperature compensating: Measurement of capacitance at 20°C and 85°C shall be made to calculate temperature characteristic by the following equation. $\frac{(C_{85} - C_{20})}{C_{20} \times \Delta T} \times 10^{-6}$ (ppm/°C) High permittivity: Change of maximum capacitance deviation in step 1 to 5 Temperature at step 1: +20°C Temperature at step 2: minimum operating temperature Temperature at step 3: +20°C (Reference temperature) Temperature at step 4: maximum operating temperature Temperature at step 5: +20°C Reference temperature for X7R, X5R, X5S, X6S, Y5U and Y5V shall be +25°C
9. Resistance to Flexure of Substrate	Appearance: No abnormality Capacitance change: Within ±5% or ±0.5 pF, whichever is larger.	Appearance: No abnormality Capacitance change: Within ±0.5 pF	Appearance: No abnormality Capacitance change: B, BJ, C: Within ±12.5% E, F: Within ±30%	Warp: 1mm Testing board: glass epoxy-resin substrate Thickness: 1.6mm (063 TYPE : 0.8mm) The measurement shall be made with board in the bent position.  (Unit: mm)	

Multilayer Ceramic Capacitor Chips

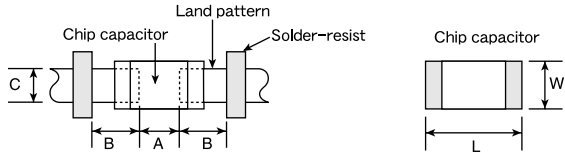
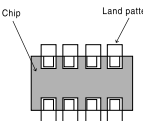
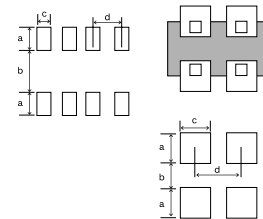
Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permittivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
10.Body Strength	—	No mechanical damage.	—	—	High Frequency Multilayer: Applied force: 5N Duration: 10 sec. 
11.Adhesion of Electrode	No separation or indication of separation of electrode.				Applied force: 5N Duration: 30±5 sec. (0201 TYPE 2N) 
12.Solderability	At least 95% of terminal electrode is covered by new solder.				Solder temperature: 230±5°C Duration: 4±1 sec.
13.Resistance to soldering	Appearance: No abnormality Capacitance change: Within ± 2.5% or ±0.25pF, whichever is larger. Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±2.5% Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±7.5% (B, BJ) Within ±15% (C) Within ±20% (E, F) tan δ: Initial value Note 4 Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Preconditioning: Thermal treatment (at 150°C for 1 hr) (Applicable to Class 2.) Solder temperature: 270±5°C Duration: 3±0.5 sec. Preheating conditions: 80 to 100°C, 2 to 5 min. or 5 to 10 min. 150 to 200°C, 2 to 5 min. or 5 to 10 min. Recovery: Recovery for the following period under the standard condition after the test. 24±2 hrs (Class 1) 48±4 hrs (Class 2)	
14.Thermal shock	Appearance: No abnormality Capacitance change: Within ± 2.5% or ±0.25pF, whichever is larger. Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±0.25pF Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±7.5% (B, BJ) Within ±15% (C) Within ±20% (E, F) tan δ: Initial value Note 4 Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Preconditioning: Thermal treatment (at 150°C for 1 hr) (Applicable to Class 2.) Conditions for 1 cycle: Step 1: Minimum operating temperature -3^{+0} °C 30±3 min. Step 2: Room temperature 2 to 3 min. Step 3: Maximum operating temperature $+3^{-0}$ °C 30±3 min. Step 4: Room temperature 2 to 3 min. Number of cycles: 5 times Recovery after the test: 24±2 hrs (Class 1) 48±4 hrs (Class 2)	
15.Damp Heat (steady state)	Appearance: No abnormality Capacitance change: Within ±5% or ±0.5pF, whichever is larger. Q: $C \geq 30$ pF : $Q \geq 350$ $10 \leq C < 30$ pF: $Q \geq 275 + 2.5C$ $C < 10$ pF : $Q \geq 200 + 10C$ C: Nominal capacitance Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: Within ±0.5pF, Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: B: Within ±12.5% F: Within ±30% tan δ: B: 5.0% max. F: 7.5% max. Note 4 Insulation resistance: 50 MΩ μF or 1000 MΩ whichever is smaller. Note 5	Appearance: No abnormality Capacitance change: BJ: Within ±12.5% C(X6S) Within ±25% C(X5S),E,F Within ±30% Note 4 tan δ: BJ: 5.0% max. C, E, F: 11.0% max. Insulation resistance: 50 MΩ μF or 1000 MΩ whichever is smaller. Note 5	Multilayer : Preconditioning: Thermal treatment (at 150°C for 1 hr) (Applicable to Class 2.) Temperature: 40±2°C Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1) 48±4 hrs (Class 2) High-Frequency Multilayer: Temperature: 60±2°C Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1)

Multilayer Ceramic Capacitor Chips

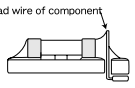
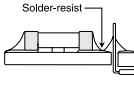
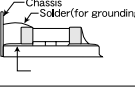
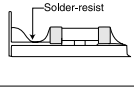
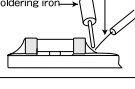
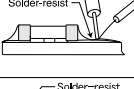
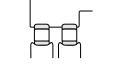

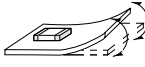
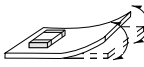
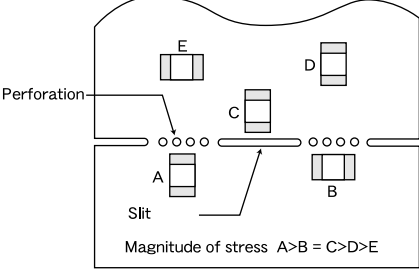
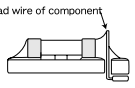
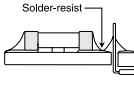
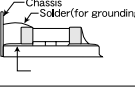
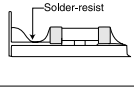
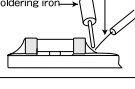
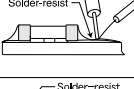
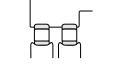

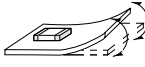
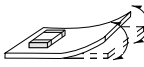
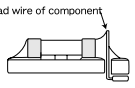
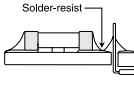
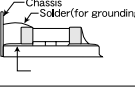
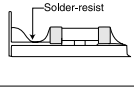
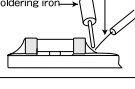
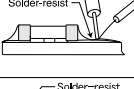
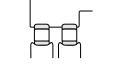

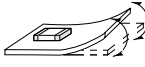
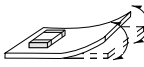
Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permittivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
16.Loading under Damp Heat	Appearance: No abnormality Capacitance change: Within $\pm 7.5\%$ or $\pm 0.75\text{pF}$, whichever is larger. Q: $C \geq 30\text{ pF}$: $Q \geq 200$ $C < 30\text{ pF}$: $Q \geq 100 + 10C/3$ C: Nominal capacitance Insulation resistance: 500 M Ω min.	Appearance: No abnormality Capacitance change: $C \leq 2\text{ pF}$: Within $\pm 0.4\text{ pF}$ $C > 2\text{ pF}$: Within $\pm 0.75\text{ pF}$ C: Nominal capacitance Insulation resistance: 500 M Ω min.	Appearance: No abnormality Capacitance change: B: Within $\pm 12.5\%$ F: Within $\pm 30\%$ $\tan \delta$: B: 5.0% max. F: 7.5% max. Note 4 Insulation resistance: 25 M $\Omega \mu\text{F}$ or 500 M Ω , whichever is the smaller. Note 5	Appearance: No abnormality Capacitance change: BJ: Within $\pm 12.5\%$ C, E, F: Within $\pm 30\%$ Note 4 $\tan \delta$: BJ: 5.0% max. C, E, F: 11% max. Insulation resistance: 25 M $\Omega \mu\text{F}$ or 500 M Ω , whichever is the smaller. Note 5	According to JIS C 5102 Clause 9. 9. Multilayer: Preconditioning: Voltage treatment (Class 2) Temperature: 40 $\pm 2^\circ\text{C}$ Humidity: 90 to 95% RH Duration: 500 $_{-0}^{+24}$ hrs Applied voltage: Rated voltage Charge and discharge current: 50mA max. (Class 1,2) Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24 ± 2 hrs (Class 1) 48 ± 4 hrs (Class 2) High-Frequency Multilayer: Temperature: 60 $\pm 2^\circ\text{C}$ Humidity: 90 to 95% RH Duration: 500 $_{-0}^{+24}$ hrs Applied voltage: Rated voltage Charge and discharge current: 50mA max. Recovery: 24 ± 2 hrs of recovery under the standard condition after the removal from test chamber.
17.Loading at High Temperature	Appearance: No abnormality Capacitance change: Within $\pm 3\%$ or $\pm 0.3\text{pF}$, whichever is larger. Q: $C \geq 30\text{ pF}$: $Q \geq 350$ $10 \leq C < 30\text{ pF}$: $Q \geq 275 + 2.5C$ $C < 10\text{ pF}$: $Q \geq 200 + 10C$ C: Nominal capacitance Insulation resistance: 1000 M Ω min.	Appearance: No abnormality Capacitance change: Within $\pm 3\%$ or $\pm 0.3\text{pF}$, whichever is larger. Insulation resistance: 1000 M Ω min.	Appearance: No abnormality Capacitance change: B: Within $\pm 12.5\%$ F: Within $\pm 30\%$ Note 4 $\tan \delta$: B: 4.0% max. F: 7.5% max. Insulation resistance: 50 M $\Omega \mu\text{F}$ or 1000 M Ω , whichever is smaller. Note 5	Appearance: No abnormality Capacitance change: BJ: Within $\pm 12.5\%$ Within $\pm 20\% \text{***}$ Within $\pm 25\% \text{***}$ C: Within $\pm 25\%$ (X6S) Within $\pm 30\%$ (X5S) E, F: Within $\pm 30\%$ Note 4 $\tan \delta$: BJ: 5.0% max. C, F, F: 11% max. Insulation resistance: 50 M $\Omega \mu\text{F}$ or 1000 M Ω , whichever is smaller. Note 5	According to JIS C 5102 clause 9.10. Multilayer: Preconditioning: Voltage treatment (Class 2) Temperature: 125 $\pm 3^\circ\text{C}$ (Class 1, Class 2: B, BJ(X7R)) 85 $\pm 2^\circ\text{C}$ (Class 2: BJ,F) Duration: 1000 $_{-0}^{+48}$ hrs Applied voltage: Rated voltage $\times 2$ Note 6 Recovery: Recovery for the following period under the standard condition after the removal from test chamber. As for Ni product, thermal treatment shall be performed prior to the recovery. 24 ± 2 hrs (Class 1) 48 ± 4 hrs (Class 2) High-Frequency Multilayer: Temperature: 125 $\pm 3^\circ\text{C}$ (Class 1) Duration: 1000 $_{-0}^{+48}$ hrs Applied voltage: Rated voltage $\times 2$ Recovery: 24 ± 2 hrs of recovery under the standard condition after the removal from test chamber.

Note 1 :For 105 type, specified in "High value".
 Note 2 :Thermal treatment (Multilayer): 1 hr of thermal treatment at 150 ± 0 / -10 $^\circ\text{C}$ followed by 48 ± 4 hrs of recovery under the standard condition shall be performed before the measurement.
 Note 3 :Voltage treatment (Multilayer): 1 hr of voltage treatment under the specified temperature and voltage for testing followed by 48 ± 4 hrs of recovery under the standard condition shall be performed before the measurement.
 Note 4, 5 :The figure indicates typical inspection. Please refer to individual specifications.
 Note 6 :Some of the parts are applicable in rated voltage $\times 1.5$. Please refer to individual specifications.
 Note on standard condition: "standard condition" referred to herein is defined as follows: 5 to 35 $^\circ\text{C}$ of temperature, 45 to 85% relative humidity, and 86 to 106kPa of air pressure.
 When there are questions concerning measurement results: In order to provide correlation data, the test shall be conducted under condition of 20 $\pm 2^\circ\text{C}$ of temperature, 60 to 70% relative humidity, and 86 to 106kPa of air pressure. Unless otherwise specified, all the tests are conducted under the "standard condition."

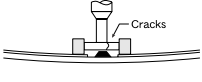
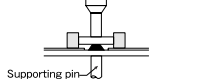
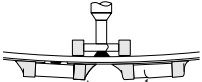
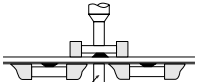
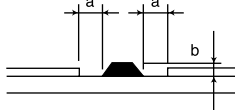
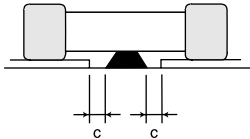
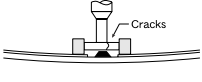
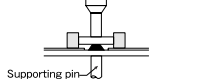
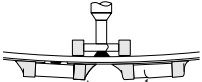
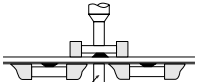
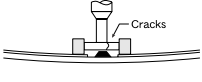
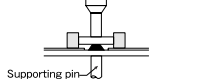
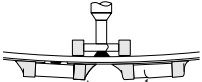
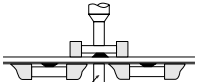
Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations																																																																																																																												
1.Circuit Design	<p>Verification of operating environment, electrical rating and performance</p> <p>1. A malfunction in medical equipment, spacecraft, nuclear reactors, etc. may cause serious harm to human life or have severe social ramifications. As such, any capacitors to be used in such equipment may require higher safety and/or reliability considerations and should be clearly differentiated from components used in general purpose applications.</p> <p>Operating Voltage (Verification of Rated voltage)</p> <p>1. The operating voltage for capacitors must always be lower than their rated values.</p> <p>If an AC voltage is loaded on a DC voltage, the sum of the two peak voltages should be lower than the rated value of the capacitor chosen. For a circuit where both an AC and a pulse voltage may be present, the sum of their peak voltages should also be lower than the capacitor's rated voltage.</p> <p>2. Even if the applied voltage is lower than the rated value, the reliability of capacitors might be reduced if either a high frequency AC voltage or a pulse voltage having rapid rise time is present in the circuit.</p>																																																																																																																													
2.PCB Design	<p>Pattern configurations (Design of Land-patterns)</p> <p>1. When capacitors are mounted on a PCB, the amount of solder used (size of fillet) can directly affect capacitor performance. Therefore, the following items must be carefully considered in the design of solder land patterns:</p> <p>(1) The amount of solder applied can affect the ability of chips to withstand mechanical stresses which may lead to breaking or cracking. Therefore, when designing land-patterns it is necessary to consider the appropriate size and configuration of the solder pads which in turn determines the amount of solder necessary to form the fillets.</p> <p>(2) When more than one part is jointly soldered onto the same land or pad, the pad must be designed so that each component's soldering point is separated by solder-resist.</p>	<p>1.The following diagrams and tables show some examples of recommended patterns to prevent excessive solder amounts.(larger fillets which extend above the component end terminations)</p> <p>Examples of improper pattern designs are also shown.</p> <p>(1) Recommended land dimensions for a typical chip capacitor land patterns for PCBs</p>  <p>Recommended land dimensions for wave-soldering (unit: mm)</p> <table border="1" data-bbox="853 1255 1236 1430"> <thead> <tr> <th>Type</th> <th>107</th> <th>212</th> <th>316</th> <th>325</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Size</td> <td>L</td> <td>1.6</td> <td>2.0</td> <td>3.2</td> <td>3.2</td> </tr> <tr> <td>W</td> <td>0.8</td> <td>1.25</td> <td>1.6</td> <td>2.5</td> </tr> <tr> <td>A</td> <td>0.8~1.0</td> <td>1.0~1.4</td> <td>1.8~2.5</td> <td>1.8~2.5</td> </tr> <tr> <td>B</td> <td>0.5~0.8</td> <td>0.8~1.5</td> <td>0.8~1.7</td> <td>0.8~1.7</td> </tr> <tr> <td>C</td> <td>0.6~0.8</td> <td>0.9~1.2</td> <td>1.2~1.6</td> <td>1.8~2.5</td> </tr> </tbody> </table> <p>Recommended land dimensions for reflow-soldering (unit: mm)</p> <table border="1" data-bbox="845 1496 1380 1681"> <thead> <tr> <th>Type</th> <th>063</th> <th>105</th> <th>107</th> <th>212</th> <th>316</th> <th>325</th> <th>432</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Size</td> <td>L</td> <td>0.6</td> <td>1.0</td> <td>1.6</td> <td>2.0</td> <td>3.2</td> <td>3.2</td> <td>4.5</td> </tr> <tr> <td>W</td> <td>0.3</td> <td>0.5</td> <td>0.8</td> <td>1.25</td> <td>1.6</td> <td>2.5</td> <td>3.2</td> </tr> <tr> <td>A</td> <td>0.20~0.30</td> <td>0.45~0.55</td> <td>0.6~0.8</td> <td>0.8~1.2</td> <td>1.8~2.5</td> <td>1.8~2.5</td> <td>2.5~3.5</td> </tr> <tr> <td>B</td> <td>0.20~0.30</td> <td>0.40~0.50</td> <td>0.6~0.8</td> <td>0.8~1.2</td> <td>1.0~1.5</td> <td>1.0~1.5</td> <td>1.5~1.8</td> </tr> <tr> <td>C</td> <td>0.25~0.40</td> <td>0.45~0.55</td> <td>0.6~0.8</td> <td>0.9~1.6</td> <td>1.2~2.0</td> <td>1.8~3.2</td> <td>2.3~3.5</td> </tr> </tbody> </table> <p>Excess solder can affect the ability of chips to withstand mechanical stresses. Therefore, please take proper precautions when designing land-patterns.</p> <table border="1" data-bbox="853 1747 1189 1921"> <thead> <tr> <th>Type</th> <th>316 (4 circuits)</th> <th>212 (4 circuits)</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Size</td> <td>L</td> <td>3.2</td> <td>2.0</td> </tr> <tr> <td>W</td> <td>1.6</td> <td>1.25</td> </tr> <tr> <td>a</td> <td>0.7~0.9</td> <td>0.5~0.6</td> </tr> <tr> <td>b</td> <td>1</td> <td>0.5~0.6</td> </tr> <tr> <td>c</td> <td>0.4~0.5</td> <td>0.2~0.3</td> </tr> <tr> <td>d</td> <td>0.8</td> <td>0.5</td> </tr> </tbody> </table>  <table border="1" data-bbox="853 1932 1189 2096"> <thead> <tr> <th>Type</th> <th>212 (2 circuits)</th> <th>110 (2 circuits)</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Size</td> <td>L</td> <td>2.0</td> <td>1.37</td> </tr> <tr> <td>W</td> <td>1.25</td> <td>1.0</td> </tr> <tr> <td>a</td> <td>0.5~0.6</td> <td>0.35~0.45</td> </tr> <tr> <td>b</td> <td>0.5~0.6</td> <td>0.55~0.65</td> </tr> <tr> <td>c</td> <td>0.5~0.6</td> <td>0.3~0.4</td> </tr> <tr> <td>d</td> <td>1.0</td> <td>0.64</td> </tr> </tbody> </table> 	Type	107	212	316	325	Size	L	1.6	2.0	3.2	3.2	W	0.8	1.25	1.6	2.5	A	0.8~1.0	1.0~1.4	1.8~2.5	1.8~2.5	B	0.5~0.8	0.8~1.5	0.8~1.7	0.8~1.7	C	0.6~0.8	0.9~1.2	1.2~1.6	1.8~2.5	Type	063	105	107	212	316	325	432	Size	L	0.6	1.0	1.6	2.0	3.2	3.2	4.5	W	0.3	0.5	0.8	1.25	1.6	2.5	3.2	A	0.20~0.30	0.45~0.55	0.6~0.8	0.8~1.2	1.8~2.5	1.8~2.5	2.5~3.5	B	0.20~0.30	0.40~0.50	0.6~0.8	0.8~1.2	1.0~1.5	1.0~1.5	1.5~1.8	C	0.25~0.40	0.45~0.55	0.6~0.8	0.9~1.6	1.2~2.0	1.8~3.2	2.3~3.5	Type	316 (4 circuits)	212 (4 circuits)	Size	L	3.2	2.0	W	1.6	1.25	a	0.7~0.9	0.5~0.6	b	1	0.5~0.6	c	0.4~0.5	0.2~0.3	d	0.8	0.5	Type	212 (2 circuits)	110 (2 circuits)	Size	L	2.0	1.37	W	1.25	1.0	a	0.5~0.6	0.35~0.45	b	0.5~0.6	0.55~0.65	c	0.5~0.6	0.3~0.4	d	1.0	0.64
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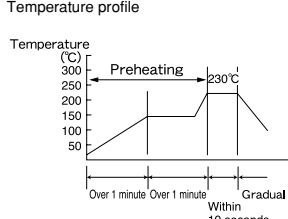
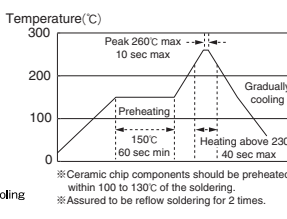
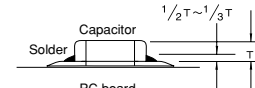
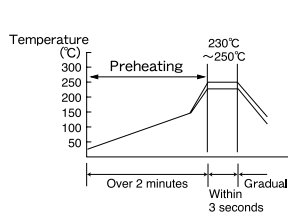
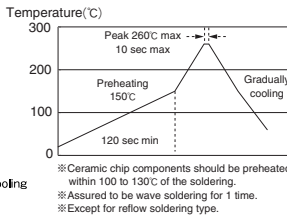
Precautions on the use of Multilayer Ceramic Capacitors

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2.PCB Design	<p>Pattern configurations (Capacitor layout on panelized [breakaway] PC boards)</p> <p>1. After capacitors have been mounted on the boards, chips can be subjected to mechanical stresses in subsequent manufacturing processes (PCB cutting, board inspection, mounting of additional parts, assembly into the chassis, wave soldering the reflow soldered boards etc.) For this reason, planning pattern configurations and the position of SMD capacitors should be carefully performed to minimize stress.</p>	<p>(2) Examples of good and bad solder application</p> <table border="1" data-bbox="849 301 1452 746"> <thead> <tr> <th>Items</th> <th>Not recommended</th> <th>Recommended</th> </tr> </thead> <tbody> <tr> <td>Mixed mounting of SMD and leaded components</td> <td></td> <td></td> </tr> <tr> <td>Component placement close to the chassis</td> <td></td> <td></td> </tr> <tr> <td>Hand-soldering of leaded components near mounted components</td> <td></td> <td></td> </tr> <tr> <td>Horizontal component placement</td> <td></td> <td></td> </tr> </tbody> </table> <p>1-1. The following are examples of good and bad capacitor layout; SMD capacitors should be located to minimize any possible mechanical stresses from board warp or deflection.</p> <table border="1" data-bbox="849 847 1452 1000"> <thead> <tr> <th></th> <th>Not recommended</th> <th>Recommended</th> </tr> </thead> <tbody> <tr> <td>Deflection of the board</td> <td></td> <td> Position the component at a right angle to the direction of the mechanical stresses that are anticipated.</td> </tr> </tbody> </table> <p>1-2. To layout the capacitors for the breakaway PC board, it should be noted that the amount of mechanical stresses given will vary depending on capacitor layout. The example below shows recommendations for better design.</p> <div data-bbox="906 1109 1327 1380" data-label="Diagram">  <p>The diagram illustrates a breakaway PCB layout with five capacitors labeled A, B, C, D, and E. A horizontal line with four circles represents a perforation. A vertical line with a gap represents a slit. Capacitors A and B are positioned below the perforation, while C, D, and E are above it. The stress magnitude is indicated as $A > B = C > D > E$.</p> </div> <p>1-3. When breaking PC boards along their perforations, the amount of mechanical stress on the capacitors can vary according to the method used. The following methods are listed in order from least stressful to most stressful: push-back, slit, V-grooving, and perforation. Thus, any ideal SMD capacitor layout must also consider the PCB splitting procedure.</p>	Items	Not recommended	Recommended	Mixed mounting of SMD and leaded components			Component placement close to the chassis			Hand-soldering of leaded components near mounted components			Horizontal component placement				Not recommended	Recommended	Deflection of the board		 Position the component at a right angle to the direction of the mechanical stresses that are anticipated.
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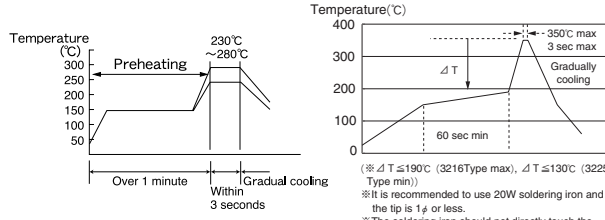
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<p>3. Considerations for automatic placement</p>	<p>Adjustment of mounting machine</p> <ol style="list-style-type: none"> Excessive impact load should not be imposed on the capacitors when mounting onto the PC boards. The maintenance and inspection of the mounters should be conducted periodically. <p>Selection of Adhesives</p> <ol style="list-style-type: none"> Mounting capacitors with adhesives in preliminary assembly, before the soldering stage, may lead to degraded capacitor characteristics unless the following factors are appropriately checked; the size of land patterns, type of adhesive, amount applied, hardening temperature and hardening period. Therefore, it is imperative to consult the manufacturer of the adhesives on proper usage and amounts of adhesive to use. 	<ol style="list-style-type: none"> If the lower limit of the pick-up nozzle is low, too much force may be imposed on the capacitors, causing damage. To avoid this, the following points should be considered before lowering the pick-up nozzle: <ol style="list-style-type: none"> The lower limit of the pick-up nozzle should be adjusted to the surface level of the PC board after correcting for deflection of the board. The pick-up pressure should be adjusted between 1 and 3 N static loads. To reduce the amount of deflection of the board caused by impact of the pick-up nozzle, supporting pins or back-up pins should be used under the PC board. The following diagrams show some typical examples of good pick-up nozzle placement: <table border="1" data-bbox="849 526 1452 797"> <thead> <tr> <th></th> <th>Not recommended</th> <th>Recommended</th> </tr> </thead> <tbody> <tr> <td>Single-sided mounting</td> <td></td> <td></td> </tr> <tr> <td>Double-sided mounting</td> <td></td> <td></td> </tr> </tbody> </table> <ol style="list-style-type: none"> As the alignment pin wears out, adjustment of the nozzle height can cause chipping or cracking of the capacitors because of mechanical impact on the capacitors. To avoid this, the monitoring of the width between the alignment pin in the stopped position, and maintenance, inspection and replacement of the pin should be conducted periodically. <ol style="list-style-type: none"> Some adhesives may cause reduced insulation resistance. The difference between the shrinkage percentage of the adhesive and that of the capacitors may result in stresses on the capacitors and lead to cracking. Moreover, too little or too much adhesive applied to the board may adversely affect component placement, so the following precautions should be noted in the application of adhesives. <ol style="list-style-type: none"> Required adhesive characteristics <ol style="list-style-type: none"> The adhesive should be strong enough to hold parts on the board during the mounting & solder process. The adhesive should have sufficient strength at high temperatures. The adhesive should have good coating and thickness consistency. The adhesive should be used during its prescribed shelf life. The adhesive should harden rapidly The adhesive must not be contaminated. The adhesive should have excellent insulation characteristics. The adhesive should not be toxic and have no emission of toxic gasses. The recommended amount of adhesives is as follows; <table border="1" data-bbox="852 1469 1404 1589"> <thead> <tr> <th>Figure</th> <th>212/316 case sizes as examples</th> </tr> </thead> <tbody> <tr> <td>a</td> <td>0.3mm min</td> </tr> <tr> <td>b</td> <td>100 ~ 120 μm</td> </tr> <tr> <td>c</td> <td>Adhesives should not contact the pad</td> </tr> </tbody> </table> <div style="display: flex; justify-content: space-around; margin-top: 20px;"> <div data-bbox="874 1664 1109 1808"> <p>Amount of adhesive</p>  </div> <div data-bbox="1173 1664 1423 1852"> <p>After capacitors are bonded</p>  </div> </div>		Not recommended	Recommended	Single-sided mounting			Double-sided mounting			Figure	212/316 case sizes as examples	a	0.3mm min	b	100 ~ 120 μm	c	Adhesives should not contact the pad
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<p>4. Soldering</p>	<p>Selection of Flux</p> <p>1. Since flux may have a significant effect on the performance of capacitors, it is necessary to verify the following conditions prior to use;</p> <p>(1) Flux used should be with less than or equal to 0.1 wt% (equivalent to chlorine) of halogenated content. Flux having a strong acidity content should not be applied.</p> <p>(2) When soldering capacitors on the board, the amount of flux applied should be controlled at the optimum level.</p> <p>(3) When using water-soluble flux, special care should be taken to properly clean the boards.</p> <p>Soldering</p> <p>Temperature, time, amount of solder, etc. are specified in accordance with the following recommended conditions.</p> <p>And please contact us about peak temperature when you use lead-free paste.</p>	<p>1-1. When too much halogenated substance (Chlorine, etc.) content is used to activate the flux, or highly acidic flux is used, an excessive amount of residue after soldering may lead to corrosion of the terminal electrodes or degradation of insulation resistance on the surface of the capacitors.</p> <p>1-2. Flux is used to increase solderability in flow soldering, but if too much is applied, a large amount of flux gas may be emitted and may detrimentally affect solderability. To minimize the amount of flux applied, it is recommended to use a flux-bubbling system.</p> <p>1-3. Since the residue of water-soluble flux is easily dissolved by water content in the air, the residue on the surface of capacitors in high humidity conditions may cause a degradation of insulation resistance and therefore affect the reliability of the components. The cleaning methods and the capability of the machines used should also be considered carefully when selecting water-soluble flux.</p> <p>1-1. Preheating when soldering</p> <p>Heating: Ceramic chip components should be preheated to within 100 to 130°C of the soldering.</p> <p>Cooling: The temperature difference between the components and cleaning process should not be greater than 100°C.</p> <p>Ceramic chip capacitors are susceptible to thermal shock when exposed to rapid or concentrated heating or rapid cooling. Therefore, the soldering process must be conducted with great care so as to prevent malfunction of the components due to excessive thermal shock.</p> <p>Recommended conditions for soldering</p> <p>[Reflow soldering]</p> <p>Temperature profile</p>   <p>※ Ceramic chip components should be preheated to within 100 to 130°C of the soldering. ※ Assured to be reflow soldering for 2 times.</p> <p>Caution</p> <p>1. The ideal condition is to have solder mass (fillet) controlled to 1/2 to 1/3 of the thickness of the capacitor, as shown below:</p>  <p>PC board</p> <p>2. Because excessive dwell times can detrimentally affect solderability, soldering duration should be kept as close to recommended times as possible.</p> <p>[Wave soldering]</p> <p>Temperature profile</p>   <p>※ Ceramic chip components should be preheated to within 100 to 130°C of the soldering. ※ Assured to be wave soldering for 1 time. ※ Except for reflow soldering type.</p> <p>Caution</p> <p>1. Make sure the capacitors are preheated sufficiently.</p> <p>2. The temperature difference between the capacitor and melted solder should not be greater than 100 to 130°C</p> <p>3. Cooling after soldering should be as gradual as possible.</p> <p>4. Wave soldering must not be applied to the capacitors designated as for reflow soldering only.</p>

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
4. Soldering		<p>[Hand soldering]</p> <p>Temperature profile</p>  <p>Caution</p> <ol style="list-style-type: none"> 1. Use a 20W soldering iron with a maximum tip diameter of 1.0 mm. 2. The soldering iron should not directly touch the capacitor.
5. Cleaning	<p>Cleaning conditions</p> <ol style="list-style-type: none"> 1. When cleaning the PC board after the capacitors are all mounted, select the appropriate cleaning solution according to the type of flux used and purpose of the cleaning (e.g. to remove soldering flux or other materials from the production process.) 2. Cleaning conditions should be determined after verifying, through a test run, that the cleaning process does not affect the capacitor's characteristics. 	<ol style="list-style-type: none"> 1. The use of inappropriate solutions can cause foreign substances such as flux residue to adhere to the capacitor or deteriorate the capacitor's outer coating, resulting in a degradation of the capacitor's electrical properties (especially insulation resistance). 2. Inappropriate cleaning conditions (insufficient or excessive cleaning) may detrimentally affect the performance of the capacitors. <p>(1)Excessive cleaning</p> <p>In the case of ultrasonic cleaning, too much power output can cause excessive vibration of the PC board which may lead to the cracking of the capacitor or the soldered portion, or decrease the terminal electrodes' strength. Thus the following conditions should be carefully checked;</p> <p>Ultrasonic output Below 20 W/ℓ Ultrasonic frequency Below 40 kHz Ultrasonic washing period 5 min. or less</p>
6. Post cleaning processes	<ol style="list-style-type: none"> 1. With some type of resins a decomposition gas or chemical reaction vapor may remain inside the resin during the hardening period or while left under normal storage conditions resulting in the deterioration of the capacitor's performance. 2. When a resin's hardening temperature is higher than the capacitor's operating temperature, the stresses generated by the excess heat may lead to capacitor damage or destruction. The use of such resins, molding materials etc. is not recommended. 	
7. Handling	<p>Breakaway PC boards (splitting along perforations)</p> <ol style="list-style-type: none"> 1. When splitting the PC board after mounting capacitors and other components, care is required so as not to give any stresses of deflection or twisting to the board. 2. Board separation should not be done manually, but by using the appropriate devices. <p>Mechanical considerations</p> <ol style="list-style-type: none"> 1. Be careful not to subject the capacitors to excessive mechanical shocks. <ol style="list-style-type: none"> (1)If ceramic capacitors are dropped onto the floor or a hard surface, they should not be used. (2)When handling the mounted boards, be careful that the mounted components do not come in contact with or bump against other boards or components. 	

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations				
8.Storage conditions	<p>Storage</p> <p>1. To maintain the solderability of terminal electrodes and to keep the packaging material in good condition, care must be taken to control temperature and humidity in the storage area. Humidity should especially be kept as low as possible.</p> <p>• Recommended conditions</p> <table border="0"> <tr> <td>Ambient temperature</td> <td>Below 40°C</td> </tr> <tr> <td>Humidity</td> <td>Below 70% RH</td> </tr> </table> <p>The ambient temperature must be kept below 30°C. Even under ideal storage conditions capacitor electrode solderability decreases as time passes, so should be used within 6 months from the time of delivery.</p> <p>• Ceramic chip capacitors should be kept where no chlorine or sulfur exists in the air.</p> <p>2. The capacitance value of high dielectric constant capacitors (type 2 &3) will gradually decrease with the passage of time, so this should be taken into consideration in the circuit design. If such a capacitance reduction occurs, a heat treatment of 150°C for 1hour will return the capacitance to its initial level.</p>	Ambient temperature	Below 40°C	Humidity	Below 70% RH	<p>1. If the parts are stored in a high temperature and humidity environment, problems such as reduced solderability caused by oxidation of terminal electrodes and deterioration of taping/packaging materials may take place. For this reason, components should be used within 6 months from the time of delivery. If exceeding the above period, please check solderability before using the capacitors.</p>
Ambient temperature	Below 40°C					
Humidity	Below 70% RH					