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RoHS
Available on commercial versions

NPN MEDIUM POWER SILICON TRANSISTOR

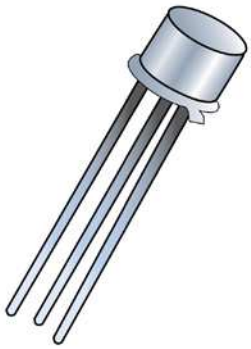
Qualified per MIL-PRF-19500/393

Qualified Levels:
JAN, JANTX and JANTXV

DESCRIPTION

This family of high-frequency, epitaxial planar transistors feature low saturation voltage. These devices are also available in TO-5 and low profile U4 packages. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website http://www.microsemi.com.



TO-39 (TO-205AD) Package

FEATURES

- JEDEC registered 2N3418 through 2N3421 series.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/393.
- RoHS compliant versions available (commercial grade only).
- $V_{CE(sat)}$ = 0.25 V @ Ic = 1 A.
- Rise time t_r = 0.22 µs max @ I_C = 1.0 A, I_{B1} = 100 mA.
- Fall time t_f = 0.20 µs max @ I_C = 1.0 A, I_{B2} = -10 0 mA.

APPLICATIONS / BENEFITS

- General purpose transistors for medium power applications requiring high frequency switching and low package profile.
- Military and other high-reliability applications.

Also available in:

TO-5 package
(leaded)
2N3418 – 2N3421

U4 package
(surface mount)
2N3418U4 – 2N3421U4

MAXIMUM RATINGS

Parameters / Test Conditions	Symbol	2N3418S 2N3420S	2N3419S 2N3421S	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	V
Collector-Base Voltage	V_{CBO}	85	125	V
Emitter-Base Voltage	V_{EBO}	8		V
Collector Current tp <= 1 ms, duty cycle <= 50%	I_C	3 5		A
Total Power Dissipation @ T_A = +25 °C (1) @ T_C = +100 °C (2)	P_D	1 5		W
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

Notes: 1. Derate linearly 5.72 mW/°C for T_A > +25 °C.
2. Derate linearly 150 mW/°C for T_C > +100 °C.

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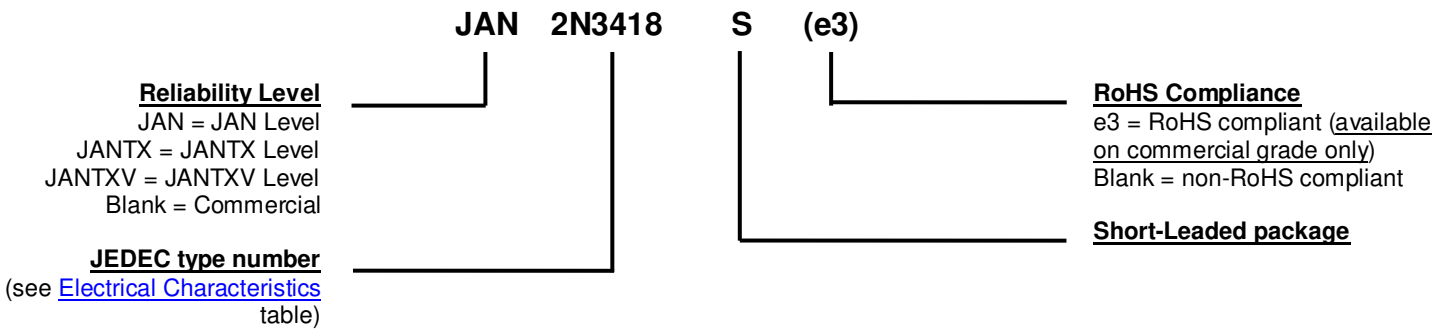
Website:
www.microsemi.com

MECHANICAL and PACKAGING

- CASE: Hermetically sealed, kovar base, nickel cap.
- MARKING: Part number, date code, manufacturer's ID.
- POLARITY: See Package Dimensions on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS

Symbol	Definition
C_{obo}	Common-base open-circuit output capacitance.
I_{CEO}	Collector cutoff current, base open.
I_{CEX}	Collector cutoff current, circuit between base and emitter.
I_{EBO}	Emitter cutoff current, collector open.
h_{FE}	Common-emitter static forward current transfer ratio.
T_A	Ambient temperature, free-air temperature.
V_{CEO}	Collector-emitter voltage, base open.
V_{CBO}	Collector-emitter voltage, emitter open.
V_{EBO}	Emitter-base voltage, collector open.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted)

OFF CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Collector-Emitter Breakdown Current I_C = 50 mA, I_B = 0	2N3418S, 2N3420S 2N3419S, 2N3421S	$V_{(BR)CEO}$	60 80		V
Collector-Emitter Cutoff Current V_{BE} = -0.5 V, V_{CE} = 80 V V_{BE} = -0.5 V, V_{CE} = 120 V	2N3418S, 2N3420S 2N3419S, 2N3421S	I_{CEX}		0.3 0.3	µA
Collector-Base Cutoff Current V_{CE} = 45 V, I_B = 0 V_{CE} = 60 V, I_B = 0	2N3418S, 2N3420S 2N3419S, 2N3421S	I_{CEO}		5.0 5.0	µA
Emitter-Base Cutoff Current V_{EB} = 6.0 V, I_C = 0 V_{EB} = 8.0 V, I_C = 0		I_{EBO}		0.5 10	µA

ON CHARACTERISTICS (1)

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Forward-Current Transfer Ratio					
I_C = 100 mA, V_{CE} = 2.0 V	2N3418S, 2N3419S 2N3420S, 2N3421S		20 40		
I_C = 1.0 A, V_{CE} = 2.0 V	2N3418S, 2N3419S 2N3420S, 2N3421S		20 40	60 120	
I_C = 2.0 A, V_{CE} = 2.0 V	2N3418S, 2N3419S 2N3420S, 2N3421S	h_{FE}	15 30		
I_C = 5.0 A, V_{CE} = 5.0 V	2N3418S, 2N3419S 2N3420S, 2N3421S		10 15		
Collector-Emitter Saturation Voltage I_C = 1.0 A, I_B = 0.1 A I_C = 2.0 A, I_B = 0.2 A		$V_{CE(sat)}$		0.25 0.5	V
Base-Emitter Saturation Voltage I_C = 1.0 A, I_B = 0.1 A I_C = 2.0 A, I_B = 0.2 A		$V_{BE(sat)}$	0.6 0.7	1.2 1.4	V

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio I_C = 0.1 A, V_{CE} = 10 V, f = 20 MHz	$\|h_{fe}\|$	1.3	0.8	
Output Capacitance V_{CB} = 10 V, I_E = 0, 100 kHz ≤ f ≤ 1.0 MHz	C_{obo}		150	pF

NOTES: (1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.

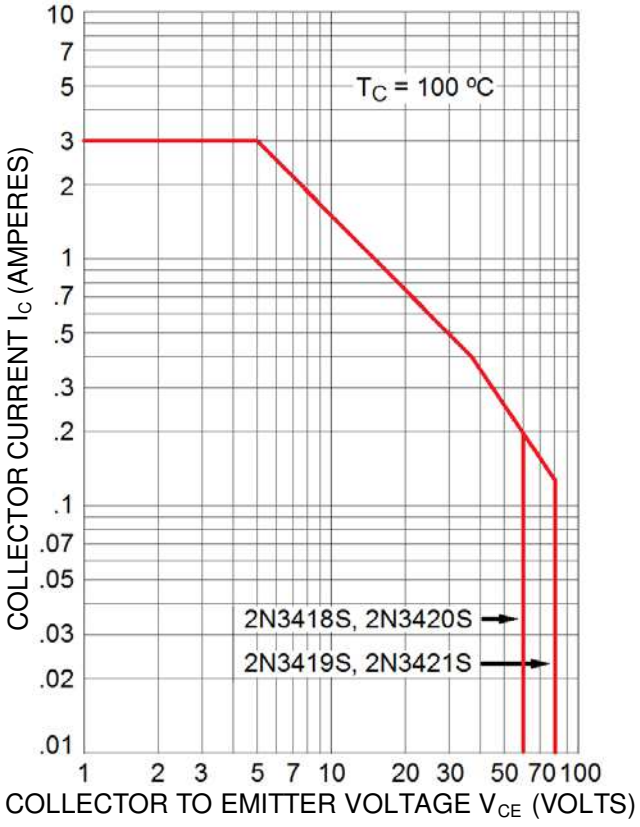
ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted) continued

SWITCHING CHARACTERISTICS

Parameters / Test Conditions (for all symbols)		Symbol	Min.	Max.	Unit
Delay Time Rise Time	$V_{BE(off)}$ = -3.7 V, I_C = 1.0 A, I_{B1} = 100 mA	t_d t_r		0.08 0.22	µs
Storage Time Fall Time	$V_{BE(off)}$ = -3.7 V, I_C = 1.0 A, I_{B2} = -100 mA	t_s t_f		1.10 0.20	µs
Turn-Off Time	$V_{BE(off)}$ = -3.7 V, I_C = 1.0 A, I_{B2} = -100 mA, R_L = 20 Ω	t_{off}		1.20	µs

SAFE OPERATING AREA (See graph below and reference MIL-STD-750, method 3053)

DC Test
T_C = +100 °C, 1 cycle, t ≥ 1.0 s
Test 1
V_{CE} = 5.0 V, I_C = 3.0 A
Test 2
V_{CE} = 37 V, I_C = 0.4 A
Test 3
V_{CE} = 60 V, I_C = 0.185 A — 2N3418S, 2N3420S
V_{CE} = 80 V, I_C = 0.12 A — 2N3419S, 2N3421S
Clamped Switching — T_A = +25 °C, I_B = 0.5 A, I_C = 3.0 A



Maximum Safe Operating Area (continuous dc)

GRAPHS

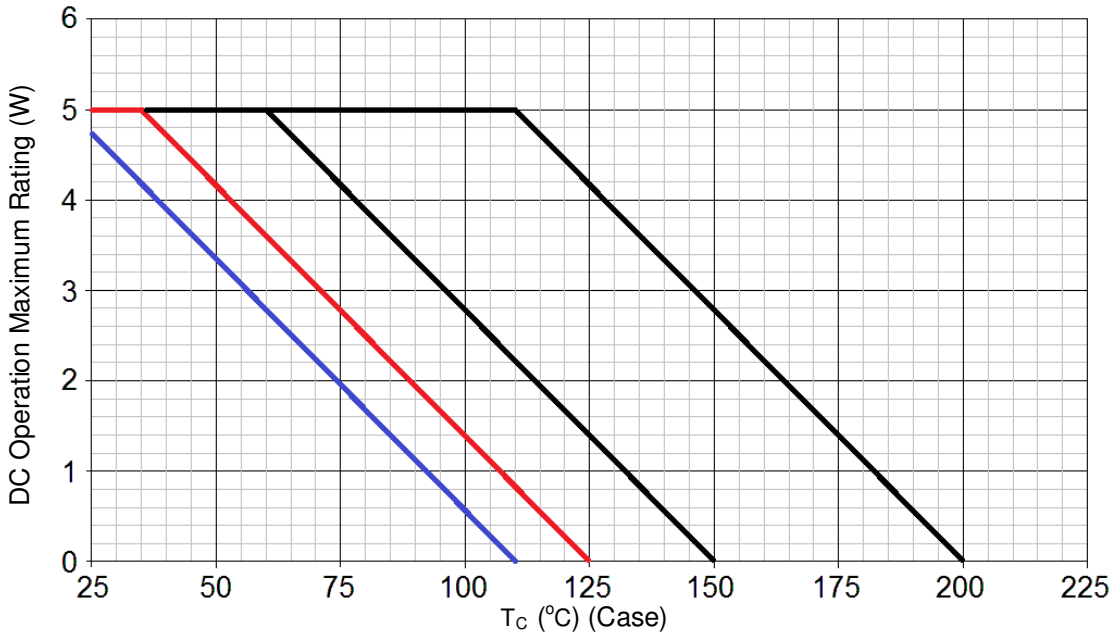


FIGURE 1
Temperature-Power Derating Curve
NOTES: Thermal Resistance Junction to Case = 4.5 °C/W
Max Finish-Alloy Temp = 175.0 °C

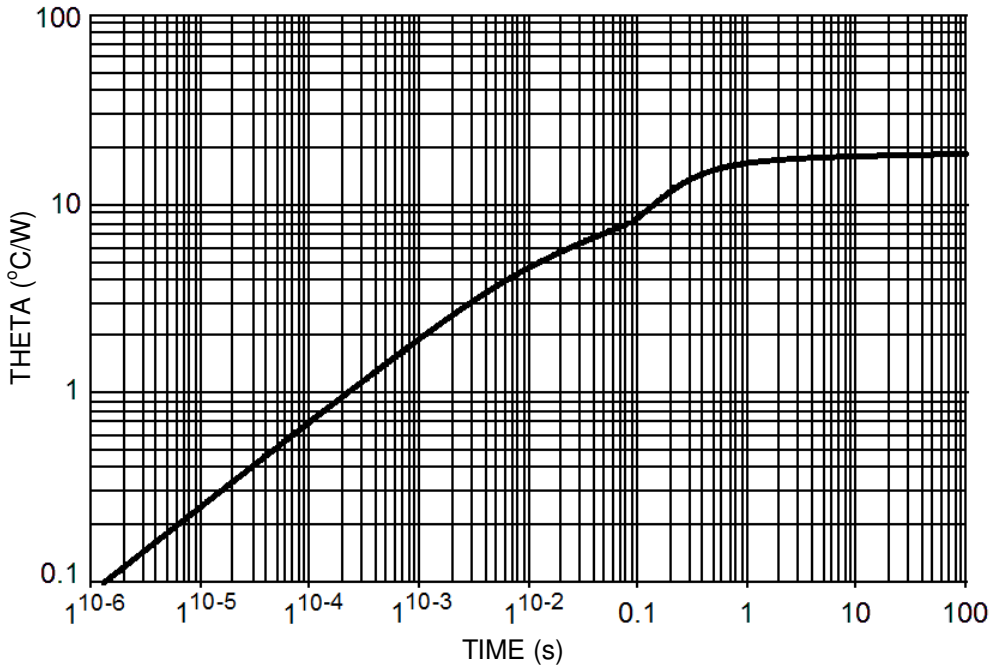
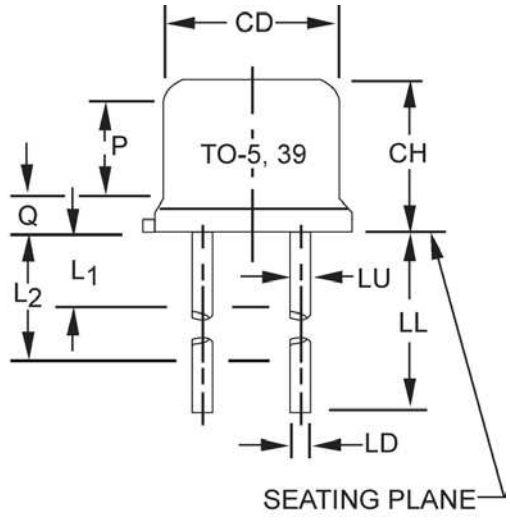
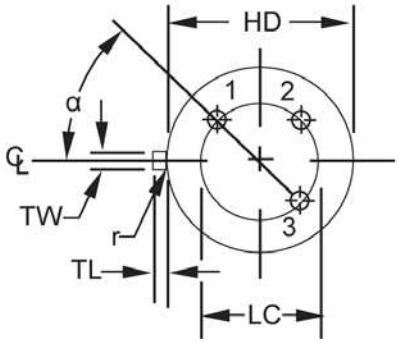


FIGURE 2
Maximum Thermal Impedance
NOTE: T_C = +25 °C, Thermal Resistance $R_{\theta JC}$ = 4.5 °C/W

PACKAGE DIMENSIONS





Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	
LL	.500	.750	12.7	19.05	7
LU	See notes 7, 13, 14				
L_1		.050		1.27	7
L_2	.250		6.35		7
P	.100		2.54		5
Q		.040		1.02	4
TL	.029	.045	0.74	1.14	3, 10
TW	.028	.034	0.71	.86	9, 10
r		.010		0.25	11
α	45° TP		45° TP		6

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LU applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. Lead number 3 is electrically connected to case.
9. Beyond r maximum, TW shall be held for a minimum length of .021 inch (0.53 mm).
10. Lead number 4 omitted on this variation.
11. Symbol r applied to both inside corners of tab.
12. For transistor types 2N3418S, 2N3419S, 2N3420S, 2N3421S, LL is .500 (12.70 mm) minimum and .750 (19.05 mm) maximum.
13. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
14. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.