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Data Sheet: JN5139-001 and JN5139-Z01

IEEE802.15.4 and ZigBee Wireless Microcontrollers

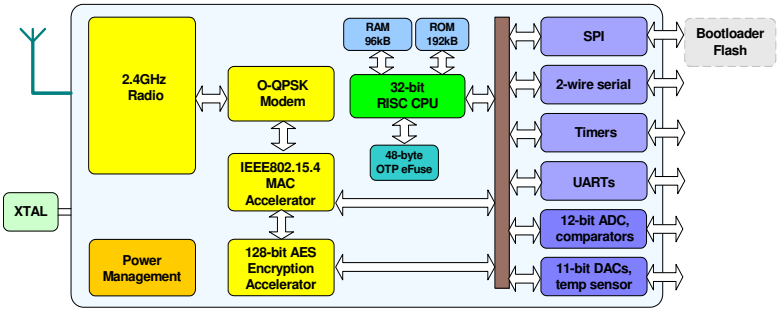
Overview

The JN5139 is a low power, low cost wireless microcontroller suitable for IEEE802.15.4 and ZigBee applications. The device integrates a 32-bit RISC processor, with a fully compliant 2.4GHz IEEE802.15.4 transceiver, 192kB of ROM, 96kB of RAM, and a rich mixture of analogue and digital peripherals.

The cost sensitive ROM/RAM architecture supports the storage of system software, including protocol stacks, routing tables and application code/data. An external flash memory may be used to store application code that will be bootloaded into internal RAM and executed at runtime.

The device integrates hardware MAC and AES encryption accelerators, power saving and timed sleep modes, and mechanisms for security key and program code encryption. These features all make for a highly efficient, low power, single chip wireless microcontroller for battery-powered applications.

Block Diagram



Benefits

- Single chip integrates transceiver and microcontroller for wireless sensor networks
- Cost sensitive ROM/RAM architecture, meets needs for volume application
- System BOM is low in component count and cost
- Hardware MAC ensures low power consumption and low processor overhead
- Extensive user peripherals

Applications

- Robust and secure low power wireless applications
- Wireless sensor networks, particularly IEEE802.15.4 and ZigBee systems
- Home and commercial building automation
- Remote Control
- Toys and gaming peripherals
- Industrial systems
- Telemetry and utilities (e.g. AMR)

Features: Transceiver

- 2.4GHz IEEE802.15.4 compliant
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- Integrated power management and sleep oscillator for low power
- On-chip power regulation for 2.2V to 3.6V battery operation
- Deep sleep current 60nA
- Sleep current with active sleep timer 1.2µA
- Needs minimum of external components (< US$1 cost)
- Rx current 37mA
- Tx current 38mA
- Receiver sensitivity -97dBm
- Transmit power +3dBm

Features: Microcontroller

- 32-bit RISC processor sustains up to 16MIPs with low power
- 192kB ROM stores system firmware that includes Bootloader, and IEEE802.15.4 MAC
- 96kB RAM stores system data and bootloaded application code
- 48-byte OTP eFuse supporting AES based code encryption feature
- 4-input 12-bit ADC, 2 11-bit DACs, 2 comparators
- 2 Application timer/counters, 3 system timers
- 2 UARTs (one for debug)
- SPI port with 5 selects
- 2-wire serial interface
- Up to 21 DIO
- Pin compatible with JN5121

Industrial temperature range (-40°C to +85°C)

8x8mm 56-lead QFN

Lead-free and RoHS compliant

1 Introduction

The JN5139-001 and JN5139-Z01 are IEEE802.15.4 wireless microcontrollers that provide a fully integrated solution for applications using the IEEE802.15.4 and ZigBee standards in the 2.4 - 2.5GHz ISM frequency band [1]. They include all of the functionality required to meet the IEEE802.15.4 specification and have additional processor capability to run a wide range of applications including but not limited to Remote Control, Home and Building Automation, Toys and Gaming. The following table explains which software stack is compatible with which chip variant:

ROM Variant	802.15.4	JenNet	ZigBee 04
001	✓	✓	
Z01	✓	✓	✓

The devices include a Wireless Transceiver, RISC CPU, on-chip memory and an extensive range of peripherals.

Hereafter, the JN5139-001 and JN5139-Z01 will be referred to collectively as JN5139.

1.1 Wireless Microcontroller

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimise this complexity, Jennic provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN5139. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, the register details of the JN5139 are not provided in the datasheet.

1.2 Wireless Transceiver

The Wireless Transceiver is highly integrated and, together with the integrated IEEE802.15.4 MAC library contained in ROM requires little knowledge of RF or wireless design.

The Wireless Transceiver comprises a low-IF 2.45GHz radio, an O-QPSK modem, a baseband controller and a security coprocessor. The radio has a 200Ω resistive differential antenna port that includes all the required matching components on-chip, allowing a differential antenna to be connected directly to the port, minimising the system BOM costs. Connection to a single ported antenna can be achieved using a 200/50Ω 2.45GHz balun. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realised very easily.

The security coprocessor provides hardware-based 128-bit AES-CCM* modes, as specified by the IEEE802.15.4-2006 standard. Specifically, this includes encryption and authentication covered by the MIC -32/-64/-128, ENC and ENC-MIC-32/-64/-128 modes of operation.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 Medium Access Control under the control of a protocol stack.

(1) AES-CBC processing is only available off-line for use under software control.

1.3 RISC CPU and Memory

A 32-bit RISC CPU allows software to be run on-chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN5139 has a unified memory architecture, code memory, data memory, peripheral devices and I/O ports are organized within the same linear address space. The device contains 192kBytes of ROM, 96kBytes of RAM and a 48-byte OTP eFuse memory.

1.4 Peripherals

The following peripherals are available on-chip:

- Master SPI port with five select outputs
- Two UARTs
- Two programmable Timer/Counters with capture/compare facility
- Two programmable Sleep Timers and a Tick Timer
- Two-wire serial interface (compatible with SMbus and I^2C)
- Slave SPI port (shared with digital I/O)
- Twenty-one digital I/O lines (multiplexed with UARTs, timers and SPI selects)
- Four-channel, 12-bit, Analogue-to-Digital converter
- Two 11-bit Digital-to-Analogue converters
- Two programmable analogue comparators
- Internal temperature sensor and battery monitor

1.5 Block Diagram

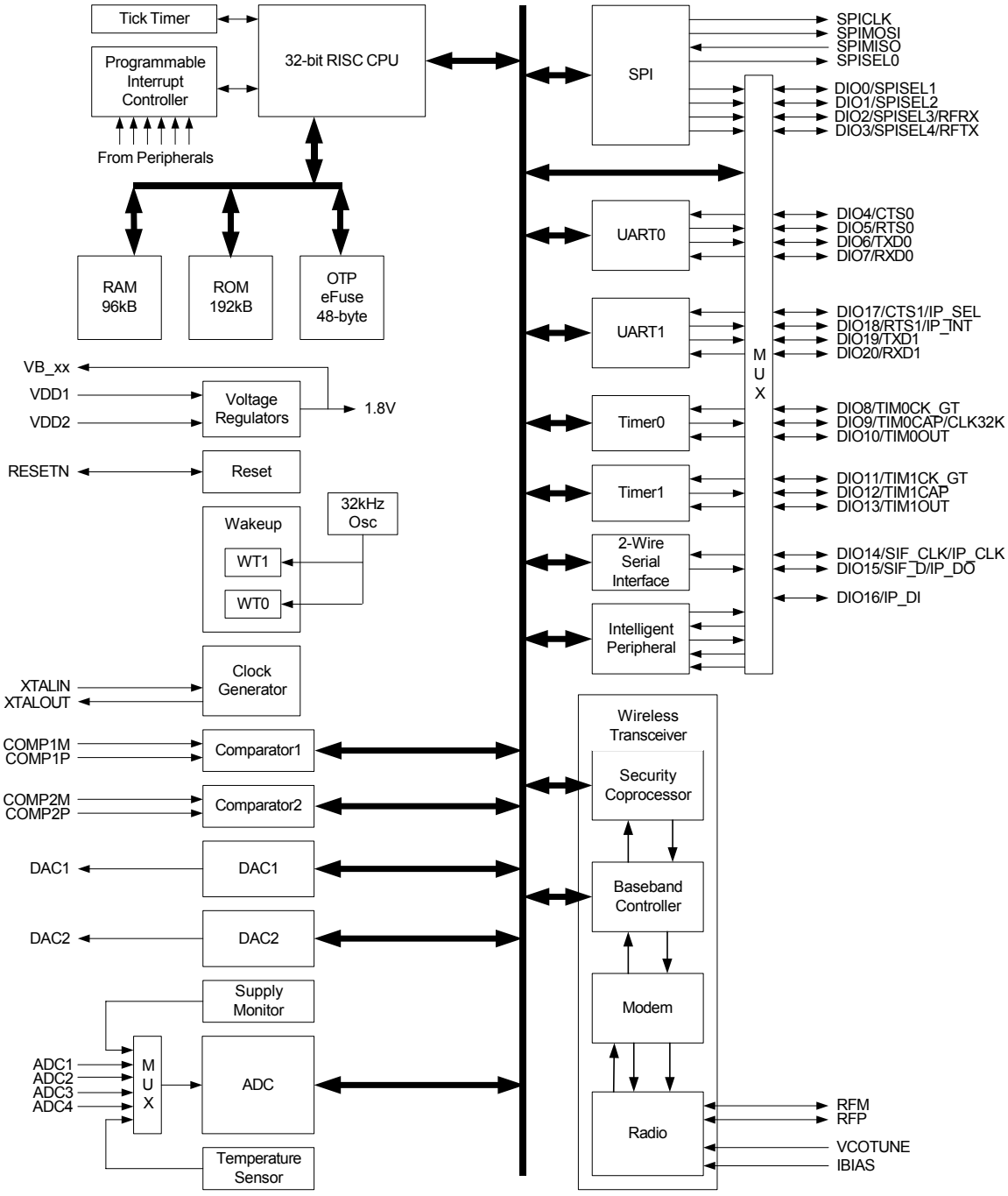


Figure 1: JN5139 Block Diagram

2 Pin Configurations

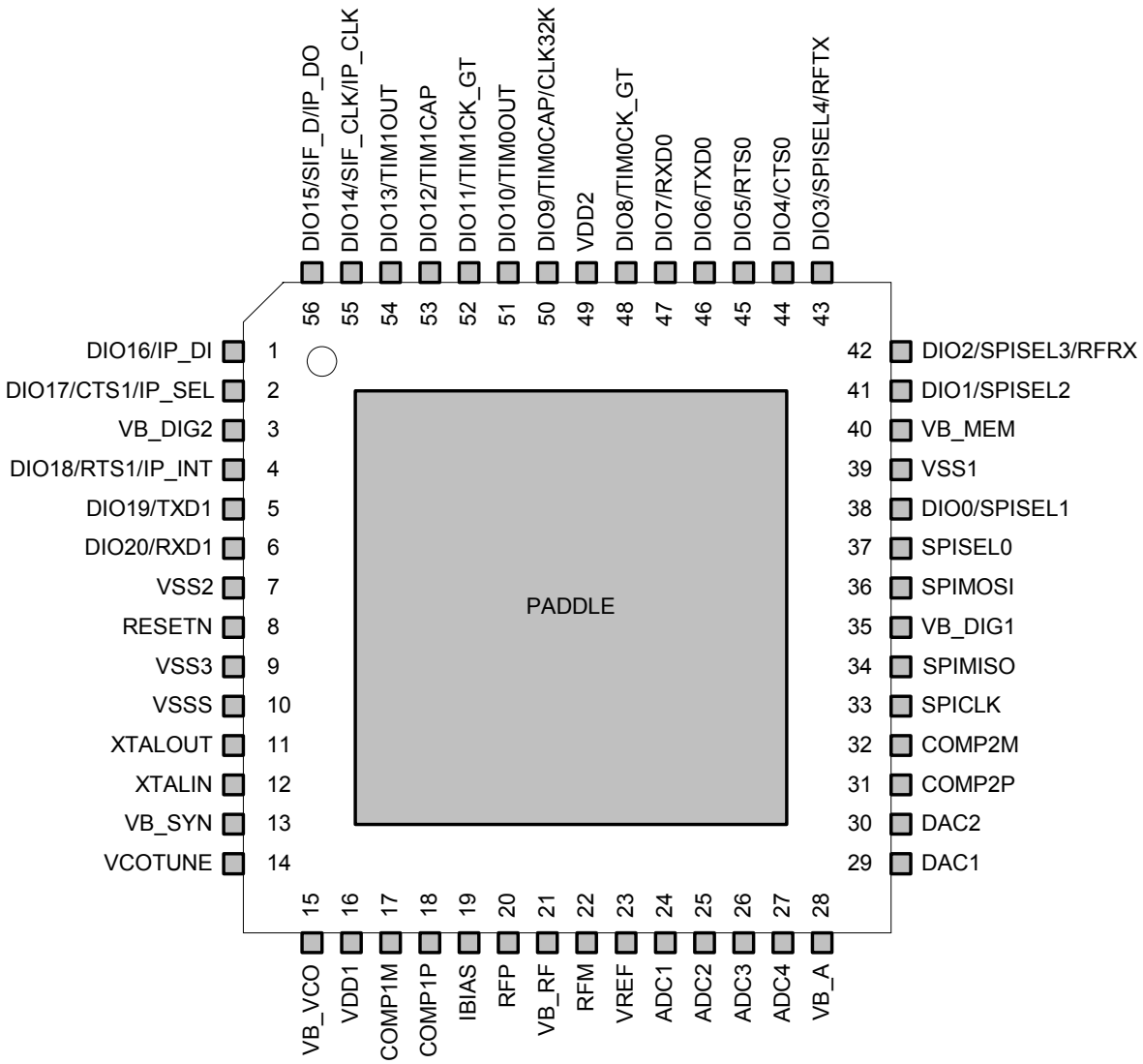


Figure 2: 56-pin QFN Configuration (top view)

Note: Please refer to Appendix B.3 for important applications information regarding the connection of the PADDLE to the PCB.

2.1 Pin Assignment

Pin No	Power supplies		Description
3, 13, 15, 21 28, 35, 40	VB_DIG2, VB_SYN, VB_VCO, VB_RF, VB_A, VB_DIG1, VB_MEM		Regulated supply voltage
16, 49	VDD1, VDD2		Device supplies: VDD1 for analogue, VDD2 for digital
7,9,10,39, PADDLE	VSS2, VSS3, VSSS, VSS1, VSSA		Device grounds
	General		
8	RESETN		Reset output/input
11, 12	XTALOUT, XTALIN		System crystal oscillator
	Radio		
14	VCOTUNE		VCO tuning RC network
19	IBIAS		Bias current control
20, 22	RFP, RFM		Differential antenna port
	Analogue Peripheral I/O		
24, 25, 26, 27	ADC1, ADC2, ADC3, ADC4		ADC inputs
23	VREF		Analogue peripheral reference voltage
29, 30	DAC1, DAC2		DAC outputs
17, 18, 31, 32	COMP1M, COMP1P, COMP2P, COMP2M		Comparator inputs
	Digital I/O		
	Function	**Alternate Function(s)**	
33	SPICLK		SPI Clock
36	SPIMOSI		SPI Master Out Slave In
34	SPIMISO		SPI Master In Slave Out
37	SPISEL0		SPI Slave Select Output 0
38	DIO0	SPISEL1	DIO0 or SPI Slave Select Output 1
41	DIO1	SPISEL2	DIO1 or SPI Slave Select Output 2
42	DIO2	SPISEL3, RFRX	DIO2 or SPI Slave Select Output 3 or Radio Receive Control Output
43	DIO3	SPISEL4, RFTX	DIO3 or SPI Slave Select Output 4 or Radio Transmit Control Output
44	DIO4	CTS0	DIO4 or UART 0 Clear To Send Input
45	DIO5	RTS0	DIO5 or UART 0 Request To Send Output
46	DIO6	TXD0	DIO6 or UART 0 Transmit Data Output
47	DIO7	RXD0	DIO7 or UART 0 Receive Data Input
48	DIO8	TIM0CK_GT	DIO8 or Timer0 Clock/Gate Input
50	DIO9	TIM0CAP,CLK32K	DIO9 or Timer0 Capture Input or CLK32K
51	DIO10	TIM0OUT	DIO10 or Timer0 PWM Output
52	DIO11	TIM1CK_GT	DIO11 or Timer1 Clock/Gate Input
53	DIO12	TIM1CAP, ADO	DIO12 or Timer1 Capture Input or Antenna Diversity Output
54	DIO13	TIM1OUT	DIO13 or Timer1 PWM Output
55	DIO14	SIF_CLK, IP_CLK	DIO14 or Serial Interface Clock or Intelligent Peripheral Clock Input
56	DIO15	SIF_D, IP_DO	DIO15 or Serial Interface Data or Intelligent Peripheral Data Out
1	DIO16	IP_DI	DIO16 or Intelligent Peripheral Data In
2	DIO17	CTS1, IP_SEL	DIO17 or UART 1 Clear To Send Input or Intelligent Peripheral Device Select Input
4	DIO18	RTS1, IP_INT	DIO18 or UART 1 Request To Send Output or Intelligent Peripheral Interrupt Output
5	DIO19	TXD1	DIO19 or UART 1 Transmit Data Output
6	DIO20	RXD1	DIO20 or UART 1 Receive Data Input

2.2 Pin Descriptions

2.2.1 Power Supplies

The device is powered from the VDD1 and VDD2 pins, each being decoupled with a 100nF ceramic capacitor. VDD1 is the power supply to the analogue circuitry; it should be decoupled to ground. VDD2 is the power supply for the digital circuitry; it should be decoupled to ground. A 10uF tantalum capacitor is required at the common ground star point of analogue and digital supplies. Decoupling pins for the internal 1.8V regulators are provided which require a 100nF capacitor located as close to the device as practical. VB_VCO, VB_RF, VB_A and VB_SYN should be decoupled to analogue ground, while VB_MEM, VB_DIG1 and VB_DIG2 should be decoupled to ground. VB_SYN and VB_RF also require an additional 47pF capacitor. See also Appendix B for connection details.

VSSA is the analogue ground, connected to the paddle of the device, while VSSS, VSS1, VSS2, VSS3 are digital ground pins. All grounds should be connected to a ground plane.

2.2.2 Reset

RESETN is a bi-directional active low reset pin that is connected to a 40kΩ internal pull-up resistor. It may be pulled low by an external circuit, or can be driven low by the JN5139 if an internal reset is generated. Typically, it will be used to provide a system reset signal. Refer to section 6.2, External Reset, for more details.

2.2.3 16MHz System Clock

A crystal connected between XTALIN and XTALOUT drives the system clock. A capacitor to analogue ground is required on each of these pins. Refer to section 5.1 16MHz System Clock / Crystal Oscillator for more details.

2.2.4 Radio

A 200Ω balanced antenna (such as a printed circuit antenna) can be connected directly to the radio interface pins RFM and RFP.

A single-ended 50Ω antenna such as a ceramic type or SMA connector for an external antenna requires the addition of a 200/50Ω 2.45GHz balun transformer connected to the antenna pins. The balun differential port should be connected to the antenna port with 200Ω balanced controlled impedance track. A 50Ω controlled impedance track should be used to connect the unbalanced port of the balun to the antenna to ensure good impedance matching and reduce losses and reflections.

A simple external loop filter circuit consisting of two capacitors and a resistor is connected to VCOTUNE. Refer to section 8.1 Radio for more details.

An external resistor (43kΩ) is required between IBIAS and analogue ground to set various bias currents and references within the radio.

2.2.5 Analogue Peripherals

Several of the analogue peripherals require a reference voltage to use as part of their operations. They can use either an internal reference voltage or an external reference connected to VREF. This voltage is referenced to analogue ground and the performance of the analogue peripherals is dependant on the quality of this reference.

There are four ADC inputs, two pairs of comparator inputs and two DAC outputs. The analogue I/O pins on the JN5139 can have signals applied up to 0.3v higher than VDD1. A schematic view of the analogue I/O cell is shown in Figure 3: Analogue I/O Cell

In reset and deep sleep, the analogue peripherals are all off and the DAC outputs are in a high impedance state.

In sleep, the ADC and DACs are off, with the DAC outputs in high impedance state. The comparators may optionally be used as a wakeup source.

Unused ADC and comparator inputs should be left unconnected.

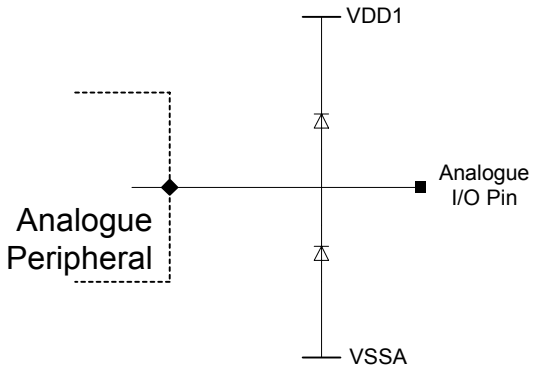


Figure 3: Analogue I/O Cell

2.2.6 Digital Input/Output

Digital I/O pins on the JN5139 can have signals applied up to 2V higher than VDD2 (with the exception of pins DIO9 and DIO10 that are 3V tolerant) and are therefore TTL-compatible with VDD2 > 3V. For other DC properties of these pins see section 17.2.3 I/O Characteristics.

When used in their primary function all Digital Input/Output pins are bi-directional and are connected to weak internal pull up resistors (40kΩ nominal) that can be disabled. When used in their secondary function (selected when the appropriate peripheral block is enabled through software library calls) then their direction is fixed by the function. The pull up resistor is enabled or disabled independently of the function and direction; the default state from reset is enabled.

A schematic view of the digital I/O cell is in Figure 4: DIO Pin Equivalent Schematic.

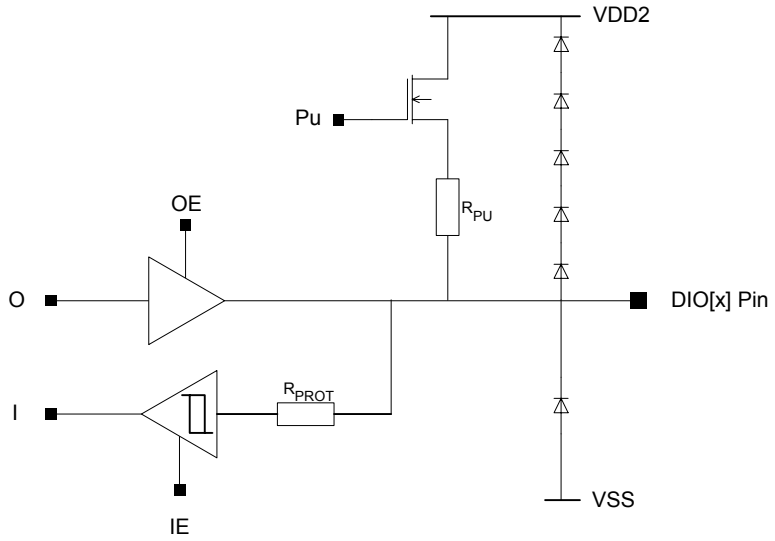


Figure 4: DIO Pin Equivalent Schematic

In reset, the digital peripherals are all off and the DIO pins are set as high-impedance inputs. During sleep and deep sleep, the DIO pins retain both their input/output state and output level that was set as sleep commences. If the DIO pins were enabled as inputs and the interrupts were enabled then these pins may be used to wake up the JN5139 from sleep.

3 CPU

The CPU of the JN5139 is a 32-bit load and store RISC processor. It has been architected for three key requirements:

- Low power consumption for battery powered applications
- High performance to implement a wireless protocol at the same time as complex applications
- Efficient coding of high-level languages such as C provided with the Jennic Software Developers Kit

It features a linear 32-bit logical address space with unified memory architecture, accessing both code and data in the same address space. Registers for peripheral units, such as the timers, UARTs and the baseband processor are also mapped into this space.

The CPU contains a block of 32 32-bit General-Purpose (GP) registers together with a small number of special purpose registers which are used to store processor state and control interrupt handling. The contents of any GP register can be loaded from or stored to memory, while arithmetic and logical operations, shift and rotate operations, and signed and unsigned comparisons can be performed either between two registers and stored in a third, or between registers and a constant carried in the instruction. Operations between general or special-purpose registers execute in one cycle (16MHz) while those that access memory require a further cycle to allow the memory to respond.

The instruction set manipulates 8, 16 and 32-bit data, stored in big-endian format; this means that programs can use objects of these sizes very efficiently. Manipulation of 32-bit quantities is particularly useful for protocols and high-end applications allowing algorithms to be implemented in fewer instructions than on smaller word-size processors, and to execute in fewer clock cycles.

The instruction set is designed for the efficient implementation of high-level languages such as C. Access to fields in complex data structures is very efficient due to the provision of several addressing modes, together with the ability to be able to use any of the GP registers to contain the address of objects. Subroutine parameter passing is also made more efficient by using GP registers rather than pushing objects on the stack. The recommended programming method for the JN5139 is by using C, which is supported by a software developer kit comprising a C compiler, linker and debugger.

The CPU architecture also contains features that make the processor suitable for embedded, real-time applications. In some applications, it may be necessary to use a real-time operating system to allow multiple tasks to run on the processor.

Embedded applications require efficient handling of external hardware events. Exception processing (including reset and interrupt handling) is enhanced by the inclusion of a number of special-purpose registers into which the PC and status register contents are copied as part of the operation of the exception hardware. This means that the essential registers for exception handling are stored in one cycle, rather than the slower method of pushing them onto the processor stack. The PC is also loaded with the vector address for the exception that occurred, allowing the handler to start executing in the next cycle.

To improve power consumption a number of power-saving modes are implemented in the JN5139, described more fully in section 16 - Power Management and Sleep Modes. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on an interrupt will wake up to service the request.

4 Memory Organisation

This section describes the different memories found within the JN5139. The device contains ROM, RAM, OTP eFuse memory, the wireless transceiver and peripherals all within the same linear address space.

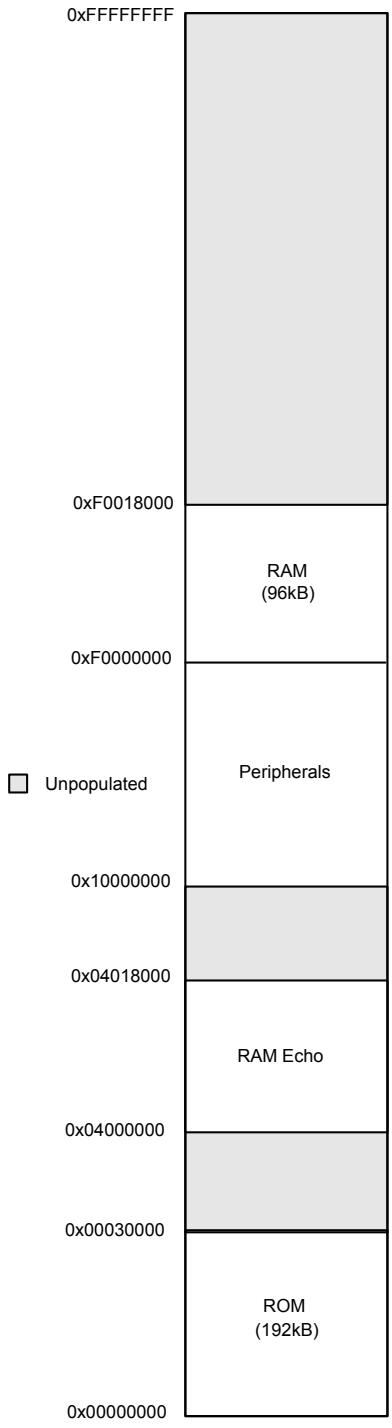


Figure 5: JN5139 Memory Map

4.1 ROM

The ROM is 192K bytes in size, organized as 48k x 32-bit words and can be accessed by the CPU in a single clock cycle. The ROM contents include bootloader to allow external Flash memory contents to be bootloaded into RAM at runtime, a default interrupt vector table, an interrupt manager, IEEE802.15.4 MAC and assorted APIs for interfacing to the MAC and on-chip hardware peripherals. The operation of the boot loader is described in detail in Application Note JN-AN-1003 Boot Loader Operation [2]. The interrupt manager routes interrupt calls to the application's soft interrupt vector table contained within RAM. Section 7 contains further information regarding the handling of interrupts. Typical ROM contents are shown in Figure 6.

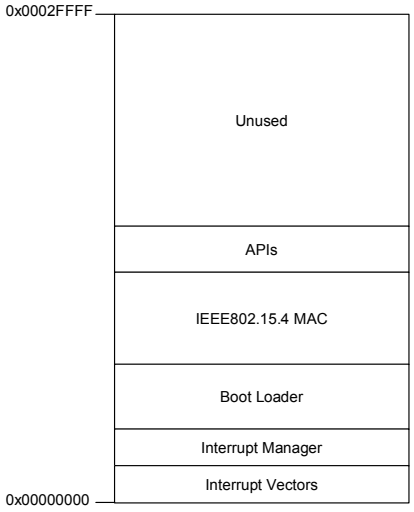


Figure 6: ROM contents

4.2 RAM

The JN5139 contains 96k bytes of high speed RAM organized as 24k x 32-bit. It can be used for both code and data storage and is accessed by the CPU in a single clock cycle. At reset, a boot loader controls the loading of segments of code and data from an external memory connected to the SPI port, into RAM. Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are un-powered. Typical RAM contents are shown in Figure 7.

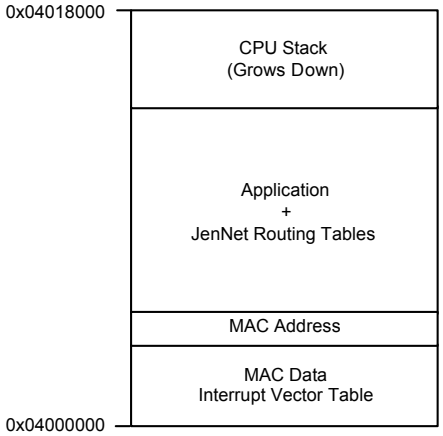


Figure 7: Typical RAM Contents

4.3 OTP eFuse Memory

The JN5139 contains 48-bytes of eFuse memory; this is one time programmable memory that is organised as 12 x 32-bit words, 4 words are reserved by Jennic and 4 words are reserved for future use. The remaining 4 words are fully user programmable, designed to allow for the storage of a 128-bit encryption key for secure external memory encryption (see section 4.4.1)

For full details on how to program and use the eFuse memory, please refer to application note JN-AN-1062 Using OTP eFuse Memory [3].

Alternatively, Jennic can provide an eFuse programming service for customers that wish to use the eFuse but do not wish to undertake this for themselves. For further details of this service, please contact your local Jennic sales office.

4.4 External Memory

An external memory with an SPI interface may be used to provide storage for program code and data for the device when external power is removed. The memory is connected to the SPI interface using select line SPISEL0; this select line is dedicated to the external memory interface and is not available for use with other external devices. See Figure 8 for connection details.

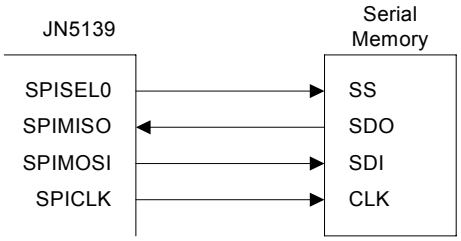


Figure 8: Connecting External Serial Memory

At reset, the contents of this memory are copied into RAM by the software boot loader. The Flash memory devices that are supported as standard through the JN5139 bootloader are given in Table 1. Jennic recommends that where possible one of these devices should be selected.

Manufacturer	Device Number
SST (Silicon Storage Technology)	25VF010A (1Mbyte device)
Numonyx	M25P10-A (1Mbyte device), M25P40 (4Mbyte device)

Table 1: Supported Flash Memories

Applications wishing to use an alternate Flash memory device should refer to application note JN-AN-1038 Programming Flash devices not supported by the JN51xx ROM-based bootloader [4]. This application note provides guidance on developing an interface to an alternate device.

4.4.1 External Memory Encryption

The contents of the external serial memory can be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in eFuse.

When bootloading program code from external serial memory, the JN5139 automatically accesses the encryption key to execute the decryption process. User program code does not need to handle any of the decryption process; it is a transparent process.

With encryption enabled, the time taken to boot code from external Flash memory is increased.

4.5 Peripherals

All peripherals have their registers mapped into the memory space. Access to these registers requires 3 clock cycles. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see the Integrated Peripherals API Reference Manual (JN-RM-2001).

4.6 Unused Memory Addresses

Any attempt to access an unpopulated memory area will result in a bus error exception (interrupt) being generated.

5 System Clocks

Two system clocks are used to provide timing references into the on-chip subsystems of the JN5139. A 16MHz clock, generated by a crystal-controlled 16MHz oscillator, is used by the transceiver, processor, memory and digital and analogue peripherals. A 32kHz clock is used by the sleep timer and during the startup phase of the chip.

5.1 16MHz System Clock / Crystal Oscillator

The JN5139 contains the necessary on-chip components to build a 16 MHz reference oscillator with the addition of an external crystal resonator, two tuning capacitors and a resistor. The schematic of these components are shown in Figure 9. The two capacitors, C1 and C2, will typically be 15pF ±5% and use a COG dielectric, R2 should be 1M5Ω. Due to the small size of the capacitors, it is important to keep the traces to the external components as short as possible. The on-chip transconductance amplifier is compensated for temperature variation, and is self-biasing by means of the internal resistor R1. The electrical specification of the oscillator can be found in section 17.3.7. For detailed application support and specification of the crystal required and factors affecting C1 and C2 see Appendix B.1.

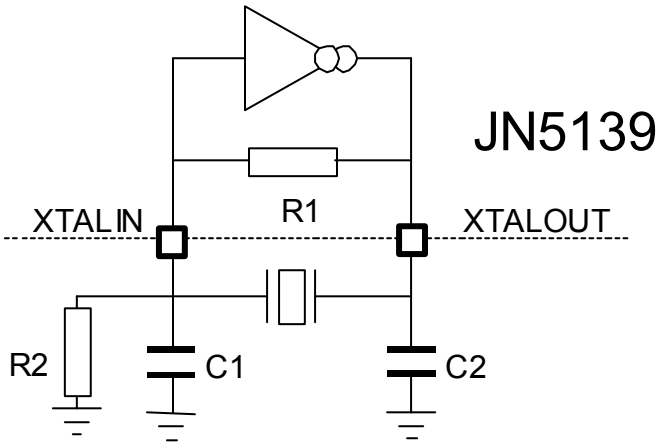


Figure 9: Crystal oscillator connections

The clock generated by this oscillator provides the reference for most of the JN5139 subsystems, including the transceiver, processor, memory and digital and analogue peripherals.

5.2 32kHz System Clock

The 32kHz system clock is used for timing the length of a sleep period (see section 16 Power Management and Sleep Modes) and also to generate the system clock used internally during reset. The clock can be selected from one of two sources through the application software:

- 32kHz RC Oscillator
- 32kHz External Clock

Once a clock source has been selected, then it will remain in use for all 32kHz timing until a chip reset is performed. Upon a chip reset the JN5139 defaults to using the internal 32kHz RC Oscillator.

5.2.1 32kHz RC Oscillator

The internal 32kHz RC oscillator is the default clock and requires no external components. It provides a low speed clock for use in sleep mode. The internal timing components of the oscillator have a wide tolerance due to manufacturing process variation and so the oscillator runs nominally at 32kHz ±30%. To make this useful as a timing source for accurate wakeup from sleep, a frequency calibration factor derived from the more accurate 16MHz clock may be applied. The calibration factor is derived through software, details can be found in section 12.3.1. For detailed electrical specifications, see section 17.3.6.

5.2.2 32kHz External Clock

An externally supplied 32kHz reference clock on the CLK32K input (DIO9) may be provided to the JN5139. This would allow the 32kHz system clock to be sourced from a very stable external oscillator module, allowing more accurate sleep cycle timings. (See section 17.2.3 I/O Characteristics, DIO9 is a 3V tolerant input)

6 Reset

A system reset initialises the device to a predefined state and forces the CPU to start program execution from the reset vector. The reset process that the JN5139 goes through is as follows.

When power is applied, the internal 32kHz oscillator starts up and stabilises, which takes approximately 100μsec. At this point, the 16MHz crystal oscillator is enabled and power is applied to the processor and digital logic. The logic blocks are held in reset until the 16MHz crystal oscillator stabilises, which typically takes 2.75ms.

Once the oscillator is up and running the internal reset is removed from the CPU and peripheral logic and the CPU starts to run code beginning at the reset vector, consisting of initialisation code and the resident Boot Loader (described in JN-AN-1003 Boot Loader Operation [2]).

Section 17.3.1 provides detailed electrical data and timing.

The JN5139 has three sources of reset:

- Internal Power-on Reset
- External Reset
- Software Reset

Note: When the device exits a reset condition, device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, then the device must be held in reset until the operating conditions are met. (See section 17.3.1)

When reset is low, the digital logic and RAM are not powered and therefore anything stored in the RAM after reset is released cannot be guaranteed to still be valid.

6.1 Internal Power-on Reset

For the majority of applications the internal power-on reset is capable of generating the required reset signal. When power is applied to the device, the power-on reset circuit monitors the rise of the VDD supply. When VDD reaches the specified threshold, the reset signal is generated and can be observed as a rising edge on the RESETN pin. This signal is held internally until the power supply and oscillator stabilisation time has elapsed, at which point the internal reset signal is then removed and the CPU is allowed to run.

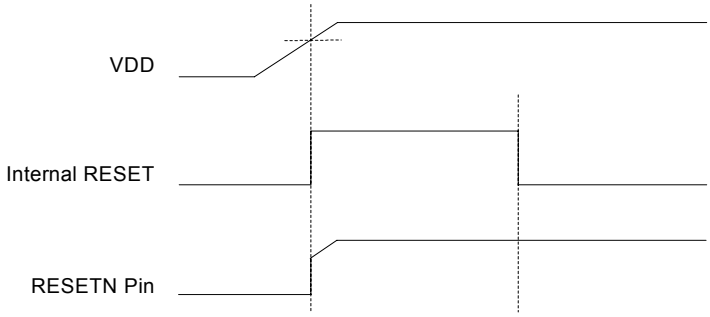


Figure 10: Internal Power-on Reset

The external resistor and capacitor provides a simple reset operation when connected to the RESETN pin, as shown in Figure 11. This can be used to extend the reset length and help in systems with noisy reset push-buttons.

If the application requires a power supply reset to be used, i.e. removing and then applying VDD, it is important that the device decoupling capacitors are completely discharged (less than 0.4v) before the VDD is re-applied. Failure to do so may inhibit device operation. If complete discharge is difficult to achieve then it is recommended to use of an external reset device to hold the device in reset whilst the voltage has dropped below the device operating voltage range.

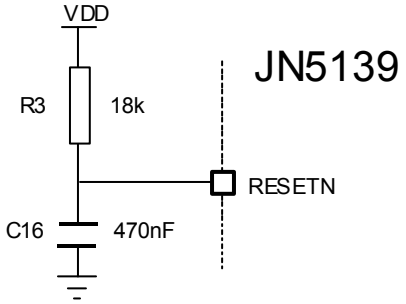


Figure 11: External Reset Generation

6.2 External Reset

An external reset is generated by a low level on the RESETN pin. Reset pulses longer than the minimum pulse width will generate a reset during active or sleep modes. Shorter pulses are not guaranteed to generate a reset. The JN5139 is held in reset while the RESETN pin is low and when the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the internal reset process starts.

Multiple devices may connect to the RESETN pin in an open-collector mode. The JN5139 has an internal pull-up resistor although an external pull-up resistor is recommended when multiple devices connect to the RESETN pin. The pin is an input for an external reset and an output, driven low, during the power-on reset and software reset. No devices should drive the RESETN pin high.

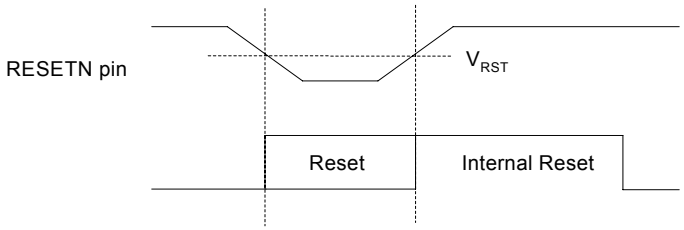


Figure 12: External Reset

6.3 Software Reset

A system reset can be triggered at any time through software control, causing a full chip reset and invalidating the RAM contents. For example this can be executed within a user's application upon detection of a system failure. When performing the reset, the RESETN pin is driven low for 1µsec; depending on the external components this may or may not be visible on the pin.

In addition, the RESETN line can be driven low by the JN5139 to provide a reset to other devices in the system (e.g. external sensors) without resetting itself. When the RESETN line is not driven it will pull back high through either the internal pull-up resistor or any external circuitry. It is essential to ensure that the RESETN line pulls back high within 100µsec after the JN5139 stops driving the line; otherwise a system reset will occur. Due to this, careful consideration should be taken of any capacitance on this line. For instance, the RC values recommended in section 6.1 may need to be replaced with a suitable reset IC.

7 Interrupt System

The interrupt system on the JN5139 is a hardware-vectored interrupt system. The JN5139 provides several interrupt sources, some associated with CPU operations (CPU exceptions) and others which are used by hardware in the device. When an interrupt occurs the CPU stops executing the current program and loads its program counter with a fixed hardware address specific to that interrupt. The interrupt handler or interrupt service routine is stored at this location and is run on the next CPU cycle. Execution of interrupt service routines is always performed in supervisor mode. Interrupt sources and their vector locations are listed in Table 2 below:

Interrupt Source	Vector Location	Interrupt Definition
Reset	0x100	Software or hardware reset
Bus Error	0x200	Bus error or attempt to access invalid physical address
Tick Timer	0x500	Tick Timer expiry
Alignment	0x600	Load/Store to naturally not aligned location
Illegal Instruction	0x700	Illegal instruction in instruction stream
Hardware Interrupts	0x800	Hardware Interrupt
System Call	0xC00	System Call Initiated by software (l.sys instruction)
Trap	0xE00	Caused by l.trap instruction

Table 2: Interrupt Vectors

7.1 System Calls

Executing the `l.sys` instruction causes a system call interrupt to be generated. The purpose of this interrupt is to allow a task to switch into supervisor mode when a real time operating system is in use, see section 3 for further details. It also allows a software interrupt to be issued, as does execution of the `l.trap` instruction.

7.2 Processor Exceptions

7.2.1 Bus Error

A bus error exception is generated when software attempts to access a memory address that does not exist, or is not populated with memory or peripheral registers.

7.2.2 Alignment

Alignment exceptions are generated when software attempts to access objects that are not aligned to natural word boundaries. 16-bit objects must be stored on even byte boundaries, while 32-bit objects must be stored on quad byte boundaries. For instance, attempting to read a 16-bit object from address 0xFFF1 will trigger an alignment exception as will a read of a 32-bit object from 0xFFF1, 0xFFF2 or 0xFFF3. Examples of legal 32-bit object addresses are 0xFFF0, 0xFFF4, 0xFFF8 etc.

7.2.3 Illegal Instruction

If the CPU reads an unrecognised instruction from memory as part of its instruction fetch, it will cause an illegal instruction exception.

7.3 Hardware Interrupts

Hardware interrupts generated from the transceiver, analogue or digital peripherals and DIO pins are individually masked using the Programmable Interrupt Controller (PIC). Management of interrupts is provided in the peripherals library. Further details of interrupts are provided for the functions in their respective sections in this datasheet.

Interrupts are used to wake the JN5139 from sleep. The peripherals, baseband controller, security coprocessor and PIC are powered down during sleep but the DIO interrupts and optionally the wake-up timers and analogue comparator interrupts remain powered to bring the JN5139 out of sleep.

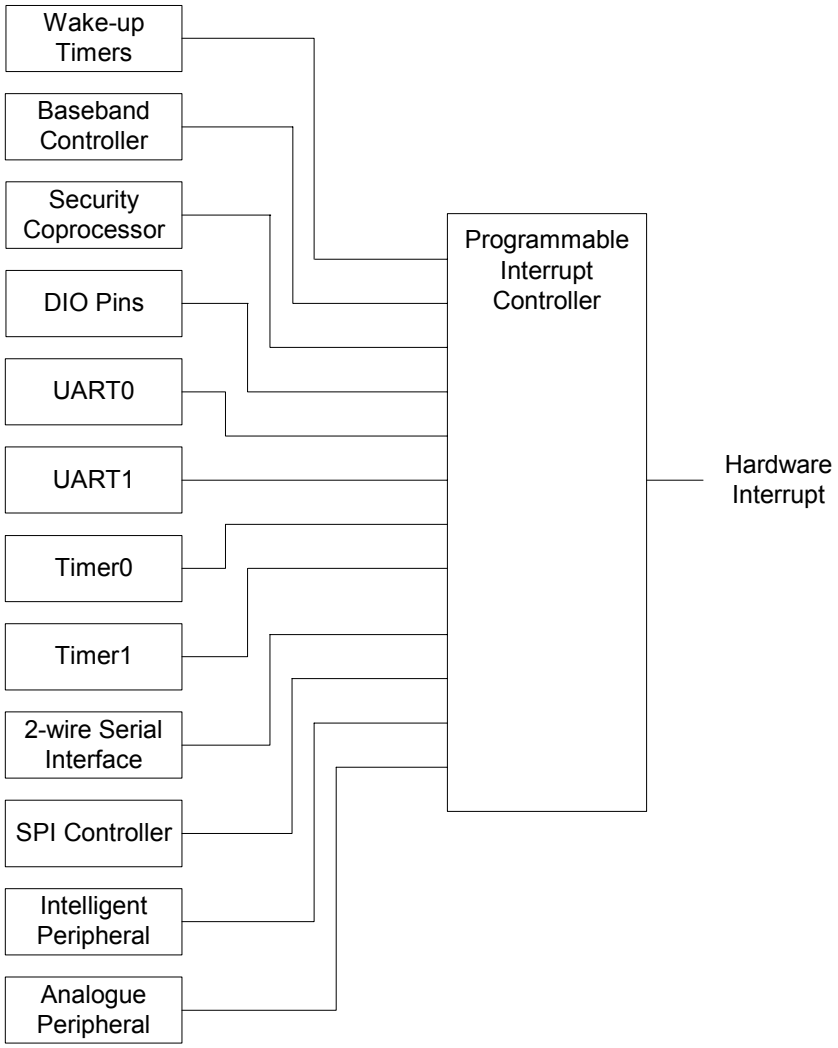


Figure 13: Programmable Interrupt Controller

8 Wireless Transceiver

The wireless transceiver comprises a 2.45GHz radio, an O-QPSK modem, a baseband processor, a security coprocessor and PHY controller. These blocks, with protocol software provided as a library, implement an IEEE802.15.4 standards-based wireless transceiver that transmits and receives data over the air in the unlicensed 2.4GHz band.

8.1 Radio

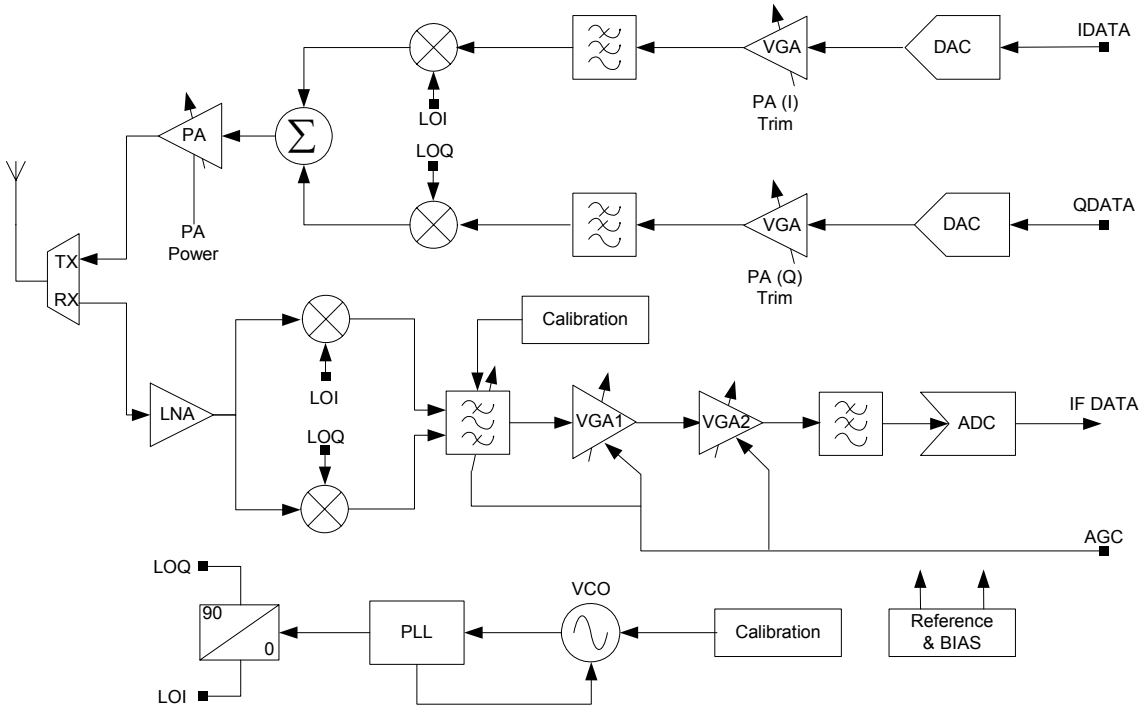


Figure 14: Radio Architecture

The radio comprises a low-IF receive path and a direct up-conversion transmit path, which converge at the TX/RX switch. This switch includes the necessary matching components such that a 200Ω differential antenna may be directly connected without external components. Alternatively, a balun can be used for single ended antennas.

The 16MHz crystal oscillator feeds a divider, which provides the frequency synthesiser with a reference frequency. The synthesiser contains programmable feedback dividers, phase detector, charge pump and internal Voltage Controlled Oscillator (VCO). The VCO has no external components, and includes calibration circuitry to compensate for differences in internal component values due to process and temperature variations. The VCO is controlled by a Phase Locked Loop (PLL) that has a loop filter comprising 3 external components. A programmable charge pump is also used to tune the loop characteristic. Finally, quadrature (I and Q) local oscillator signals for the mixer drives are derived.

The receiver chain starts with the low noise amplifier / mixer combination whose outputs are passed to the polyphase bandpass filter. This filter provides the channel definition as well as image frequency rejection. The signal is then passed to two variable gain amplifier blocks. The gain control for these stages and the bandpass filter is derived in the automatic gain control (AGC) block within the Modem. The signal is conditioned with the anti-alias low pass filter before being converted to a digital signal with a flash ADC.

In the transmit direction, the digital I and Q streams from the Modem are passed to I and Q quadrature DAC blocks which are buffered and low-pass filtered, before being applied to the modulator mixers. The summed 2.4 GHz signal is then passed to the RF Power Amplifier (PA), whose power control can be selected from one of six settings. The output of the PA drives the antenna via the RX/TX switch.

8.1.1 Radio External components

The VCO loop filter requires three external components and the IBIAS pin requires one external component as shown in Figure 15. These components should be placed close to the JN5139 pins and analogue ground.

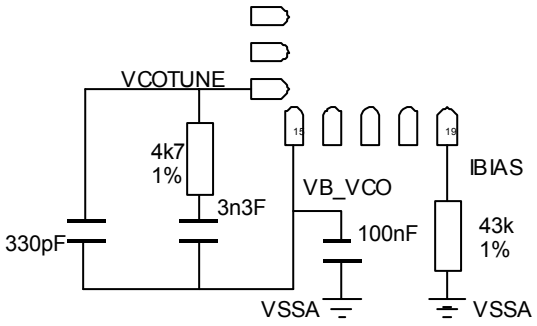


Figure 15: VCO Loop Filter and IBIAS

The radio is powered from a number of internal 1.8V regulators fed from the analogue supply VDD1, in order to provide good noise isolation between the digital logic of the JN5139 and the analogue blocks. These regulators are also controlled by the baseband controller and protocol software to minimise power consumption. Decoupling for internal regulators is required as described in section 2.2.1, Power Supplies.

In addition, as described in section 8.1, for single ended antennas or connectors a balun will be required.

8.1.2 Antenna Diversity

Support is provided for antenna diversity. Antenna diversity is a technique that maximises the performance of an antenna system. It allows the radio to switch between two antennas that have very low correlation between their received signals. Typically, this is achieved by spacing two antennas around 0.25 wavelengths apart or by using two orthogonal polarisations. So, if a packet is transmitted and no acknowledgement is received, the radio system can switch to the other antenna for the retry, with a different probability of success.

The JN5139 provides an output on DIO12 that is asserted on odd numbered retries that can be used to control an antenna switch; this enables antenna diversity to be implemented easily (see Figure 16 and Figure 17)

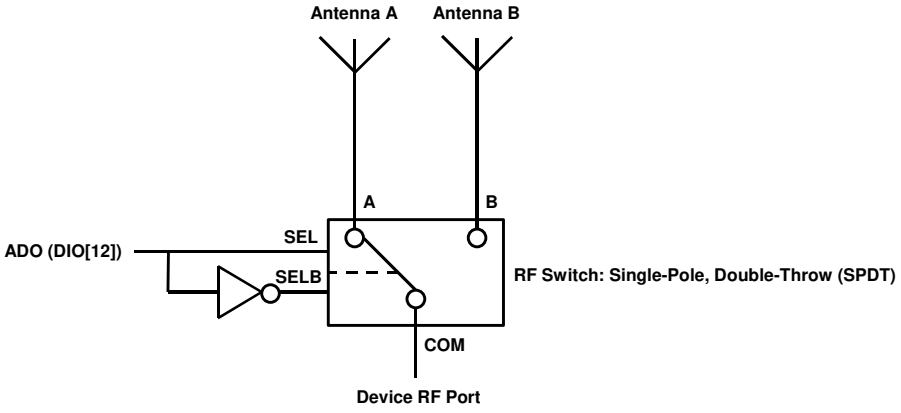


Figure 16 Simple Antenna Diversity Implementation using External RF Switch

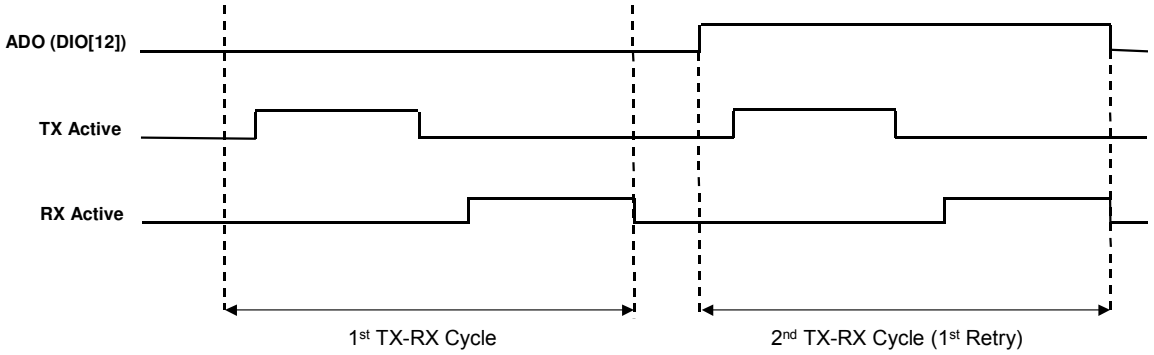


Figure 17 Antenna Diversity ADO Signal for TX with Acknowledgement

8.2 Modem

The Modem performs all the necessary modulation and spreading functions required for digital transmission and reception of data at 250kbps in the 2450MHz radio frequency band in compliance with the IEEE802.15.4 standard.

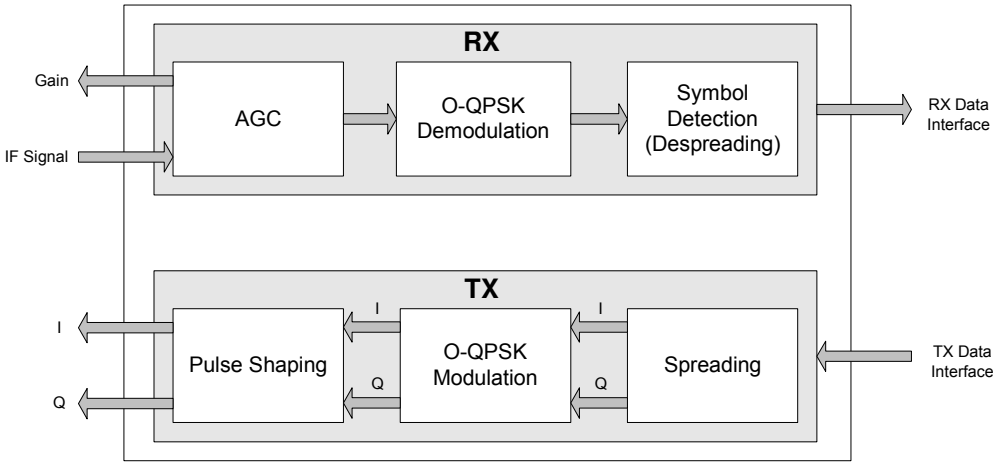


Figure 18: Modem Architecture

The transmitter receives symbols from the baseband processor and uses the spreading function to map each unique 4-bit symbol to a 32-chip Pseudo-random Noise (PN) sequence. Offset-QPSK modulation and half-sine pulse shaping is applied to the resultant spreading sequence to produce two independent quadrature phase signals (I and Q), which are subsequently converted to analogue voltages in the radio transmit path.

The Automatic Gain Control (AGC) monitors the received signal level and adjusts the gain of the amplifiers in the radio receiver to ensure that the optimum signal amplitude is maintained during reception.

The demodulator performs digital IF down-conversion and matched filtering and is extremely tolerant to carrier frequency offsets in excess of ±80ppm without suffering any significant degradation in performance.