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JN5169

IEEE802.15.4 Wireless Microcontroller

Rev. 1.3 — 22 September 2017 Product data sheet

1. General description

The JN5169 is an ultra low power, high performance wireless microcontroller suitable for ZigBee applications. It features 512 kB embedded Flash, 32 kB RAM and 4 kB EEPROM memory, allowing OTA upgrade capability without external memory. The 32-bit RISC processor offers high coding efficiency through variable width instructions, a multi-stage instruction pipeline and low-power operation with programmable clock speeds. It also includes a 2.4 GHz IEEE802.15.4 compliant transceiver and a comprehensive mix of analog and digital peripherals. The best in class RX operating current (down to 13 mA and with a 0.7 μA sleep timer mode) gives excellent battery life allowing operation direct from a coin cell. Radio transmit power is configurable up to +10 dBm output.

The peripherals support a wide range of applications. They include a 2-wire compatible I^2C-bus and SPI-bus which can operate as either master or slave, a 6-channel ADC with a battery monitor and a temperature sensor. It can support a large switch matrix of up to 100 elements, or alternatively a 40-key capacitive touch pad.

2. Features and benefits

2.1 Benefits

- Single chip device to run stack and application
- Very low current solution for long battery life; over 10 years
- Very low RX current for low standby power of mains powered nodes
- Integrated power amplifier for long range and robust communication
- High tolerance to interference from other 2.4 GHz radio sources
- Supports multiple network stacks
- Highly featured 32-bit RISC CPU for high performance and low power
- Large embedded Flash memory to enable over-the-air firmware updates without external Flash memory
- System BOM is low in component count and cost
- Flexible sensor interfacing options
- Very thin quad flat 6 × 6 mm, 40 terminal package; lead-free and RoHS compliant
- Temperature range: −40 °C to +125 °C

2.2 Features: radio

- 2.4 GHz IEEE802.15.4 compliant
- RX current 14.7 mA, in low power receive mode 13 mA
- Receiver sensitivity −96 dBm
- Configurable transmit power, for example:

  - 10 dBm, 23.3 mA
  - 8.5 dBm, 19.6 mA
  - 3 dBm, 14 mA
- Radio link budget 106 dB
- Maximum input level of +10 dBm
- Compensation for temperature drift of crystal oscillator frequency
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- Integrated ultra low-power RC sleep oscillator (0.7 μA)
- 2.0 V to 3.6 V battery operation
- Deep sleep current 50 nA (wake-up from IO)
- < 0.15 $ external component cost
- Antenna diversity (Auto RX)

2.3 Features: microcontroller

- 32-bit RISC CPU; 1 MHz to 32 MHz clock speed
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- 512 kB Flash
- 32 kB RAM
- 4 kB EEPROM
- Data EEPROM with guaranteed 100 k write operations
- ZigBee PRO stack with Home Automation, Light Link and Smart Energy profiles
- 2-wire I^2C-bus compatible serial interface; can operate as either master or slave
- 5 × PWM (4 timers, 1 timer/counter)
- 2 low-power sleep counters
- 2 UARTs
- SPI-bus master and slave port, 3 selects
- Supply voltage monitor with 8 programmable thresholds
- 6-input 10-bit ADC, comparator
- Battery and temperature sensors
- Watchdog and Supply Voltage Monitor (SVM)
- Up to 20 Digital IO (DIO) pins

3. Applications

- Robust and secure low-power wireless applications
- ZigBee 3.0
- Internet of Things (IoT)
- ZigBee Smart Energy networks
- ZigBee Light Link networks
- ZigBee Home Automation networks
- Toys and gaming peripherals
- Energy harvesting - for example, self-powered light switch

4. Overview

The JN5169 wireless microcontroller that provides a fully integrated solution for applications that use the IEEE802.15.4 standard in the 2.4 GHz to 2.5 GHz ISM frequency band, including ZigBee PRO applications based on the Smart Energy, Light Link and Home Automation profiles.

The JN5169 features 512 kB embedded Flash, 32 kB RAM and 4 kB EEPROM memory and radio outputs up to 10 dBm.

Applications that transfer data wirelessly tend to be more complex than applications for wired solutions. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimize this complexity, NXP provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN5169. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, we do not provide the JN5169 register details in this data sheet.

The device includes a wireless transceiver, RISC CPU, on-chip memory and an extensive range of peripherals.

4.1 Wireless transceiver

The wireless transceiver comprises a 2.45 GHz radio, a modem, a baseband controller and a security coprocessor. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realized very easily. Section 15.1 describes a complete reference design including Printed-Circuit Board (PCB) design and Bill Of Materials (BOM).

The security coprocessor provides hardware-based 128-bit AES-CCM modes as specified by the IEEE802.15.4 2006 standard. Specifically this includes encryption and authentication covered by the MIC-32/-64/-128, ENC and ENC-MIC-32/-64/-128 modes of operation.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 (2006) MAC and PHY functionality under the control of a protocol stack. Applications incorporating IEEE802.15.4 functionality can be developed rapidly by combining user-developed application software with a protocol stack library.

4.2 RISC CPU and memory

A 32-bit RISC CPU allows software to be run on-chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN5169 has a unified memory architecture. Code memory, data memory, peripheral devices and I/O ports are organized within the same linear address space. The device contains up to 512 kB of Flash, 32 kB of RAM and 4 kB EEPROM.

4.3 Peripherals

The following peripherals are available on chip:

- Master SPI-bus port with 3 select outputs
- Slave SPI-bus port
- 2 UARTs: one capable of hardware flow control (4-wire, includes RTS/CTS); the other just 2-wire (RX/TX)
- 1 programmable timer/counter which supports Pulse Width Modulation (PWM) and capture/compare, plus 4 PWM timers which support PWM and Timer modes only
- 2 programmable sleep timers and 1 tick timer
- 2-wire serial interface (compatible with SMbus and I^2C-bus) supporting master and slave operation
- 20 digital I/O lines (multiplexed with peripherals such as timers, SPI-bus and UARTs)
- 2 digital outputs (multiplexed with SPI-bus port)
- 10-bit, Analog-to-Digital Converter (ADC) with up to 6 input channels
- Programmable analog comparator
- Internal temperature sensor and battery monitor
- 2 low-power pulse counters
- Random number generator
- Watchdog timer and Supply Voltage Monitor
- JTAG hardware debug port
- Transmit and receive antenna diversity with automatic receive switching based on received energy detection

User applications access the peripherals using the JN516x Integrated Peripherals API (Application Programming Interface). This allows applications to use a tested and easily understood view of the peripherals facilitating rapid system development.

5. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
JN5169	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-8

For further details, refer to the Wireless Connectivity area of the NXP web site Ref. 1.

6. Block diagram

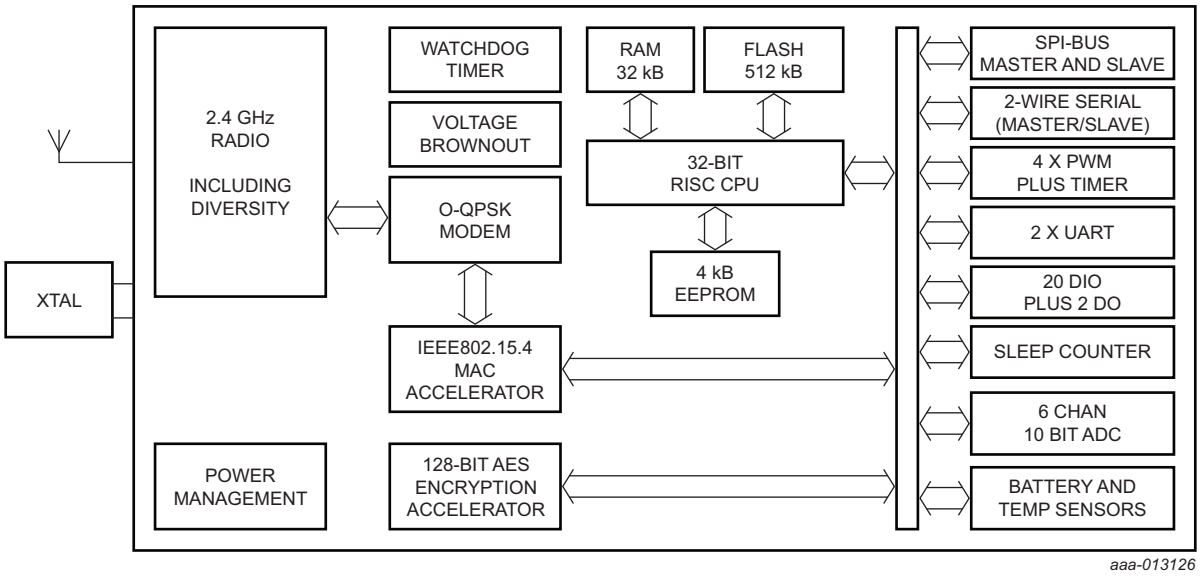
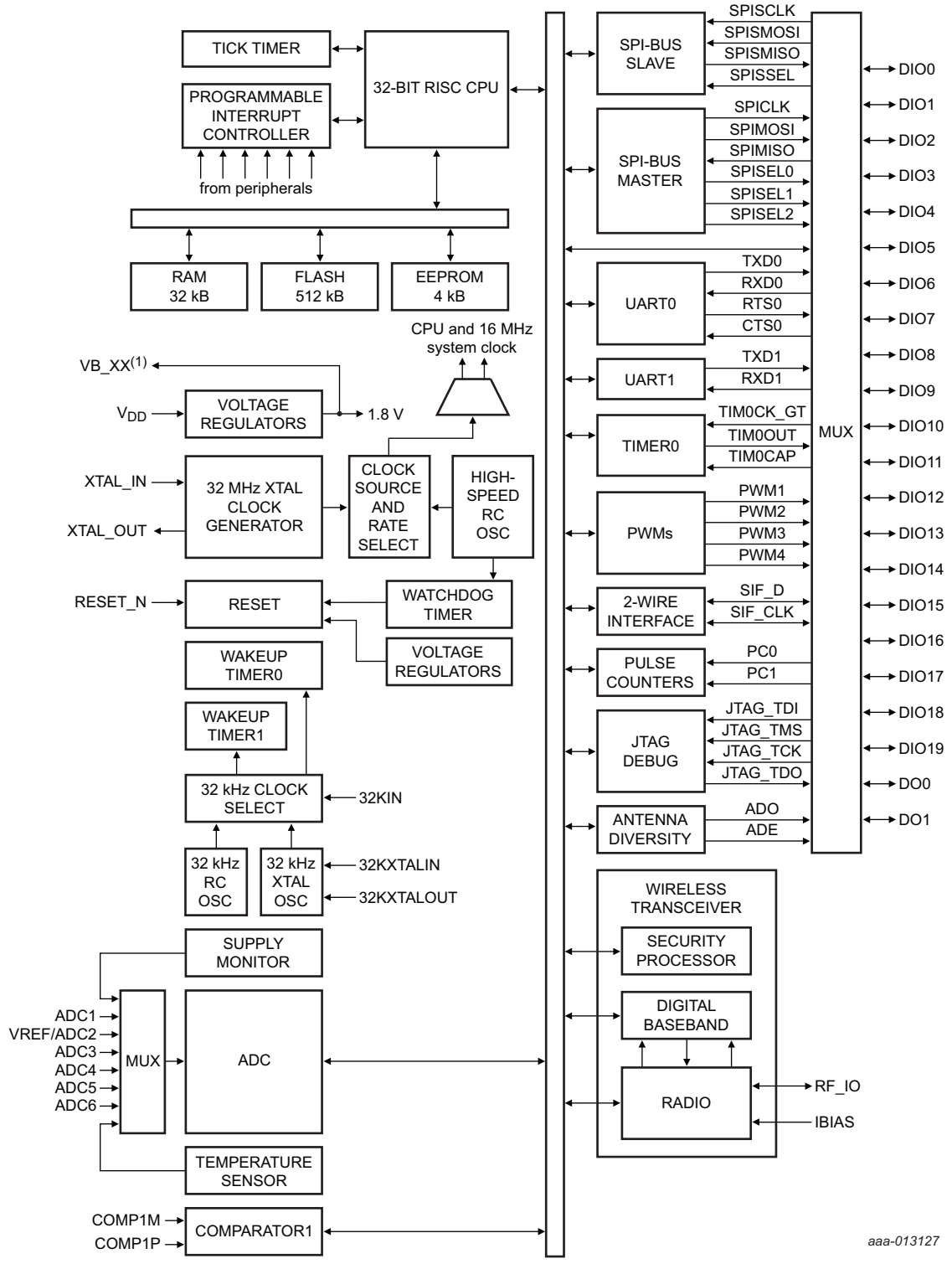


Fig 1. Block diagram

7. Functional diagram

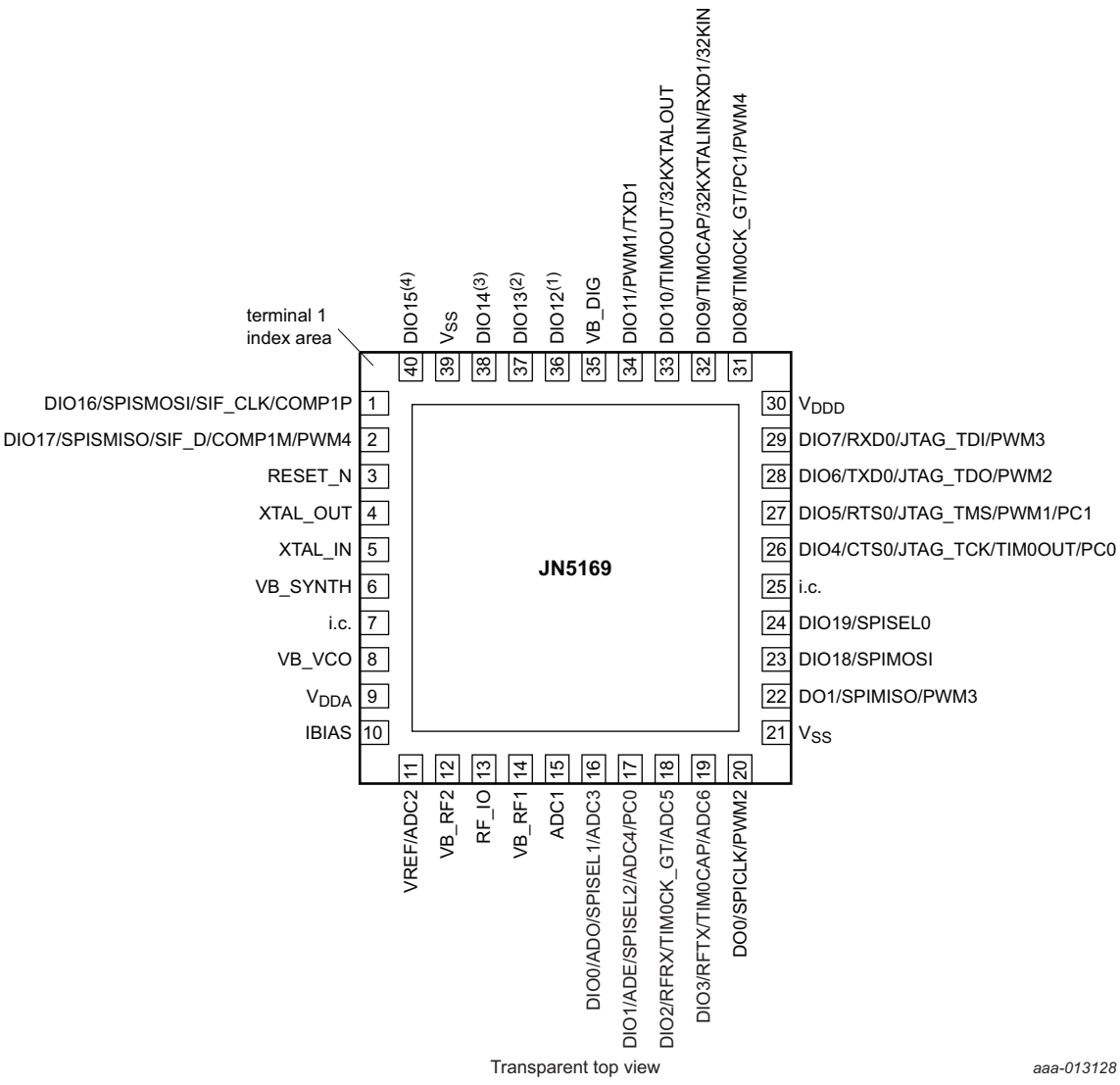


(1) With XX = SYNTH or VCO or RF2 or RF1 or DIG.

Fig 2. Functional block diagram

8. Pinning information

8.1 Pinning



Refer to Section 15 for important applications information regarding the connection of the paddle to the PCB.

(1) Multi-function: DIO12/PWM2/CTS0/JTAG_TCK/ADO/SPISMOSI.

(2) Multi-function: DIO13/PWM3/RTS0/JTAG_TMS/ADE/SPISMISO.

(3) Multi-function: DIO14/SIF_CLK/TXD0/TXD1/JTAG_TDO/SPISEL1/SPISSEL.

(4) Multi-function: DIO15/SIF_D/RXD0/RXD1/JTAG_TDI/SPISEL2/SPISCLK.

Fig 3. Pin configuration

8.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
DIO16/SPISMOSI/SIF_CLK/COMP1P	1	I/O	**DIO16 —** DIO16
			COMP1P — comparator plus input
			SIF_CLK — Serial Interface clock
			SPISMOSI — SPI-bus slave Master Out Slave In input
DIO17/SPISMISO/SIF_D/COMP1M/PWM4	2	I/O	**DIO17 —** DIO17
			COMP1M — comparator minus input
			SIF_D — Serial Interface Data
			SPISMISO — SPI-bus slave Master In Slave Out output
			PWM4 — PWM 4 output
RESET_N	3	I	**RESET_N —** reset input
XTAL_OUT	4	O	**XTAL_OUT —** system crystal oscillator
XTAL_IN	5	I	**XTAL_IN —** system crystal oscillator
VB_SYNTH	6	P	**VB_SYNTH —** regulated supply voltage
i.c.	7	-	internally connected; leave open
VB_VCO	8	P	**VB_VCO —** regulated supply voltage
V_{DDA}	9	P	**V_{DDA} —** analog supply voltage
IBIAS	10	I	**IBIAS —** bias current control
VREF/ADC2	11	P	**VREF —** analog peripheral reference voltage
		I	**ADC2 —** ADC input 2
VB_RF2	12	P	**VB_RF2 —** regulated supply voltage
RF_IO	13	I/O	**RF_IO —** RF antenna
VB_RF1	14	P	**VB_RF1 —** regulated supply voltage
ADC1	15	I	**ADC1 —** ADC input
DIO0/ADO/SPISEL1/ADC3	16	I/O	**DIO0 —** DIO0
			ADO — antenna diversity odd output
			SPISEL1 — SPI-bus master select output 1
			ADC3 — ADC input: ADC3
DIO1/ADE/SPISEL2/ADC4/PC0	17	I/O	**DIO1 —** DIO1
			ADE — antenna diversity even output
			SPISEL2 — SPI-bus master select output 2
			ADC4 — ADC input: ADC4
			PC0 — pulse counter 0 input
DIO2/RFRX/TIM0CK_GT/ADC5	18	I/O	**DIO2 —** DIO2
			RFRX — radio receiver control output
			TIM0CK_GT — timer0 clock/gate input
			ADC5 — ADC input: ADC5

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
DIO3/RFTX/TIM0CAP/ADC6	19	I/O	**DIO3 —** DIO3
			RFTX — radio transmitter control output
			TIM0CAP — timer0 capture input
			ADC6 — ADC input: ADC6
DO0/SPICLK/PWM2[2]	20	O	**DO0 —** DO0
			SPICLK — SPI-bus master clock output
			PWM2 — PWM2 output
V_{SS}	21	GND	**V_{SS} —** ground
DO1/SPIMISO/PWM3[3]	22	I/O	**DO1 —** DO1
			SPIMISO — SPI-bus Master In, Slave Out input
			PWM3 — PWM3 output
DIO18/SPIMOSI	23	I/O	**DIO18 —** DIO18
			SPIMOSI — SPI-bus Master Out Slave In output
DIO19/SPISEL0	24	I/O	**DIO19 —** DIO19
			SPISEL0 — SPI-bus master Select Output 0
i.c.	25	-	internally connected; leave open
DIO4/CTS0/JTAG_TCK/TIM0OUT/PC0	26	I/O	**DIO4 —** DIO4
			CTS0 — UART 0 clear to send input
			JTAG_TCK — JTAG CLK input
			TIM0OUT — timer0 PWM output
			PC0 — pulse counter 0 input
DIO5/RTS0/JTAG_TMS/PWM1/PC1	27	I/O	**DIO5 —** DIO5
			RTS0 — UART 0 request to send output
			JTAG_TMS — JTAG mode select input
			PWM1 — PWM1 output
			PC1 — pulse counter 1 input
DIO6/TXD0/JTAG_TDO/PWM2	28	I/O	**DIO6 —** DIO6
			TXD0 — UART 0 transmit data output
			JTAG_TDO — JTAG data output
			PWM2 — PWM2 data output
DIO7/RXD0/JTAG_TDI/PWM3	29	I/O	**DIO7 —** DIO7
			RXD0 — UART 0 receive data input
			JTAG_TDI — JTAG data input
			PWM3 — PWM 3 data output
V_{DDD}	30	P	**V_{DDD} —** digital supply voltage
DIO8/TIM0CK_GT/PC1/PWM4	31	I/O	**DIO8 —** DIO8
			TIM0CK_GT — timer0 clock/gate input
			PC1 — pulse counter1 input
			PWM4 — PWM 4 output

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
DIO9/TIM0CAP/32KXTALIN/RXD1/32KIN	32	I/O	**DIO9 —** DIO9
			TIM0CAP — Timer0 Capture input
			32KXTALIN — 32 kHz External Crystal input
			RXD1 — UART1 Receive Data input
			32KIN — 32 kHz External clock input
DIO10/TIM0OUT/32KXTALOUT	33	I/O	**DIO10 —** DIO10
			TIM0OUT — Timer0 PWM Output
			32KXTALOUT — 32 kHz External Crystal output
DIO11/PWM1/TXD1	34	I/O	**DIO11 —** DIO11
			PWM1 — PWM1 output
			TXD1 — UART1 Transmit Data output
VB_DIG	35	P	**VB_DIG —** regulated supply voltage
DIO12[4]	36	I/O	**DIO12 —** DIO12
			PWM2 — PWM2 output
			CTS0 — UART0 clear to send input
			JTAG_TCK — JTAG CLK input
			ADO — antenna diversity odd output
			SPISMOSI — SPI-bus slave Master Out, Slave In input
DIO13[5]	37	I/O	**DIO13 —** DIO13
			PWM3 — PWM3 output
			RTS0 — UART0 request to send output
			JTAG_TMS — JTAG mode select input
			ADE — antenna diversity even output
			SPISMISO — SPI-bus slave master in slave out output
DIO14[6]	38	I/O	**DIO14 —** DIO14
			SIF_CLK — serial interface clock
			TXD0 — UART 0 transmit data output
			TXD1 — UART 1 transmit data output
			JTAG_TDO — JTAG data output
			SPISEL1 — SPI-bus master select output 1
			SPISSEL — SPI-bus slave select input
V_{SS}	39	GND	**V_{SS} —** ground
DIO15[7]	40	I/O	**DIO15 —** DIO15
			SIF_D — serial interface data
			RXD0 — UART 0 receive data input
			RXD1 — UART 1 receive data input
			JTAG_TDI — JTAG data input
			SPISEL2 — SPI-bus master select output 2
			SPISCLK — SPI-bus slave clock input
V_{SSA}	-	GND	**V_{SSA} —** Exposed die paddle

[1] P = power supply; G = ground; I = input, O = output; I/O = input/output.

[2] JTAG programming mode: must be left floating high during reset to avoid entering JTAG programming mode.

[3] UART programming mode: leave pin floating high during reset to avoid entering UART programming mode or hold it low to program.

[4] Multi-function: DIO12/PWM2/CTS0/JTAG_TCK/ADO/SPISMOSI.

[5] Multi-function: DIO13/PWM3/RTS0/JTAG_TMS/ADE/SPISMISO.

[6] Multi-function: DIO14/SIF_CLK/TXD0/TXD1/JTAG_TDO/SPISEL1/SPISSEL.

[7] Multi-function: DIO15/SIF_D/RXD0/RXD1/JTAG_TDI/SPISEL2/SPISCLK.

The PCB schematic and layout rules detailed in Section 15.1 must be followed. Failure to do so will likely result in the JN5169 failing to meet the performance specification detailed in this data sheet and the worst case may result in the device not functioning in the end application.

8.2.1 Power supplies

The device is powered from the V_{DDA} and V_{DDD} pins, each being decoupled with a 100 nF ceramic capacitor. V_{DDA} is the power supply to the analog circuitry; it should be decoupled to ground. V_{DDD} is the power supply for the digital circuitry; it should also be decoupled to ground. In addition, a common 10 μF tantalum capacitor is required for low frequencies. Decoupling pins for the internal 1.8 V regulators are provided with each pin requiring a 100 nF capacitor located as close to the device as practical. VB_SYNTH and VB_DIG require only a 100 nF capacitor. VB_RF1 and VB_RF2 should be connected together as close to the device as practical, and require one 100 nF capacitor and one 47 pF capacitor. The pin VB_VCO requires a 10 nF capacitor. See Figure 48 for a schematic diagram.

V_{SSA} and V_{SS} are the ground pins.

Users are strongly discouraged from connecting their own circuits to the 1.8 V regulated supply pins, as the regulators have been optimized to supply only enough current for the internal circuits.

Rising V_{DD} voltage at power-up has to be done within 100 ms with a minimum I_{DD} current of 20 mA to avoid any start up issue.

8.2.2 Reset

RESET_N is an active-low reset input pin that is connected to a 500 kΩ internal pull-up resistor. It may be pulled low by an external circuit. See Section 9.4.2 for more details.

8.2.3 32 MHz oscillator

A crystal is connected between XTAL_IN and XTAL_OUT to form the reference oscillator, which drives the system clock. A capacitor to analog ground is required on each of these pins. See Section 9.3.1 for more details. The 32 MHz reference frequency is divided down to 16 MHz and this is used as the system clock throughout the device.

8.2.4 Radio

The radio is a single-ended design, requiring two capacitors and just two inductors to match the 50 Ω microstrip line to the RF_IO pin. In addition, extra-components are added on the line for filtering purpose.

An external resistor (43 kΩ) is required between IBIAS and analog ground (paddle) to set various bias currents and references within the radio.

8.2.5 Analog peripherals

The ADC requires a reference voltage to use as part of its operation. It can use either an internal reference voltage or an external reference connected to VREF. This voltage is referenced to analog ground and the performance of the analog peripherals is dependent on the quality of this reference.

There are 6 ADC inputs and a pair of comparator inputs. ADC1 has a designated input pin but ADC2 uses the same pin as VREF, invalidating its use as an ADC pin when an external reference voltage is required. The remaining 4 ADC channels are shared with the digital I/Os DIO0, DIO1, DIO2 and DIO3. When these 4 ADC channels are selected, the corresponding DIOs must be configured as inputs with their pull-ups disabled. Similarly, the comparator shares pins 1 and 2 with DIO16 and DIO17, so when the comparator is selected these pins must be configured as inputs with their pull-ups disabled. The analog I/O pins on the JN5169 can have signals applied up to 0.3 V higher than V_{DDA}. A schematic view of the analog I/O cell is shown in Figure 4. Figure 5 demonstrates a special case, where a digital I/O pin doubles as an input to analog devices. This applies to ADC3, ADC4, ADC5, ADC6, COMP1P and COMP1M.

In reset, sleep and deep sleep, the analog peripherals are all OFF. In sleep, the comparator may optionally be used as a wake-up source.

On platform with higher power (e.g. light Bulb, Smart Plug), unused ADC and comparator inputs should not be left unconnected, but connected to analog ground.

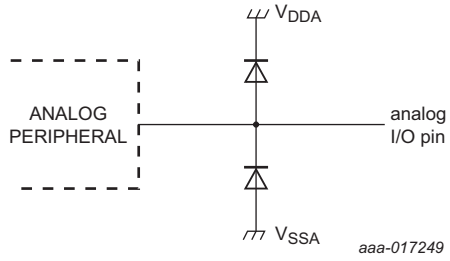
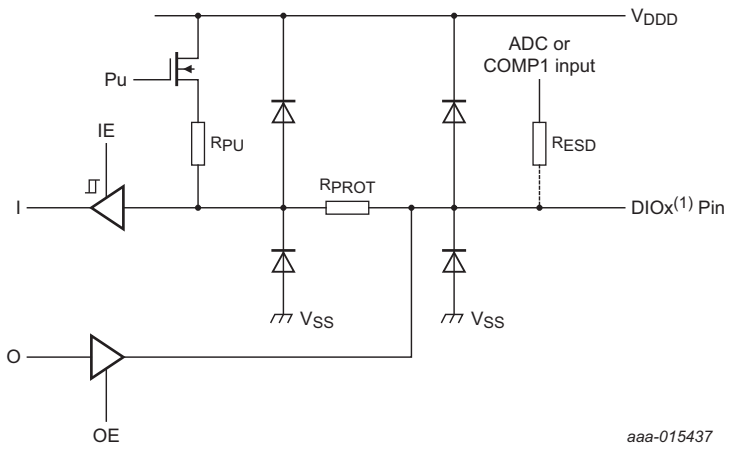


Fig 4. Analog I/O cell

8.2.6 Digital Input/Output

For the DC properties of these pins, see Section 14.2. When used in their primary function, all Digital Input/Output pins are bidirectional and are connected to weak internal pull-up resistors (50 kΩ nominal) that can be disabled. When used in their secondary function (selected when the appropriate peripheral block is enabled through software library calls), their direction is fixed by the function. The pull-up resistor is enabled or disabled independently of the function and direction; the default state from reset is enabled.

A schematic view of the Digital I/O cell shown in Figure 5. The dotted lines through resistor R_{ESD} represent a path that exists only on DIO0, DIO1, DIO2, DIO3, DIO16 and DIO17 which are also inputs to the ADC (ADC3, ADC4, ADC5 and ADC6) and Comparator (COMP1P and COMP1M) respectively. To use these DIO pins for their analog functions, the DIO must be set as an input with its pull-up resistor, R_{PU}, disabled.



(1) With x = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18 or 19.

Fig 5. DIO equivalent schematic

In reset, the digital peripherals are all off and the DIO pins are set as high-impedance inputs. During sleep and deep sleep, the DIO pins retain both their input/output state and the output level that was set at the start of sleep. If the DIO pins were enabled as inputs and the interrupts were enabled, then these pins may be used to wake up the JN5169 from sleep.

9. Functional description

9.1 CPU

The CPU of the JN5169 is a 32-bit load and store RISC processor. It has been architected for 3 key requirements:

- Low power consumption for battery powered applications
- High performance to implement a wireless protocol at the same time as complex applications
- Efficient coding of high-level languages such as C provided with the Software Developer's Kit

It features a linear 32-bit logical address space with unified memory architecture, accessing both code and data in the same address space. Registers for peripheral units, such as the timers, UART and the baseband processor, are also mapped into this space.

The CPU has access to a block of 15 × 32-bit General-Purpose (GP) registers together with a small number of special purpose registers which are used to store processor state and control interrupt handling. The contents of any GP register can be loaded from or stored to memory. Arithmetic and logical operations, shift and rotate operations, and signed and unsigned comparisons can be performed either between two registers and stored in a third, or between registers and a constant carried in the instruction. Operations between general or special-purpose registers execute in one cycle while those that access memory requires a further cycle to allow the memory to respond.

The instruction set manipulates 8-bit, 16-bit and 32-bit data; this means that programs can use objects of these sizes very efficiently. Manipulation of 32-bit quantities is particularly useful for protocols and high-end applications allowing algorithms to be implemented in fewer instructions than on smaller word-size processors, and allowing execution in fewer clock cycles. In addition, the CPU supports hardware Multiply that can be used to efficiently implement algorithms needed by Digital Signal Processing applications.

The instruction set is designed for the efficient implementation of high-level languages such as C. Access to fields in complex data structures is very efficient due to the provision of several addressing modes, together with the ability to use any of the GP registers to contain the address of objects. Subroutine parameter passing is also made more efficient by using GP registers rather than pushing objects onto the stack. The recommended programming method for the JN5169 is to use C, which is supported by a software developer kit comprising a C compiler, linker and debugger.

The CPU architecture also contains features that make the processor suitable for embedded, real-time applications. In some applications, it may be necessary to use a real-time operating system to allow multiple tasks to run on the processor. To provide protection for device-wide resources being altered by one task and affecting another, the processor can run in either supervisor or user mode, the former allowing access to all processor registers, while the latter only allows the GP registers to be manipulated. Supervisor mode is entered on reset or interrupt; tasks starting up would normally run in user mode in an RTOS environment.

Embedded applications require efficient handling of external hardware events. Exception processing (including reset and interrupt handling) is enhanced by the inclusion of a number of shadow registers into which the PC and status register contents are copied as part of the operation of the exception hardware. This means that the essential registers for exception handling are stored in one cycle, rather than the slower method of pushing them onto the processor stack. The PC is also loaded with the vector address for the exception that occurred, allowing the handler to start executing in the next cycle.

To improve power consumption, a number of power-saving modes are implemented in the JN5169, described more fully in Section 10. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on an interrupt it will wake up to service the request. Additionally, it is possible under software control to set the speed of the CPU to 1 MHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz or 32 MHz. This feature can be used to trade off processing power against current consumption.

9.2 Memory organization

This section describes the different memories found within the JN5169. The device contains Flash, RAM and EEPROM memory, the wireless transceiver and peripherals all within the same linear address space.

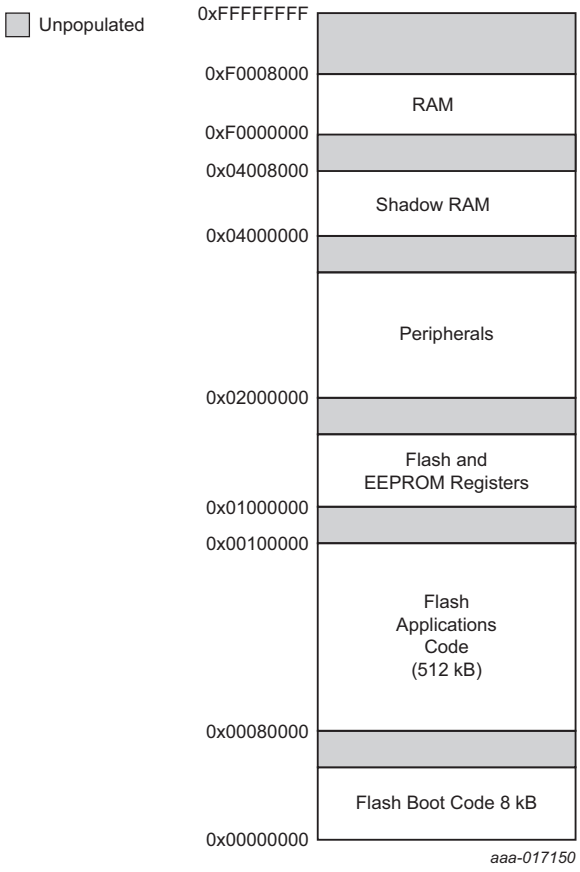


Fig 6. JN5169 memory map

9.2.1 Flash

The embedded Flash consists of 2 parts: an 8 kB region used for holding boot code and a 512 kB region used for application code. The maximum number of write cycles or endurance is 10 k guaranteed, and typically 50 k, while the data retention is guaranteed for at least 10 years. The boot code region is pre-programmed by NXP on supplied parts and contains code to handle reset, interrupts and other events (see Section 6). It also contains a Flash Programming interface to allow interaction with the PC-based Flash programming utility which allows user code compiled using the supplied toolchain to be programmed into the Application space. For further information, see the Application Note on the Wireless Connectivity area of the NXP web site Ref. 1.

9.2.2 RAM

The JN5169 devices contain 32 kB of high-speed RAM, which can be accessed by the CPU in a single clock cycle. It is primarily used to hold the CPU Stack together with program variables and data. If necessary, the CPU can execute code contained within the RAM (although it would normally just execute code directly from the embedded Flash). Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are unpowered, allowing a quicker resumption of processing once woken.

9.2.3 OTP configuration memory

The JN5169 devices contain a quantity of One Time Programmable (OTP) memory as part of the embedded Flash (Index Sector). This can be used to securely hold such things as a user 64-bit MAC address and a 128-bit AES security key. A limited number of further bits are available for customer use for storage of configuration or other information. By default, the 64-bit MAC address is pre-programmed by NXP on supplied parts; however, customers can use their own MAC address and override the default one. The user MAC address and other data can be written to the OTP memory using the Flash programmer. Details on how to obtain and install MAC addresses can be found in the dedicated Application Note.

For further information on how to program and use this facility, see BeyondStudio for NXP User Guide (JN-UG-3098) on the Wireless Connectivity area of the NXP web site Ref. 1.

9.2.4 EEPROM

The JN5169 devices contain 4 kB of EEPROM. The maximum number of write cycles or endurance is 100 k guaranteed, and 500 k typically, while the data retention is guaranteed for at least 10 years. This non-volatile memory is primarily used to hold persistent data generated from such things as the network stack software component (for example network topology, routing tables). As the EEPROM holds its contents through sleep and reset events, more stable operation and faster recovery is possible after outages. Access to the EEPROM is via registers mapped into the Flash and EEPROM registers region of the address map.

The customer may use part of the EEPROM to store their own data by interfacing with the Persistent Data Manager (PDM). Optionally, the PDM can also store data in an external memory. For further information, see the Wireless Connectivity area of the NXP web site Ref. 1.

9.2.5 External memory

An optional external serial non-volatile memory (for instance Flash or EEPROM) with a SPI-bus interface may be used to provide additional storage for program code, such as a new code image or further data for the device when external power is removed. The memory can be connected to the SPI-bus master interface using select line SPISEL0 (see Figure 7 for details).

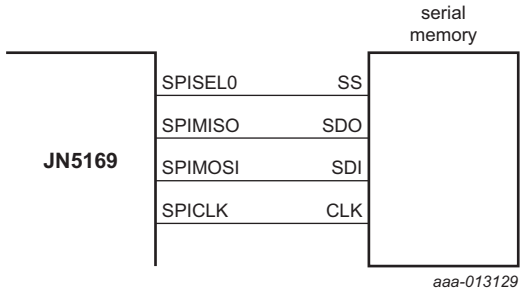


Fig 7. Connecting external serial memory

The contents of the external serial memory may be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in the Flash memory

index sector. When bootloading program code from external serial memory, the JN5169 automatically accesses the encryption key to execute the decryption process. The user program code does not need to handle any of the decryption processes; it is transparent. For more details, including the how the program code encrypts data for the external memory, see the Application Note *JN51xx Boot Loader Operation (JN-AN-1003)* on the Wireless Connectivity area of the NXP web site Ref. 1.

9.2.6 Peripherals

All peripherals have their registers mapped into the memory space. Access to these registers requires three peripheral clock cycles. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see *JN516x Integrated Peripherals API User Guide (JN-UG-3087)* on the Wireless Connectivity area of the NXP web site Ref. 1.

9.2.7 Unused memory address

Any attempt to access an unpopulated memory area will result in a bus error exception (interrupt) being generated.

9.3 System clocks

Two system clocks are used to drive the on-chip subsystems of the JN5169. The wake-up timers are driven from a low frequency clock (notionally 32 kHz). All other subsystems (transceiver, processor, memory and digital and analog peripherals) are driven by a high-speed clock (notionally 32 MHz), or a divided-down version of it.

The high-speed clock is either generated by the accurate crystal-controlled oscillator (32 MHz) or the less accurate high-speed RC oscillator (27 MHz to 32 MHz calibrated). The low-speed clock is either generated by the accurate crystal-controlled oscillator (32 kHz to 768 kHz), the less accurate RC oscillator (centered on 32 kHz) or can be supplied externally.

9.3.1 High-speed (32 MHz) system clock

The selected high-speed system clock is used directly by the radio subsystem, whereas a divided-by-two version is used by the remainder of the transceiver and the digital and analog peripherals. The direct or divided-down version of the clock is used to drive the processor and memories (32 MHz, 16 MHz, 8 MHz, 4 MHz, 2 MHz or 1 MHz).

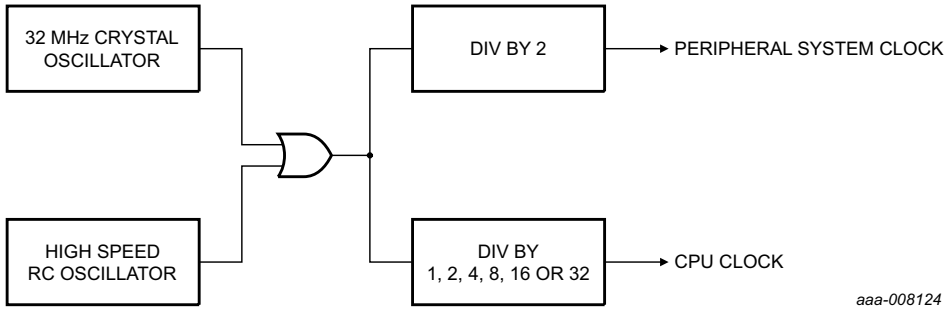


Fig 8. System and CPU clocks

Crystal oscillators are generally slow to start. Hence to provide a fast start-up following a sleep cycle or reset, the fast RC oscillator is always used as the initial source for the high-speed system clock. The oscillator starts very quickly and will run at 25 MHz to 32 MHz (uncalibrated) or 32 MHz ±5 % (calibrated). Although this means that the system clock will be running at an undefined frequency (slightly slower or faster than nominal), this does not prevent the CPU and Memory subsystems operating normally, so the program code can execute. However, it is not possible to use the radio or UARTs, as even after calibration (initiated by the user software calling an API function) there is still a ±5 % tolerance in the clock rate over voltage and temperature. Other digital peripherals can be used (e.g. SPI-bus master/slave), but care must be taken if using timers due to the clock frequency inaccuracy.

Further details of the high-speed RC oscillator can be found in Section 9.3.1.2

On wake-up from sleep, the JN5169 uses the fast RC oscillator. It can then either:

- Automatically switch over to use the 32 MHz clock source when it has started up
- Continue to use the fast RC oscillator until software triggers the switch-over to the 32 MHz clock source - for example, when the radio is required
- Continue to use the RC oscillator until the device goes back into one of the sleep modes

The use of the fast RC oscillator at wake-up means that there is no need to wait for the 32 MHz crystal oscillator to stabilize. Consequently, the application code will start executing quickly using the clock from the high-speed RC oscillator.

9.3.1.1 32 MHz crystal oscillator

The JN5169 contains the necessary on-chip components to build a 32 MHz reference oscillator with the addition of an external crystal resonator and two tuning capacitors. The schematic of these components is shown in Figure 8. The two capacitors, C1 and C2, should typically be 12 pF and use a C0G dielectric. Due to the small size of these capacitors, it is important to keep the traces to the external components as short as possible. The on-chip transconductance amplifier is compensated for temperature variation and is self-biasing by means of the internal resistor R1. This oscillator provides the frequency reference for the radio and therefore it is essential that the reference PCB layout and BOM are carefully followed. The oscillator includes a function which flags when the amplitude of oscillation has reached a satisfactory level for full operation, and this is checked before the source of the high-speed system clock is changed to the 32 MHz crystal oscillator.

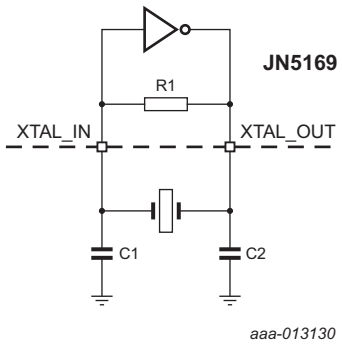


Fig 9. 32 MHz crystal oscillator connections

9.3.1.2 High-speed RC oscillator

An on-chip high-speed RC oscillator is provided in addition to the 32 MHz crystal oscillator for two purposes; to allow a fast start-up from reset or sleep and to provide a lower current alternative to the crystal oscillator for non-timing critical applications. By default the oscillator will run at 27 MHz, typically, with a wide tolerance. It can be calibrated, using a software API function, which will result in a nominal frequency of 32 MHz with a ±1.6% tolerance at 3 V and 25 °C. However, it should be noted that over the full operating range of voltage and temperature this will increase to ±5%. The calibration information is retained through speed cycles and when the oscillator is disabled, so typically the calibration function only needs to be called once. No external components are required for this oscillator. The electrical specification of the oscillator can be found in Section 14.3.9.

9.3.2 Low-speed (32 kHz) system clock

The 32 kHz system clock is used for timing the length of a sleep period (see Section 10). The clock can be selected from one of three sources through the application software:

- 32 kHz RC oscillator
- 32 kHz crystal oscillator
- 32 kHz external clock

Upon a chip reset or power-up, the JN5169 defaults to using the internal 32 kHz RC oscillator. If another clock source is selected, then it will remain in use for all 32 kHz timing until a chip reset is performed.

9.3.2.1 32 kHz RC oscillator

The internal 32 kHz RC oscillator requires no external components. The internal timing components of the oscillator have a wide tolerance due to manufacturing process variation and so the oscillator runs nominally at 32 kHz −10 % +40 %. To make this useful as a timing source for accurate wake-up from sleep, a frequency calibration factor derived from the more accurate 16 MHz clock may be applied. The calibration factor is derived through software; details can be found in Section 9.9.9. Software must check that the 32 kHz RC oscillator is running before using it. The oscillator has a default current consumption of around 0.5 μA. Optionally, this can be reduced to 0.375 μA. However, the calibrated accuracy and temperature coefficient will be worse as a consequence.

9.3.2.2 32 kHz crystal oscillator

In order to obtain more accurate sleep periods, the JN5169 contains the necessary on-chip components to build a 32 kHz oscillator with the addition of an external 32.768 kHz crystal and two tuning capacitors. The crystal should be connected between 32KXTALIN and 32KXTALOUT (DIO9 and DIO10), with two equal capacitors to ground, one on each pin. Due to the small size of the capacitors, it is important to keep the traces to the external components as short as possible.

The electrical specification of the oscillator can be found in Section 14.3.9. The oscillator cell is flexible and can operate with a range of commonly available 32.768 kHz crystals with load capacitances from 6 pF to 12.5 pF. However, the maximum ESR of the crystal and the supply current are both functions of the actual crystal used.

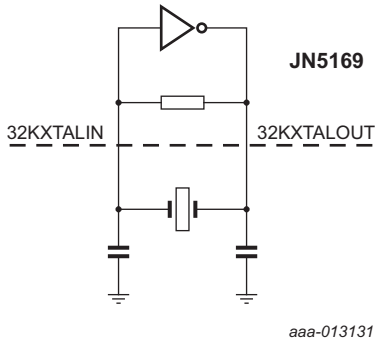


Fig 10. 32 kHz crystal oscillator connections

9.3.2.3 32 kHz external clock

An externally supplied 32 kHz reference clock on the 32KIN input (DIO9) may be provided to the JN5169. This would allow the 32 kHz system clock to be sourced from a very stable external oscillator module, allowing more accurate sleep cycle timings compared to the internal RC oscillator.

9.4 Reset

A system reset initializes the device to a pre-defined state and forces the CPU to start program execution from the reset vector. The reset process that the JN5169 goes through is as follows.

When power is first applied or when the external reset is released, the high-speed RC oscillator and 32 MHz crystal oscillator are activated. After a short wait period (approximately 13 μs) while the high-speed RC starts up, and as long as the supply voltage satisfies the default Supply Voltage Monitor (SVM) threshold (2.0 V + 0.045 V hysteresis), the internal 1.8 V regulators are turned on to power the processor and peripheral logic. The regulators are allowed to stabilize (about 15 μs) followed by a further wait (approximately 150 μs) to allow the Flash and EEPROM bandgaps to stabilize and allow their initialization, including reading the user SVM threshold from the Flash. This is applied to the SVM, and after a brief pause (approximately 2.5 μs) the SVM is checked again. If the supply is above the new SVM threshold, the CPU and peripheral logic are released from reset and the CPU starts to run code beginning at the reset vector. This runs the bootloader code contained within the Flash, which looks for a valid application to run, first from the internal Flash and then from any connected external serial memory over

the SPI-bus master interface. Once found, required variables are initialized in RAM before the application is called at its AppColdStart entry point. For more details on the bootloader, see the Application Note on the Wireless Connectivity area of the NXP web site Ref. 1.

The JN5169 has 5 sources of reset:

- Internal Power-On Reset/Brown-Out Reset (BOR)
- External reset
- Software reset
- Watchdog timer
- Supply voltage detect

Remark: When the device exits a reset condition, device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, then the device must be held in reset until the operating conditions are met (see Section 14.3.1)

9.4.1 Internal Power-On Reset/Brown-Out Reset (BOR)

For the majority of applications, the Internal Power-On Reset is capable of generating the required reset signal. When power is applied to the device, the Power-On Reset circuit monitors the rise of the V_{DD} supply. When the V_{DD} reaches the specified threshold, the reset signal is generated. This signal is held internally until the power supply and oscillator stabilization time has elapsed, when the internal reset signal is then removed and the CPU is allowed to run.

The BOR circuit has the ability to reject spikes on the V_{DD} rail to avoid false triggering of the reset module. Typically for a negative going square pulse of duration 1 μs, the voltage must fall to 1.2 V before a reset is generated. Similarly for a triangular wave pulse of 10 μs width, the voltage must fall to 1.3 V before causing a reset. The exact characteristics are complex and these are only examples. See Figure 42 for more details on BOR and SVM characteristics.

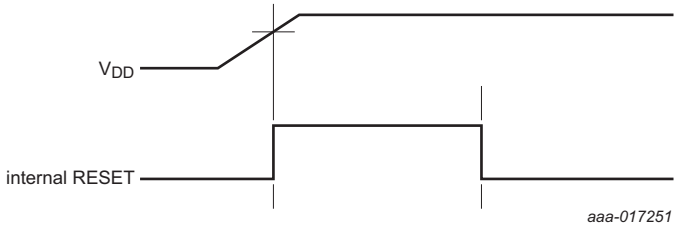


Fig 11. Internal Power-On Reset

When the supply drops below the POR 'falling' threshold, it will retrigger the reset. On platform with higher power (e.g. light bulb, smart plug) it is recommended to use this external circuit to avoid unexpected reset due to spurs.

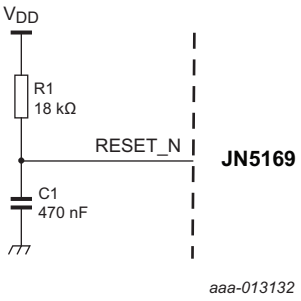


Fig 12. External reset generation

The external resistor and capacitor provide a simple reset operation when connected to the RESET_N pin but are not necessary.

9.4.2 External reset

An external reset is generated by a low level on the RESET_N pin. Reset pulses longer than the minimum pulse width will generate a reset during active or sleep modes. Shorter pulses are not guaranteed to generate a reset. The JN5169 is held in reset while the RESET_N pin is low. When the applied signal reaches the reset threshold voltage (V_{rst}) on its positive edge, the internal reset process starts.

The JN5169 has an internal 500 kΩ pull-up resistor connect to the RESET_N pin. The pin is an input for an external reset only. By holding the RESET_N pin low, the JN5169 is held in reset, resulting in a typical current of 6 μA.

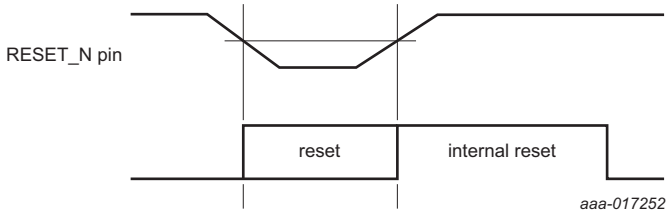


Fig 13. External reset

9.4.3 Software reset

A system reset can be triggered at any time through software control, causing a full chip reset and invalidating the RAM contents. For example, this can be executed within a user's application upon detection of a system failure.

9.4.4 Supply Voltage Monitor (SVM)

An internal SVM is used to monitor the supply voltage to the JN5169; this can be used while the device is awake or is in CPU doze mode. Dips in the supply voltage below a variable threshold can be detected and can be used to cause the JN5169 to perform a chip reset. Equally, dips in the supply voltage can be detected and used to cause an interrupt to the processor, when the voltage either drops below the threshold or rises above it.

The SVM is enabled by default from power-up and can extend the reset during power-up. This will keep the CPU in reset until the voltage exceeds the SVM threshold voltage. The threshold voltage is configurable to 1.95 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.7 V or 3.0 V and is controllable by software. From power-up, the threshold is set according to the value stored in Flash and the default chip configuration is for the 2.0 V threshold. It is expected that the threshold is set to the minimum needed by the system. See Figure 42 for more details on BOR and SVM characteristics.

9.4.5 Watchdog timer

A watchdog timer is provided to guard against software lock-ups. It operates by counting cycles of the high-speed RC system clock. A pre-scaler is provided to allow the expiry period to be set between typically 8 ms and 16.4 s (dependent on high-speed RC accuracy: +30 %, −15 %). Failure to restart the watchdog timer within the pre-configured timer period will cause a chip reset to be performed. A status bit is set if the watchdog was triggered so that the software can differentiate watchdog initiated resets from other resets, and can perform any required recovery once it restarts. Optionally, the watchdog can cause an exception rather than a reset; this preserves the state of the memory and is useful for debugging.

After power-up, reset, start from deep sleep or start from sleep, the watchdog is always enabled with the largest time-out period and will commence counting as if it had just been restarted. Under software control, the watchdog can be disabled. If it is enabled, the user must regularly restart the watchdog timer to stop it from expiring and causing a reset. The watchdog runs continuously, even during doze. However the watchdog does not operate during sleep or deep sleep, or when the hardware debugger has taken control of the CPU. If enabled, it will restart automatically once the debugger has unstalled the CPU.

9.5 Interrupt system

A hardware-vectored interrupt system is provided on the JN5169. The JN5169 provides several interrupt sources, some associated with CPU operations (CPU exceptions) and others which are used by hardware in the device. When an interrupt occurs, the CPU stops executing the current program and loads its program counter with a fixed hardware address specific to that interrupt. The interrupt handler or interrupt service routine is stored at this location and is run on the next CPU cycle. Execution of interrupt service routines is always performed in supervisor mode. Interrupt sources and their vector locations are shown in Table 3.

Table 3. Interrupt vectors

Interrupt source	Vector location	Interrupt definition
Bus error	0x08	typically caused by an attempt to access an invalid address or a disabled peripheral
Tick timer	0x0E	tick timer interrupt asserted
Alignment error	0x14	load/store address to non-naturally aligned location
Illegal instruction	0x1A	attempt to execute an unrecognized instruction
Hardware interrupt	0x20	interrupt asserted
System call	0x26	system call initiated by b.sys instruction
Trap	0x2C	caused by the b.trap instruction or the debug unit
Reset	0x38	caused by software or hardware reset
Stack overflow	0x3E	stack overflow

9.5.1 System calls

The b.trap and b.sys instructions allow processor exceptions to be generated by software.

A system call exception will be generated when the b.sys instruction is executed. This exception can, for example, be used to enable a task to switch the processor into supervisor mode when a real-time operating system is in use (see Section 9.5.3 for further details).

The b.trap instruction is commonly used for trapping errors and for debugging.

9.5.2 Processor exceptions

9.5.2.1 Bus error

A bus error exception is generated when software attempts to access a memory address that does not exist, or is not populated with memory or peripheral registers.

9.5.2.2 Alignment

Alignment exceptions are generated when software attempts to access objects that are not aligned to natural word boundaries. 16-bit objects must be stored on even byte boundaries, while 32-bit objects must be stored on quad byte boundaries. For instance, attempting to read a 16-bit object from address 0xFFF1 will trigger an alignment exception as will a read of a 32-bit object from 0xFFF1, 0xFFF2 or 0xFFF3. Examples of legal 32-bit object addresses are 0xFFF0, 0xFFF4, 0xFFF8 etc.

9.5.2.3 Illegal instruction

If the CPU reads an unrecognized instruction from memory as part of its instruction fetch, it will cause an illegal instruction exception.

9.5.2.4 Stack overflow

When enabled, a stack overflow exception occurs if the stack pointer reaches a programmable location.

9.5.3 Hardware interrupts

Hardware interrupts generated from the transceiver, analog or digital peripherals and DIO pins are individually masked using the Programmable Interrupt Controller (PIC). Management of interrupts is provided in the *JN516x Integrated Peripherals API User Guide (JN-UG-3087)* on the Wireless Connectivity area of the NXP web site Ref. 1. For details of the interrupts generated from each peripheral, see the respective section in this data sheet.

Interrupts can be used to wake the JN5169 from sleep. The peripherals, baseband controller, security coprocessor and PIC are powered down during sleep but the DIO interrupts and optionally the pulse counters, wake-up timers and analog comparator interrupts remain powered to bring the JN5169 out of sleep.

Prioritized external interrupt handling (i.e., interrupts from hardware peripherals) is provided to enable an application to control an events priority to provide for deterministic program execution.

The priority Interrupt controller provides 15 levels of prioritized interrupts. The priority level of all interrupts can be set, with value 0 being used to indicate that the source can never produce an external interrupt, 1 for the lowest priority source(s) and 15 for the highest priority source(s). Note that multiple interrupt sources can be assigned the same priority level if desired.

If while processing an interrupt, a new event occurs at the same or lower priority level, a new external interrupt will not be triggered. However, if a new higher priority event occurs, the external interrupt will again be asserted, interrupting the current interrupt service routine.

Once the interrupt service routine is complete, lower priority events can be serviced.

9.6 Wireless transceiver

The wireless transceiver comprises a 2.4 GHz radio, modem, a baseband processor, a security coprocessor and PHY controller. These blocks, with protocol software provided as a library, implement an IEEE802.15.4 standards-based wireless transceiver that transmits and receives data over the air in the unlicensed 2.4 GHz band.

9.6.1 Radio

Figure 14 shows the single ended radio architecture.

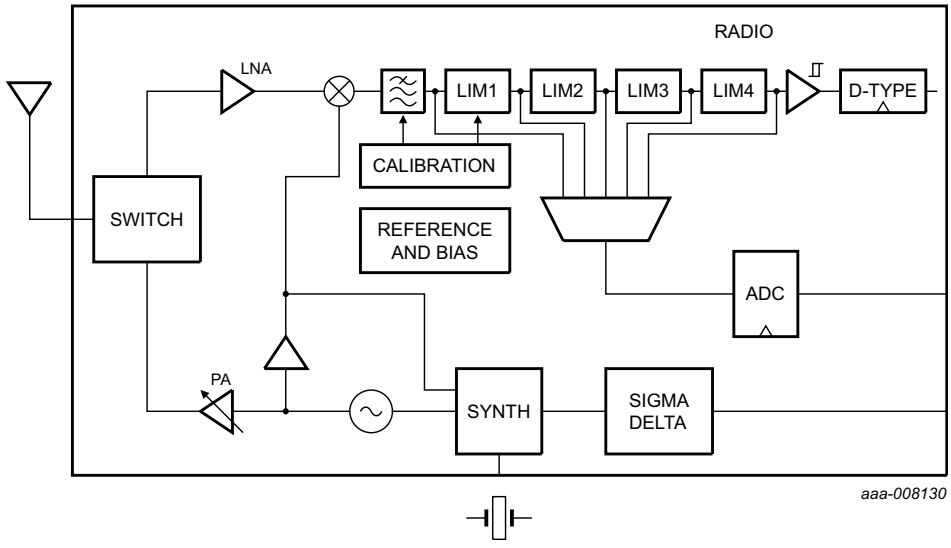


Fig 14. Radio architecture

The radio comprises a low-IF receive path and a direct modulation transmit path, which converge at the TX/RX switch. The switch connects to the external single-ended matching network, which consists of two inductors and a capacitor. This arrangement creates a 50 Ω port and removes the need for a balun. A 50 Ω single-ended antenna can be connected directly to this port.

The 32 MHz crystal oscillator feeds a divider, which provides the frequency synthesizer with a reference frequency. The synthesizer contains programmable feedback dividers, phase detector, charge pump and internal Voltage Controlled Oscillator (VCO). The VCO has no external components, and includes calibration circuitry to compensate for