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JN517x

IEEE802.15.4 Wireless Microcontroller

Rev. 2.0 — 8 November 2016 Product data sheet

1. General description

The JN517x series is a range of ultra low power, high performance wireless microcontrollers suitable for Thread and ZigBee applications to facilitate the development of Smart Home and Smart Lighting applications. It features a high-performance and low-power ARM Cortex-M3 processor with debug with programmable clock speeds. The JN517x devices are available in JN5174, JN5178 and JN5179 variants, respectively having 160 kB, 256 kB and 512 kB of embedded Flash memory as well as 32 kB of RAM and 4 kB of EEPROM. The embedded Flash can support “Over-The-Air” code download of software stacks. Radio transmit power is configurable up to +10 dBm output. The very-low receive operating current (down to 12.7 mA and with a 0.6 μA sleep timer mode) gives excellent battery life allowing operation direct from a coin cell. The JN517x also includes a 2.4 GHz “IEEE802.15.4 compliant” transceiver and a comprehensive mix of analog and digital peripherals.

The JN517x is ideal for battery-operated applications supported through the comprehensive power-saving modes available in the device. The on-chip peripherals, which include a fail-safe I^2C-bus, SPI-bus ports (both master and slave), and a six-channel analog-digital converter with internal temperature sensor support a wide range of applications directly without extra hardware.

2. Features and benefits

2.1 Benefits

- Very low current solution for long battery life: over 10 years
- Very low receive current for low standby power of receiver always on nodes
- Integrated power amplifier for long range and robust communication
- Large embedded Flash memory to enable Over-The-Air (OTA) firmware updates without external Flash memory
- Single chip device to run communication stack and application
- Supports multiple network stacks
- Peripherals customized for lighting applications
- System BOM is low in component count and cost
- Flexible sensor interfacing
- Package
  - 6 × 6 mm HVQFN40, 0.5 mm pitch
  - lead-free and RoHS compliant
- Temperature range: −40 °C to +125 °C

2.2 Radio features

- 2.4 GHz IEEE802.15.4 compliant Ref. 1
- Receive current 14.8 mA, in low-power receive mode 12.7 mA
- Receiver sensitivity −96 dBm
- Configurable transmit power, for reduced current consumption, for example:
  - 10 dBm, 22.5 mA
  - 8.5 dBm, 19.6 mA
  - 3 dBm, 14 mA
- Radio link budget 106 dB
- Maximum input level of +10 dBm
- Compensation for temperature drift of crystal oscillator frequency
- 2.0 V to 3.6 V battery operation
- Antenna diversity (Auto RX)
- Integrated ultra-low-power sleep oscillator (0.6 μA)
- 100 nA deep sleep current with wake-up from external event
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers

2.3 Microcontroller features

- ARM Cortex-M3 CPU with debug support
- JN5174: 160 kB/32 kB/4 kB (Flash/RAM/EEPROM)
- JN5178: 256 kB/32 kB/4 kB (Flash/RAM/EEPROM)
- JN5179: 512 kB/32 kB/4 kB (Flash/RAM/EEPROM)
- OTA firmware upgrade capability
- 32 MHz clock selectable down to 1 MHz for low-power operation
- Dual PAN ID support
- Fail-safe I^2C-bus interface. operates as either master or slave
- 8 Timers (6 × PWM and 2 timer/counters)
- 2 low-power sleep counters
- 2 × UART, one with flow control
- SPI-bus master and slave port, 2 simultaneous selects
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- Data EEPROM with guaranteed 100 k write operations
- Supply voltage monitor with 8 programmable thresholds
- Battery voltage and temperature sensors
- 6-input 10-bit ADC
- Analog comparator
- Digital monitor for ADC
- Watchdog timer and POR
- Low-power modes controller
- Up to 18 Digital IO (DIO) and 2 digital outputs pins

3. Applications

- Robust and secure low-power wireless applications
- Thread
- ZigBee 3.0
- Commercial Building and Home Automation
- Smart Lighting networks
- Internet of Things (IoT)
- Toys and gaming peripherals
- Energy harvesting, for example self-powered light switch

4. Overview

The JN517x is an IEEE802.15.4 wireless microcontroller that provides a fully integrated solution for applications using the IEEE802.15.4 standard in the 2.4 GHz to 2.5 GHz ISM frequency band, including ZigBee PRO and Thread.

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimize this complexity, NXP provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN517x. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, it is not necessary to provide the register details of the JN517x in the data sheet.

The device includes a wireless transceiver, ARM Cortex-M3 CPU, “on-chip memory” and an extensive range of peripherals.

4.1 Wireless transceiver

The wireless transceiver comprises a 2.45 GHz radio, a modem, a baseband controller and a security coprocessor. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realized very easily. Section 15.1 describes a complete reference design including Printed-Circuit Board (PCB) design and Bill Of Materials (BOM).

The security coprocessor provides hardware-based 128-bit AES-CCM modes as specified by the IEEE802.15.4 2006 standard. Specifically this includes encryption and authentication covered by the MIC-32/-64/-128, ENC and ENC-MIC-32/-64/-128 modes of operation.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 (2006) MAC and PHY functionality under the control of a protocol stack. The transmitter is equipped with a power amplifier with 3 options for transmit power (major steps, fine steps and attenuator) see Figure 51. Applications incorporating IEEE802.15.4

functionality can be developed rapidly by combining user-developed application software with a protocol stack library.

4.2 CPU and memory

An ARM Cortex-M3 CPU allows software to be run on-chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN517x has a unified memory architecture, where code memory, data memory, peripheral devices and IO ports are organized within the same linear address space. The device contains 160 kB or 256 kB or 512 kB of Flash and 32 kB of RAM and 4 kB EEPROM.

4.3 Peripherals

The following peripherals are available on chip:

- Master SPI-bus port with 2 simultaneous select outputs
- Slave SPI-bus port
- 2 UARTs: one capable of hardware flow control (4-wire, includes RTS/CTS) and the other a 2-wire (RX/TX).
- 2 programmable timer/counters which support Pulse Width Modulation (PWM) and capture/compare, plus 6 PWM timers which support PWM and Timer modes only.
- 2 programmable sleep timers and a system tick timer
- 2-wire serial interface (compatible with SMbus and I^2C-bus) supporting master and slave operation. Fail-safe open-drain IOs for I^2C-bus.
- 18 digital IO lines (multiplexed with peripherals such as timers, SPI-bus and UARTs)
- 2 digital outputs (multiplexed with SPI-bus port)
- 10-bit, Analog-to-Digital Converter with 6 input channels. Autonomous multi-channel sampling.
- Programmable analog comparator
- Digital comparator/monitor linked to ADC
- Internal temperature sensor and battery monitor
- 2 low-power pulse counters
- Random number generator
- Watchdog Timer and Supply Voltage Monitor (SVM)
- Debug support using serial-wire or 4-pin JTAG interface
- Debug trace port with up to 4 data lines.
- Transmit and receive antenna diversity with automatic receive switching based on received energy detection

User applications access the peripherals using the Integrated Peripherals API. For further details, refer to the JN517x Integrated Peripherals API User Guide, JN-UG-3118 on the Wireless Connectivity area of the NXP web site Ref. 2. This allows applications to use a tested and easily understood view of the peripherals allowing rapid system development.

5. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
JN517x[1]	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-8

[1] x = 4: Flash = 160 kB.
x = 8: Flash = 256 kB.
x = 9: Flash = 512 kB.

For further details, refer to the Wireless Connectivity area of the NXP web site Ref. 2.

6. Block diagram

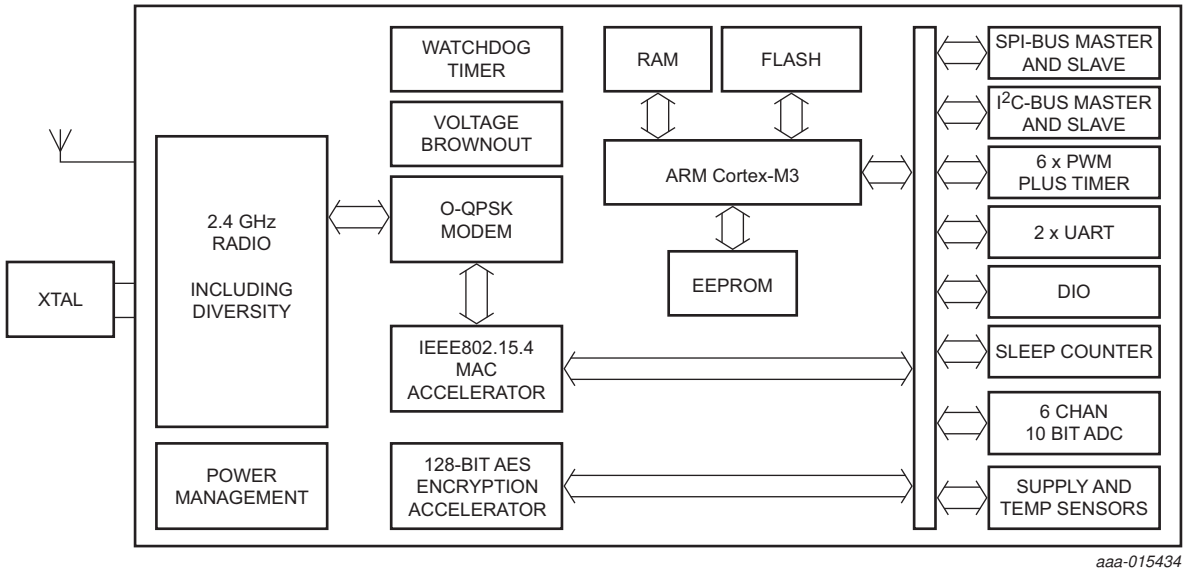
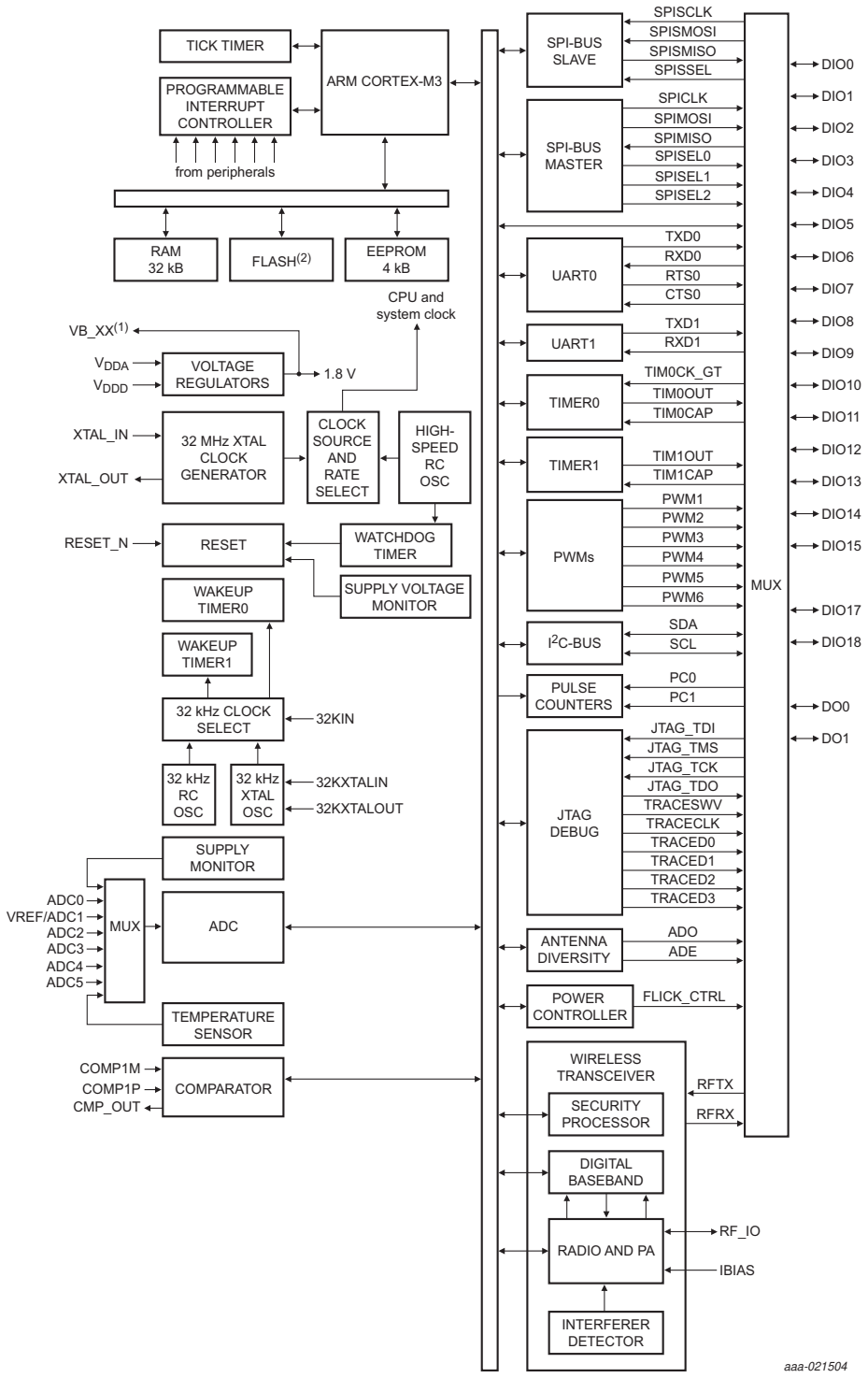


Fig 1. Block diagram

7. Functional diagram



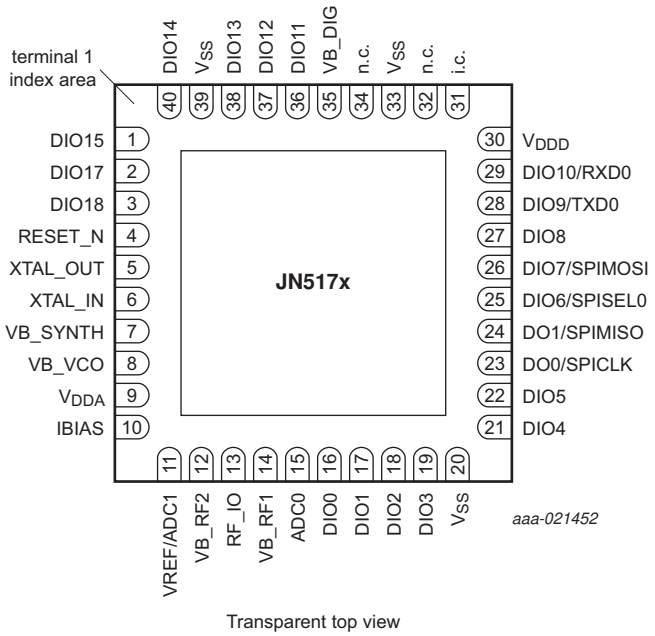
(1) With XX = SYNTH or VCO or RF2 or RF1 or DIG.

(2) JN5174: 160 kB, JN5178: 256 kB and JN5179: 512 kB.

Fig 2. Functional block diagram

8. Pinning information

8.1 Pinning



Transparent top view

Refer to Section 15.1 for important applications information regarding the connection of the paddle to the PCB.

Fig 3. Pin configuration

8.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO15	1	IO	DIO15 (I)	pull-down	**DIO15** — digital input/output 15
					PWM6 — PWM6 output
					JTAG_TDO — JTAG TDO data output
					SPIMOSI — SPI-bus master data output
					SPISEL1 — SPI-bus master select output 1
					TIM0CK_GT — Timer0 - clock gate input
					TRACESWV — ARM trace Serial Wire Viewer output
					SPISSEL — SPI-bus slave select input
DIO17	2	IO	at reset: DIO17 (I); during boot: SWCK (I)	pull-up	**DIO17** — digital input/output 17
					JTAG_TCK — JTAG TCK input
					SWCK — Serial Wire Debugger Clock input
					SPISEL0 — SPI-bus master select output 0
					TIM1CAP — Timer1 capture input
					COMP1P — comparator plus input
					SPISMISO — SPI-bus slave data output
DIO18	3	IO	DIO18 (I)	pull-up	**DIO18** — digital input/output 18
					JTAG_TMS — JTAG TMS input
					SWD — Serial Wire Debugger input
					SPIMISO — SPI-bus master data input
					TIM1OUT — Timer1 output
					COMP1M — comparator minus input
					SPISCLK — SPI-bus slave clock input
RESET_N	4	I		pull-up	**RESET_N** — reset input
XTAL_OUT	5	O		pull-up	**XTAL_OUT** — system crystal oscillator
XTAL_IN	6	I		pull-up	**XTAL_IN** — system crystal oscillator
VB_SYNTH	7	P			**VB_SYNTH** — regulated supply voltage
VB_VCO	8	P			**VB_VCO** — regulated supply voltage
V_{DDA}	9	P			**V_{DDA}** — analog supply voltage
IBIAS	10	I			**IBIAS** — bias current control
VREF/ADC1	11	I			**VREF** — analog peripheral reference voltage
					ADC1 — ADC input 1
VB_RF2	12	P; 1.8 V			**VB_RF2** — regulated supply voltage
RF_IO	13	IO			**RF_IO** — RF antenna
VB_RF1	14	P; 1.8 V			**VB_RF1** — regulated supply voltage
ADC0	15	I			**ADC0** — ADC input 0

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO0	16	IO	DIO0 (I)	pull-up	**DIO0** — digital input/output 0
					ADC4 — ADC input 4
					SPISEL0 — SPI-bus master select output 0
					RFRX — radio receiver control output
					FLICK_CTRL — flicker control output
					ADO — antenna diversity odd output
DIO1	17	IO	DIO1 (I)	pull-up	**DIO1** — digital input/output 1
					ADC3 — ADC input 3
					RFTX — radio transmitter control input
					PC0 — pulse counter 0 input
					ADE — antenna diversity even output
DIO2	18	IO	DIO2 (I)	pull-up	**DIO2** — digital input/output 2
					ADC5 — ADC input 5
					SDA — I^2C-bus master/slave SDA input/output (push-pull output)
					RXD1 — UART 1 receive data input
					TIM0CAP — Timer0 capture input
					RFRX — radios receiver control output
DIO3	19	IO	DIO3 (I)	pull-down	**DIO3** — digital input/output 3
					ADC2 — ADC input 2
					PWM4 — PWM4 output
					SCL — I^2C-bus master/slave SCL input/output (push-pull output)
					TXD1 — UART 1 transmit data output
					TIM0OUT — Timer0 output
					RFTX — radio transmit control input
					FLICK_CTRL — flicker control output
V_{SS}	20	G			**V_{SS}** — ground
DIO4	21	IO (open-drain)	DIO4 (I)	pull-up	**DIO4** — digital input/output 4
					SCL — I^2C-bus master/slave SCL input/output (open-drain)
					RXD0 — UART 0 receive data input
					TIM0CK_GT — Timer0 clock/gate input
					ADO — antenna diversity odd output

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO5	22	IO (open-drain)	DIO5 (I)	pull-up	**DIO5** — digital input/output 5
					SDA — I^2C-bus master/slave SDA input/output (open-drain)
					TXD0 — UART 0 transmit data output
					PC1 — pulse counter 1 input
					TIM0CAP — Timer0 capture input
					ADE — antenna diversity even output
DO0[2]	23	O	SPICLK (O)	pull-up	**DO0** — digital output 0
					SPICLK — SPI-bus master clock output
					ADE — antenna diversity even output
DO1[3]	24	IO	SPIMISO (I)	pull-up	**DO1** — digital output 1
					SPIMISO — SPI-bus master data input
					SPISMISO — SPI-bus slave data output
					ADO — antenna diversity odd output
DIO6[4]	25	IO	SPISEL0 (O)	pull-up	**DIO6** — digital input/output 6
					SPISEL0 — SPI-bus master select output 0
					CTS0 — UART 0 clear to send input
					RXD1 — UART 1 receive data input
					JTAG_TCK — JTAG TCK input
					SWCK — Serial Wire Debugger Clock input
					SPISCLK — SPI-bus slave clock input
					TIM1CAP — Timer1 capture input
DIO7[5]	26	IO	SPIMOSI (O)	pull-down	**DIO7** — digital input/output 7
					SPIMOSI — SPI-bus master data output
					JTAG_TDI — JTAG TDI data input
					SPISEL2 — SPI-bus master select output 2
					SPISSEL — SPI-bus slave select input
					CMP_OUT — comparator output
					32KIN — 32 kHz External clock input
					32KXTALOUT — 32 kHz clock output
DIO8	27	IO	DIO8 (I)	pull-down	**DIO8** — digital input/output 8
					PWM5 — PWM5 output
					TIM0OUT — Timer0 output
					TRACECLK — trace clock output
					32KXTALIN — 32 kHz clock input

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO9	28	IO	JTAG_TDO (O)/ TXD0 (O)	pull-up	**DIO9** — digital input/output 9
					JTAG_TDO — JTAG TDO data output
					TXD0 — UART 0 transmit data output
					TRACESWV — ARM trace serial wire viewer output
DIO10	29	IO	JTAG_TDI (I)/ RXD0 (I)	pull-up	**DIO10** — digital input/output 10
					JTAG_TDI — JTAG TDI data input
					RXD0 — UART 0 receive data input
V_{DDD}	30	P			**V_{DDD}** — digital supply voltage
i.c.	31	-			internally connected
n.c.	32	-			not connected
V_{SS}	33	G			**V_{SS}** — ground
n.c.	34	-			not connected
VB_DIG	35	P; 1.8 V			**VB_DIG** — regulated supply voltage
DIO11	36	IO	SWD (I)	pull-up	**DIO11** — digital input/output 11
					JTAG_TMS — JTAG TMS input
					SWD — serial wire debugger input
					RTS0 — UART 0 request to send output
					TXD1 — UART 1 transmit data output
					SPICLK — SPI-bus master clock output
					SPISMOSI — SPI-bus slave data input
					TIM1OUT — Timer1 output
					TRACED0 — ARM trace data0 output
DIO12	37	IO	DIO12 (I)	pull-down	**DIO12** — digital input/output 12
					PWM1 — PWM1 output
					TXD0 — UART 0 transmit data output
					TRACED3 — ARM trace data3 output
DIO13	38	IO	DIO13 (I)	pull-down	**DIO13** — digital input/output 13
					PWM2 — PWM2 output
					RXD0 — UART 0 receive data input
					PC0 — pulse counter 0 input
					TRACED2 — ARM trace data2 output
V_{SS}	39	G			**V_{SS}** — ground
DIO14	40	IO	DIO14 (I)	pull-down	**DIO14** — digital input/output 14
					PWM3 — PWM3 output
					PC1 — pulse counter 1 input
					CMP_OUT — comparator output
					TRACED1 — ARM trace data1 output
					SPISMOSI — SPI-bus slave data input
V_{SSA}	-	G	-	-	**V_{SSA}** — Exposed die paddle

[1] P = power supply; G = ground; I = input, O = output; IO = input/output.

[2] JTAG programming mode: must be left floating high during reset to avoid entering JTAG programming mode.

[3] UART programming mode: leave pin floating high during reset to avoid entering UART programming mode or hold it low to program.

[4] Specific precautions have to be followed for UART flow control: CTS0 is not usable in the same time with SPISEL0.

[5] Specific precautions have to be followed if external 32 kHz crystal is used. SPI-bus Flash can not be used in the same time than external 32 kHz crystal.

8.2.1 Power supplies

The V_{DDA} and V_{DDD} pins are decoupled with a 100 nF ceramic capacitor. V_{DDA} is the power supply to the analog circuitry; it should be decoupled to ground. V_{DDD} is the power supply for the digital circuitry; and should also be decoupled to ground. In addition, a common 10 μF tantalum capacitor is required to filter out low frequencies noise on the power supply pins. Decoupling pins for the internal 1.8 V regulators are provided which each requires a100 nF capacitor located as close to the device as practical. VB_SYNTH and VB_DIG require only a 100 nF capacitor. VB_RF1 and VB_RF2 should be connected together as close to the device as practical, and require one 100 nF capacitor and one 47 pF capacitor. The pin VB_VCO requires a 10 nF capacitor. Refer to Figure 55 for the schematic diagram.

V_{SSA} and V_{SS} are the ground pins.

Users are strongly discouraged from connecting their own circuits to the 1.8 V regulated supply pins, as the regulators have been optimized to supply only enough current for the internal circuits.

8.2.2 Reset

RESET_N is an active low reset input pin that is connected to an internal pull-up resistor see Table 19. It may be pulled low by an external circuit. Refer to Section 9.5.2 for more details.

8.2.3 32 MHz oscillator

A crystal is connected between XTAL_IN and XTAL_OUT to form the reference oscillator, which drives the system clock. A capacitor to analog ground is required on each of these pins. Refer to Section 9.4.1 for more details. The 32 MHz reference frequency is divided down to 16 MHz and this is used as the system clock throughout the device.

8.2.4 Radio

The radio is a single ended design, requiring only a capacitor and just 2 inductors to match a 50 Ω microstrip line to the RF_IO pin. In addition, extra-components are added on the line for filtering purpose.

An external resistor (43 kΩ) is required between IBIAS and analog ground (paddle) to set various bias currents and references within the radio.

8.2.5 Analog peripherals

The ADC requires a reference voltage to use as part of its operation. It can use either an internal reference voltage or an external reference connected to VREF. This voltage is referenced to analog ground and the performance of the analog peripherals is dependent on the quality of this reference.

There are 6 ADC inputs and a pair of comparator inputs. ADC0 has a designated input pin but ADC1 uses the same pin as VREF, invalidating its use as an ADC pin when an external reference voltage is required. The remaining 4 ADC channels are shared with the digital IOs DIO0, DIO1, DIO2 and DIO3. When these 4 ADC channels are selected, the corresponding DIOs must be configured as inputs with their pull-ups disabled. Similarly, the comparator shares pins 2 and 3 with DIO17 and DIO18, so when the comparator is selected these pins must be configured as inputs with their pull-ups disabled. The analog IO pins on the JN517x can have signals applied up to 0.3 V higher than V_{DDA}. A schematic view of the analog IO cell is shown in Figure 4. Figure 5 demonstrates a special case, where a digital IO pin doubles as an input to analog devices. This applies to ADC2, ADC3, ADC4, ADC5, COMP1P and COMP1M.

In reset, sleep and deep sleep, the analog peripherals are all OFF. In sleep, the comparator may optionally be used as a wake-up source.

On platform with higher power (e.g. light Bulb, Smart Plug), unused ADC and comparator inputs should not be left unconnected, but connected to analog ground.

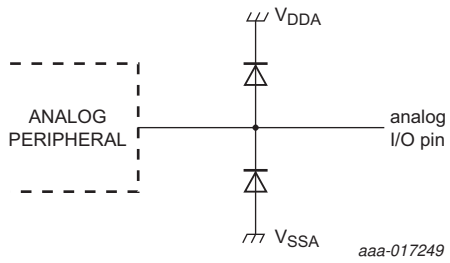


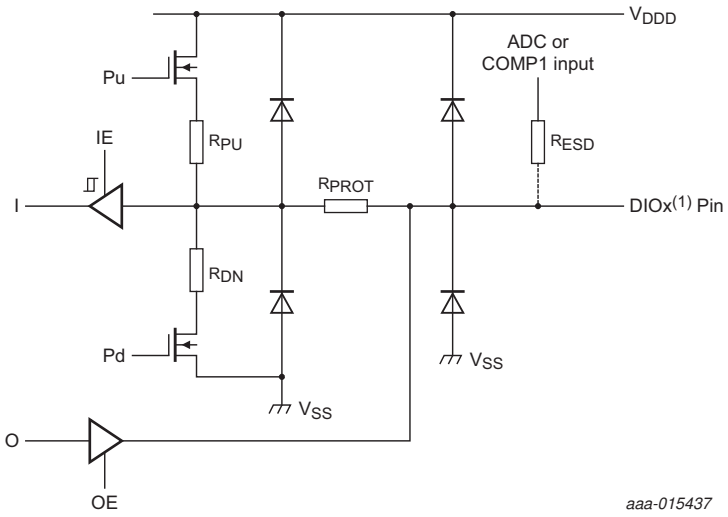
Fig 4. Analog IO cell

8.2.6 Digital Input Output (DIO)

When used in their primary function, all DIO pins are bidirectional and are connected to weak internal pull-up or pull-down resistors (50 kΩ nominal) that can be disabled. When used in their secondary function (selected when the appropriate peripheral block is enabled through software library calls), their direction is fixed by the function. The pull-up or pull-down resistor is enabled or disabled independently of the function and direction; the default state from reset is enabled.

A schematic view of the DIO cell is in Figure 5. The dotted lines through resistor R_{ESD} represent a path that exists only on DIO0, DIO1, DIO2, DIO3, DIO17 and DIO18 which are also inputs to the ADC (ADC2, ADC3, ADC4, ADC5) and comparator (COMP1P, COMP1M) respectively. To use these DIO pins for their analog functions, the DIO must be set as an input with its pull-up resistor, R_{PU}, disabled.

The DIO4 and DIO5 are different from other DIOs, as these have DIO and I^2C-bus mode. In I^2C-bus mode, DIO4 and DIO5 are true open-drain with “in-built” glitch filter enabled. A schematic view of DIO4 and DIO5 cells is shown in Figure 6.



(1) With x = 0, 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 17 or 18.

Fig 5. DIO (other than DIO4 and DIO5) pin equivalent schematic

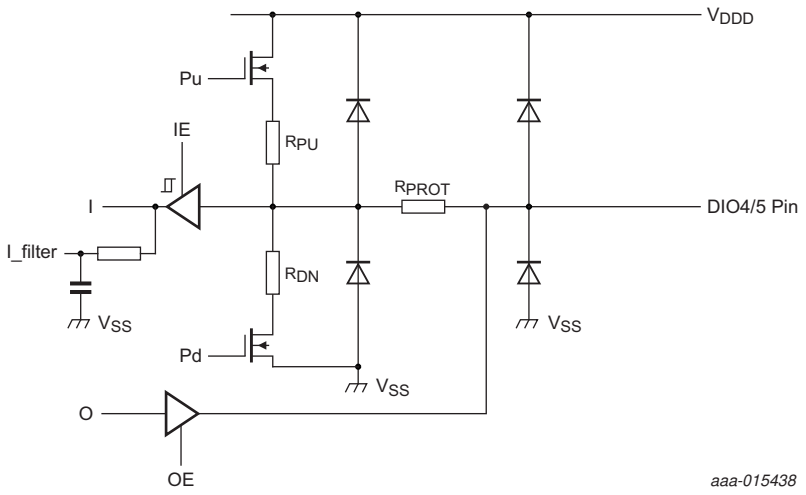


Fig 6. DIO4 and DIO5 pin equivalent schematic

In reset, the digital peripherals are all OFF and the DIO pins are set as high-impedance inputs. During sleep and deep sleep, the DIO pins retain both their input/output state and output level that was set as sleep commences. If the DIO pins were enabled as inputs and the interrupts were enabled, then these pins may be used to wake up the JN517x from sleep or deep sleep.

9. Functional description

9.1 CPU

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware divide, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-CODE bus, and the D-CODE bus. The I-CODE and D-CODE core buses are faster than the system bus and are used similarly to TCM interfaces: one bus dedicated for instruction fetch (I-CODE) and one bus for data access (D-CODE). The use of 2 core buses allows for simultaneous operations if concurrent operations target different devices.

The JN517x uses a multi-layer AHB matrix to connect the ARM Cortex-M3 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

The ARM Cortex-M3 processor is described in detail in the Cortex-M3 Technical Reference Manual that can be found on the official ARM website.

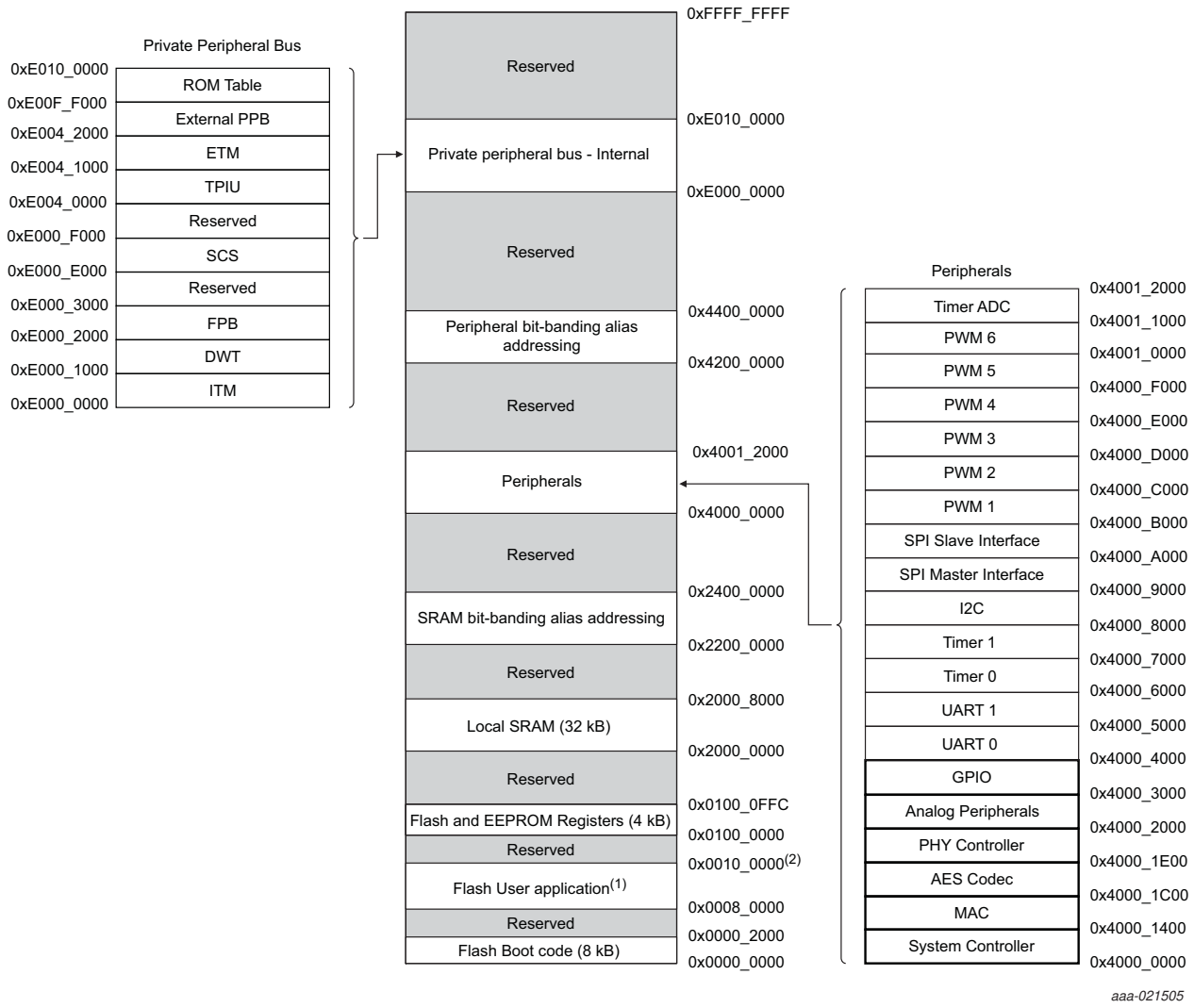
To improve power consumption a number of power-saving modes are implemented in the JN517x, described more fully in Section 10. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on receiving an interrupt it will wake up to service the request. Additionally, it is possible under software control, to set the speed of the CPU to 1 MHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz or 32 MHz. This feature can be used to trade off processing power against current consumption.

9.2 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to 8 breakpoints and 4 watch points.

9.3 Memory organization

This section describes the different memories found within the JN517x. The device contains Flash, RAM, and EEPROM memory, the wireless transceiver and peripherals registers all within the same linear address space.



(1) JN5174: 160 kB, JN5178: 256 kB and JN5179: 512 kB.

(2) JN5174: 0x000A_8000, JN5178: 0x000C_0000 and JN5179: 0x0010_0000.

Fig 7. JN517x memory map

9.3.1 Flash

The embedded Flash consists of 2 parts: an 8 kB region used for holding boot code, and a 160 kB or 256 kB or 512 kB region used for application code. The sector size of the application code is always 32 kB, for any size of Flash memory. The guaranteed endurance of the memory is 10,000 write cycles with typical endurance of 100,000 cycles, while the data retention is guaranteed for at least 10 years. The boot code region is pre-programmed by NXP on supplied parts, and contains code to handle reset, interrupts and other events (see section Section 9.6). It also contains a Flash Programming Interface to allow interaction with the PC-based Flash Programming Utility which allows user code compiled using the supplied SDK to be programmed into the application space. The memory can be erased by a single or multiple sectors and written to in units of 256 bytes, known as pagewords. For further information, refer to Flash Programmer User Guide JN-UG-3099 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.3.2 RAM

The JN517x devices contain 32 kB of high-speed RAM. It is primarily used to hold the CPU Stack together with program variables and data. If necessary, the CPU can execute code contained within the RAM (although it would normally just execute code directly from the embedded Flash). Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are unpowered, allowing a quicker resumption of processing once woken.

9.3.3 OTP configuration memory

The JN517x contains a quantity of One Time Programmable (OTP) memory as part of the embedded Flash (Index Sector). This can be used to securely hold such things as a user 64-bit MAC address and a 128-bit AES security key. By default the 64-bit MAC address is pre-programmed by NXP on supplied parts; however the pre-programmed value can be overridden by customers providing their own MAC addresses. The user MAC address and other data can be written to the OTP memory using the Flash programmer. Details on how to obtain and install MAC addresses can be found in the dedicated Application Note. In addition, 128 bits are available for customer use for storage of configuration or other information.

For further information on how to program and use this facility, refer to Flash Programmer User Guide JN-UG-3099 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.3.4 EEPROM

The JN517x contains 4 kB of EEPROM. The guaranteed endurance of the memory is 100 000 write cycles with typical endurance of 1 million cycles, while the data retention is guaranteed for at least 10 years. EEPROM endurance can be extended using the Persistent Data Manager software which wear levels the EEPROM as data is written to it. This is supplied in the NXP ZigBee SDK.

This non-volatile memory is primarily used to hold persistent data generated from such things as the Network Stack software component (for example network topology, routing tables). As the EEPROM holds its contents through sleep and reset events, this means more stable operation and faster recovery is possible after outages.

The memory can be erased by a single or multiple pages of 64 bytes. It can be written to in single or multiple bytes up to 64 bytes. For further details, refer to the JN517x Integrated Peripherals API User Guide JN-UG-3118 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.3.5 External memory

An optional external serial non-volatile memory (for instance Flash or EEPROM) with a SPI-bus interface may be used to provide additional storage for program code, such as a new code image or further data for the device when external power is removed. The memory can be connected to the SPI-bus master interface using select line SPISEL0 (see Figure 8 for details).

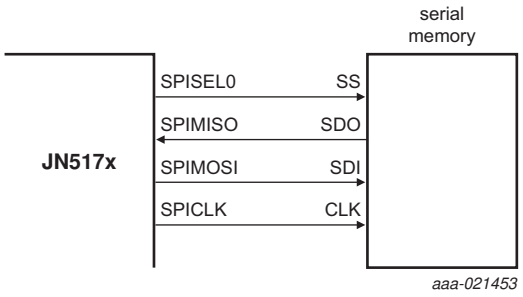


Fig 8. Connecting external serial memory

The contents of the external serial memory may be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in the Flash memory index section. When bootloading program code from external serial memory, the JN517x automatically accesses the encryption key to execute the decryption process, which is transparent to the user, user program code does not need to handle any part of the decryption process; it is transparent. For more details, including the how the program code encrypts data for the external memory, refer to Application Note Boot loader Operation JN-AN-1003 on the Wireless Connectivity area of the NXP web site Ref. 2.

Remark: SPI-bus Flash can not be used in the same time than external 32 kHz crystal.

9.3.6 Peripherals

All peripherals have their registers mapped into the memory space. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see JN517x Integrated Peripherals API User Guide JN-UG-3118 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.4 System clocks

Two system clocks are used to drive the on-chip subsystems of the JN517x. The wake-up timers are driven from a low frequency clock (notionally 32 kHz). All other subsystems (transceiver, processor, memory and digital and analog peripherals) are driven by a high-speed clock (notionally 32 MHz), or a divided-down version of it.

The high-speed clock is either generated by the accurate crystal-controlled oscillator (32 MHz) or the less accurate high-speed RC oscillator (27 MHz to 32 MHz calibrated). The low-speed clock is either generated by the less accurate RC oscillator (centered on 32 kHz) or can be supplied externally.

9.4.1 High-speed (32 MHz) system clock

The selected high-speed system clock is used directly by the radio subsystem, whereas a divided-by-two version is used by the remainder of the transceiver and the digital and analog peripherals. The direct or divided down version of the clock is used to drive the processor and memories (32 MHz, 16 MHz, 8 MHz, 4 MHz, 2 MHz or 1 MHz).

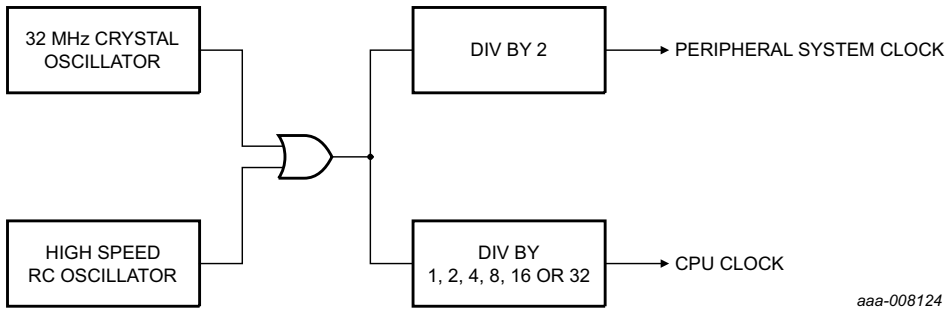


Fig 9. System and CPU clocks

Crystal oscillators are generally slow to start. Hence to provide a fast start-up following a sleep cycle or reset, the fast RC oscillator is always used as the initial source for the high-speed system clock. The oscillator starts very quickly and will run at 25 MHz to 32 MHz (uncalibrated) or 32 MHz ±5 % (calibrated). Although this means that the system clock will be running at an undefined frequency (slightly slower or faster than nominal), this does not prevent the CPU and memory subsystems operating normally, so the program code can execute. However, it is not possible to use the radio or UARTs, as even after calibration (initiated by the user software calling an API function) there is still a ±5 % tolerance in the clock rate over voltage and temperature. Other digital peripherals can be used (eg SPI-bus master/slave), but care must be taken if using Timers due to the clock frequency inaccuracy.

Further details of the high-speed RC oscillator can be found in Section 14.3.9

On wake-up from sleep, the JN517x uses the fast RC oscillator. It can then either:

- Automatically switch over to use the 32 MHz clock source when it has started up
- Continue to use the fast RC oscillator until software triggers the switch-over to the 32 MHz clock source, for example when the radio is required
- Continue to use the RC oscillator until the device goes back into one of the sleep modes

The use of the fast RC Oscillator at wake-up means that there is no need to wait for the 32 MHz crystal oscillator to stabilize.

9.4.1.1 32 MHz crystal oscillator

The JN517x contains the necessary on chip components to build a 32 MHz reference oscillator with the addition of an external crystal resonator and 2 tuning capacitors. The schematics of these components are shown in Figure 10. The 2 capacitors, C1 and C2, should typically be 12 pF and use a COG dielectric. Due to the small size of these capacitors, it is important to keep the traces to the external components as short as possible. The on-chip transconductance amplifier is compensated for temperature variation, and is self-biasing by means of the internal resistor R1. This oscillator provides the frequency reference for the radio and therefore the reference PCB layout and BOM must be carefully followed. Refer to Section 14.3.11 for development support with the crystal oscillator circuit. The oscillator includes a function which flags when the amplitude of oscillation has reached a satisfactory level for full operation, and this is checked before the source of the high-speed system clock is changed to the 32 MHz crystal oscillator.

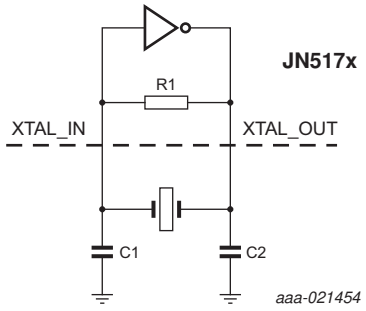


Fig 10. 32 MHz crystal oscillator connections

For operation over the extended temperature range, 85 °C to 125 °C, special care is required; this is because the temperature characteristics of crystal resonators are generally in excess of ±40 ppm frequency tolerance defined by the IEEE802.15.4 standard. The oscillator cell contains additional circuitry to compensate for the poor performance of the crystal resonators above 100 °C. Full details, including the software API function, can be found in the Temperature Dependent Operating Guidelines JN-AN-1186 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.4.1.2 High-speed RC oscillator

An on-chip high-speed RC oscillator is provided in addition to the 32 MHz crystal oscillator for 2 purposes, to allow a fast start-up from reset or sleep and to provide a lower current alternative to the crystal oscillator for non-timing critical applications. By default the oscillator will run at 27 MHz typically with a wide tolerance. It can be calibrated, using a software API function, which will result in a nominal frequency of 32 MHz with a ±1.6 % tolerance at 3 V and 25 °C. However, it should be noted that over the full operating range of voltage and temperature this will increase to ±5%. The calibration information is retained through speed cycles and when the oscillator is disabled, so typically the calibration function only needs to be called once. No external components are required for this oscillator. The electrical specification of the oscillator can be found in Section 14.3.9.

9.4.2 Low-speed (32 kHz) system clock

The 32 kHz system clock is used for timing the length of a sleep period (see Section 10. The clock can be selected from one of 2 sources through the application software:

- 32 kHz RC oscillator
- 32 kHz external clock
- 32 kHz crystal oscillator

Upon a chip reset or power-up, the JN517x defaults to using the internal 32 kHz RC oscillator. If another clock source is selected, then, it will remain in use for all 32 kHz timing until a chip reset is performed.

9.4.2.1 32 kHz RC oscillator

The internal 32 kHz RC oscillator requires no external components. The internal timing components of the oscillator have a wide tolerance due to manufacturing process variation and so the oscillator runs nominally at 32 kHz −20.7 %/+52.6 %. To make this useful as a timing source for accurate wake-up from sleep, a frequency calibration factor derived from the more accurate 16 MHz peripheral system clock may be applied. The

calibration factor is derived through software, details can be found in Section 9.10.3.1. Software must check that the 32 kHz RC oscillator is running before using it. The oscillator has a default current consumption of around 0.5 μA. Optionally, this can be reduced to 0.375 μA, however, the calibrated accuracy and temperature coefficient will be worse as a consequence. For detailed electrical specifications, see Section 14.3.9.

9.4.2.2 32 kHz External clock

An externally supplied 32 kHz reference clock on the 32KIN input (DIO7) may be provided to the JN517x. This would allow the 32 kHz system clock to be sourced from a very stable external oscillator module, allowing more accurate sleep cycle timings compared to the internal RC oscillator. SPI-bus Flash can not be used in the same time than external 32 kHz crystal.

9.4.2.3 32 kHz crystal oscillator

In order to obtain more accurate sleep periods, the JN517x contains the necessary on-chip components to build a 32 kHz oscillator with the addition of an external 32.768 kHz crystal and two tuning capacitors. The crystal should be connected between 32KXTALIN and 32KXTALOUT (DIO8 and DIO7), with two equal capacitors to ground, one on each pin. Due to the small size of the capacitors, it is important to keep the traces to the external components as short as possible.

The electrical specification of the oscillator can be found in Section 14.3.10. The oscillator cell is flexible and can operate with a range of commonly available 32.768 kHz crystals with load capacitances from 6 pF to 12.5 pF. However, the maximum ESR of the crystal and the supply current are both functions of the actual crystal used.

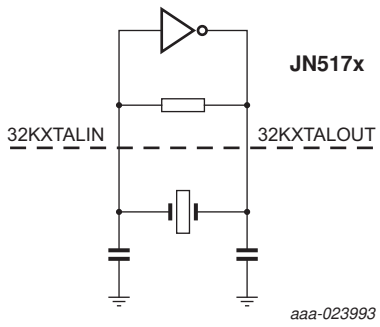


Fig 11. 32 kHz crystal oscillator connections

9.5 Reset

A system reset initializes the device to a pre-defined state and forces the CPU to start program execution from the reset vector. The reset process that the JN517x goes through is as follows.

When power is first applied (on V_{DDA} and V_{DDD} supply pins) or when the external reset is released, the high-speed RC oscillator and 32 MHz crystal oscillator are activated. After a short wait period (approximately 13 μs) while the high-speed RC starts up, and so long as the supply voltage satisfies the default SVM threshold (2.0 V + 0.045 V hysteresis), the internal 1.8 V regulators are turned on to power the processor and peripheral logic. The regulators are allowed to stabilize (about 15 μs) followed by a further wait (approximately

150 µs) to allow the Flash and EEPROM bandgaps to stabilize and allow their initialization, including reading the user SVM threshold from the Flash. This is applied to the SVM, and after a brief pause (approximately 2.5 µs) the SVM is checked again. If the supply is above the new SVM threshold, the CPU and peripheral logic is released from reset and the CPU starts to run code beginning at the reset vector. This runs the bootloader code contained within the Flash, which looks for a valid application to run, first from the internal Flash and then from any connected external serial memory over the SPI-bus master interface. Once found, required variables are initialized in RAM before the application is called at its AppColdStart entry point. For more details on the bootloader, refer to Application Note Boot loader Operation JN-AN-1003 on the Wireless Connectivity area of the NXP web site Ref. 2.

The JN517x has 5 sources of reset:

- Internal Power-On Reset/Brown-Out Reset (BOR)
- External reset
- Software reset
- Watchdog timer
- Supply voltage detect

Remark: When the device exits a reset condition, device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, then the device must be held in reset until the operating conditions are met (see Section 14.3.1).

9.5.1 Internal Power-On Reset/Brown-out Reset (BOR)

For most applications, the Internal POR is capable of generating the required reset signal. When power is applied to the device, the power-on reset circuit monitors the rise of the V_{DD} (V_{DDA} and V_{DDD}) supply. When the V_{DD} reaches the specified threshold, the reset signal is generated. This signal is held internally until the power supply and oscillator stabilization time has elapsed, when the internal reset signal is then removed and the CPU is allowed to run.

The BOR circuit has the ability to reject spikes on the V_{DD} rail to avoid false triggering of the reset module. Typically for a negative going square pulse of duration 1 µs, the voltage must fall to 1.2 V before a reset is generated. Similarly for a triangular wave pulse of 10 µs width, the voltage must fall to 1.3 V before causing a reset. The exact characteristics are complex and these are only examples. See Figure 47 for more details on BOR and SVM characteristics.

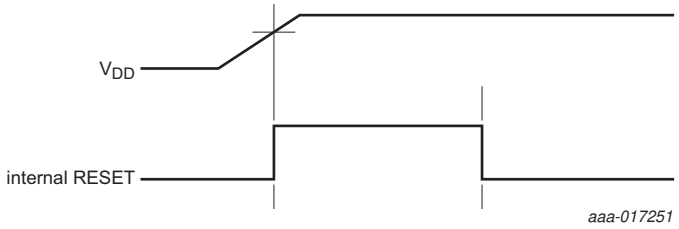


Fig 12. Internal Power-On Reset

When the supply drops below the POR 'falling' threshold, it will retrigger the reset. On platform with higher power (e.g. light bulb, smart plug) it is recommended to use this external circuit to avoid unexpected reset due to spurs.

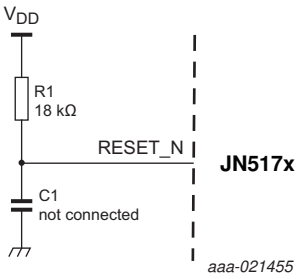


Fig 13. External reset generation

9.5.2 External reset

An external reset is generated by a low level on the RESET_N pin. Reset pulses longer than the minimum pulse width will generate a reset during active or sleep modes. Shorter pulses are not guaranteed to generate a reset. The JN517x is held in reset while the RESET_N pin is low. When the applied signal reaches the reset threshold voltage (V_{rst}) on its positive edge, the internal reset process starts.

The JN517x has an internal pull-up resistor (see Table 19) connect to the RESET_N pin. The pin is an input for an external reset only. By holding the RESET_N pin low, the JN517x is held in reset, resulting in a typical current of 6 μA.

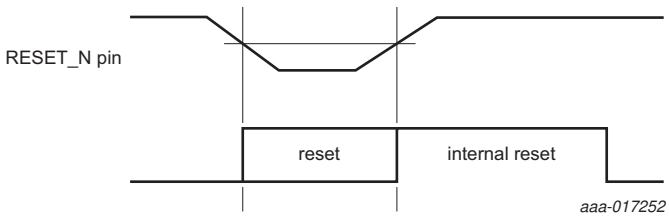


Fig 14. External reset

9.5.3 Software reset

A system reset can be triggered at any time through software control, causing a full chip reset and invalidating the RAM contents. For example, this can be executed within a user's application upon detection of a system failure.

9.5.4 Supply Voltage Monitor

An internal SVM is used to monitor the supply voltage to the JN517x; this can be used while the device is awake or is in CPU doze mode. Dips in the supply voltage below a variable threshold can be detected and can be used to cause the JN517x to perform a chip reset. Equally, dips in the supply voltage can be detected and used to cause an interrupt to the processor, when the voltage either drops below the threshold or rises above it.

The supply voltage detect is enabled by default from power-up and can extend the reset during power-up. This will keep the CPU in reset until the voltage exceeds the SVM threshold voltage. The threshold voltage is configurable to 1.95 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.7 V and 3.0 V and is controllable by software. From power-up, the threshold is set by a setting within the Flash and the default chip configuration is for the 2.0 V threshold. It is expected that the threshold is set to the minimum needed by the system. See Figure 47 for more details on BOR and SVM characteristics.

9.5.5 Watchdog timer

A watchdog timer is provided to guard against software lockups. It operates by counting cycles of the high-speed RC system clock. A pre-scaler is provided to allow the expiry period to be set between typically 8 ms and 16.4 s (dependent on high-speed RC accuracy: +30 %, −15 %). Failure to restart the watchdog timer within the pre-configured timer period will cause a chip reset to be performed. A status bit is set if the watchdog was triggered so that the software can differentiate watchdog initiated resets from other resets, and can perform any required recovery once it restarts. Optionally, the watchdog can cause an exception rather than a reset, this preserves the state of the memory and is useful for debugging.

After power-up, reset, start from deep sleep or start from sleep, the watchdog is always enabled with the largest time-out period and will commence counting as if it had just been restarted. Under software control, the watchdog can be disabled. If it is enabled, the user must regularly restart the watchdog timer to stop it from expiring and causing a reset. The watchdog runs continuously, even during doze, however the watchdog does not operate during sleep or deep sleep, or when the hardware debugger has taken control of the CPU. It will recommence automatically if enabled once the debugger unstalls the CPU.

9.6 Nested Vector Interrupt controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late-arriving interrupts. The main features of the interrupt controller are:

- Controls the system exceptions and peripheral interrupts
- Supports 20 vectored interrupts
- 16 programmable interrupt priority levels

Interrupts can be used to wake the JN517x from sleep or deep sleep. The peripherals, baseband controller, security coprocessor and NVIC are powered down during sleep or deep sleep but the DIO interrupts and optionally the pulse counters, wake-up timers and analog comparator interrupts remain powered to bring the JN517x out of sleep.

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register (VTOR) contained in the Cortex-M3. The NVIC is described in detail in the Cortex-M3 Technical Reference Manual that can be found on official ARM website.

9.6.1 Interrupts sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Table 3 lists the interrupt sources for each peripheral function. Exception numbers relate to where entries are stored in the exception vector table. Interrupt numbers are used in some other contexts, such as software interrupts.

Table 3. Interrupt sources

Interrupt ID	Exception number	Vector offset (h)	Function
0	16	0x40	PWM1
1	17	0x44	PWM2
2	18	0x48	PWM3
3	19	0x4C	PWM4
4	20	0x50	PWM5
5	21	0x54	PWM6
6	22	0x58	system controller
7	23	0x5C	MAC
8	24	0x60	AES codec
9	25	0x64	PHY controller
10	26	0x68	UART0
11	27	0x6C	UART1
12	28	0x70	SPI-bus slave
13	29	0x74	SPI-bus master
14	30	0x78	I^2C-bus master/slave
15	31	0x7C	Timer0
16	32	0x80	Timer1
17	33	0x84	timer ADC
18	34	0x88	analog peripheral
19	35	0x8C	watchdog interrupt

9.7 Wireless transceiver

The wireless transceiver comprises a 2.45 GHz radio, modem, a baseband processor, a security coprocessor and PHY controller. These blocks, with protocol software provided as a library, implement an IEEE802.15.4 standards-based wireless transceiver that transmits and receives data OTA in the unlicensed 2.4 GHz band.

9.7.1 Radio

Figure 15 shows the single-ended radio architecture.