Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Numonyx™ Axcell™ M29EW Datasheet

256-Mbit, 512-Mbit, 1-Gbit, 2-Gbit (x8/x16, uniform block)
3 V supply flash memory

Features

- Supply voltage
  - — V_{CC} = 2.7 to 3.6 V for Program, Erase and Read
  - — V_{CCQ} = 1.65 to 3.6 V for I/O buffers
- Asynchronous Random/Page Read
  - — Page size: 16 words or 32 bytes
  - — Page access: 25 ns
  - — Random access: 100ns (Fortified BGA); 110 ns (TSOP)
- Buffer Program
  - — 512-word program buffer
- Programming time
  - — 0.88 µs per byte (1.14MB/s) typical when using full buffer size in buffer program
- Memory organization
  - — Uniform blocks, 128 Kbytes/64 Kwords each
- Program/Erase controller
  - — Embedded byte/word program algorithms
- Program/ Erase Suspend and Resume
  - — Read from any block during Program Suspend
  - — Read and Program another block during Erase Suspend
- Blank Check to verify an erased block
- Unlock Bypass/Block Erase/Chip Erase/Write to Buffer
  - — Faster Buffered/Batch Programming
  - — Faster Block and Chip Erase
- Vpp/WP# pin protection
  - — Protects first or last block regardless of block protection settings
- Software protection
  - — Volatile Protection
  - — Non-Volatile Protection
  - — Password Protection
  - — Password Access
- Extended Memory block
  - — 128-word/256-byte block for permanent, secure identification.
  - — can be programmed and locked by factory or by the customer
- Low power consumption
  - — Standby
- Minimum 100,000 Program/Erase cycles per block
- ETOX™* X (65nm) MLC technology
- Fortified BGA and TSOP packages
- JESD47E Compliant
- Green packages available
  - — RoHS Compliant
  - — Halogen Free

1 Description

The Numonyx™ Axcell™ M29EW flash memory based on 65nm MLC technology is the world's leading line of parallel NOR flash for embedded applications. It can be read, erased and reprogrammed; and these operations can be performed using a single low voltage (2.7 to 3.6 V) supply. Upon power-up, the memory defaults to its array read mode.

The main memory array is divided into 64-Kword/128-Kbyte uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. Program and Erase commands are written to the command interface of the memory. An on-chip Program/Erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error condition can be identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The M29EW supports Asynchronous Random Read and Page Read from all blocks of the memory array. It also features an internal program buffer which improves throughput by programming 512 words via one command sequence.

The M29EW contains a 128-word Extended Memory Block which overlaps addresses with array block 0. The user can program this additional space; then protect it to permanently secure its contents.

The device features different levels of hardware and software protection to secure blocks from unwanted modification (program or erase):

- Hardware protection:
  - The V_{PP}/WP# provides a hardware protection of either the highest (M29EWH) or the lowest (M29EWL) block of the main memory array.
- Software protection:
  - Volatile Protection
  - Non-Volatile Protection
  - Password Protection
  - Password Access

The M29EW is offered in TSOP56 (14 x 20 mm) and Fortified BGA64 (11 x 13 mm, 1 mm pitch) packages.

The memories are delivered with all the bits erased (set to '1').

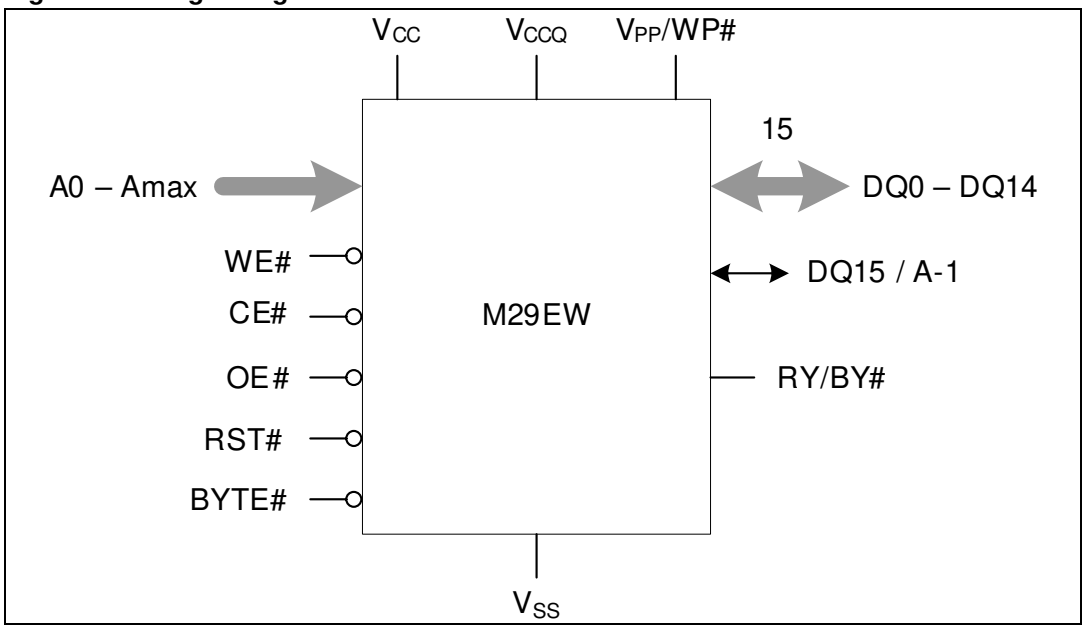
Also see *Appendix B: Common Flash Interface (CFI) on page 112* and *Table 5: Block addresses on page 12* for a full list of the block addresses.

Table 1. Signal Descriptions

Name	Description	Direction
A0-Amax	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15/A–1	Data input/output or address input	I/O
CE#	Chip Enable	Input
OE#	Output Enable	Input
WE#	Write Enable	Input
RST#	Reset	Input
RY/BY#	Ready/Busy output	Output
BYTE#	Byte/word organization select	Input
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
V_{PP}/WP#(1)	V_{PP}/Write Protect	Input
V_{SS}	Ground	-
NC	Not connected	-

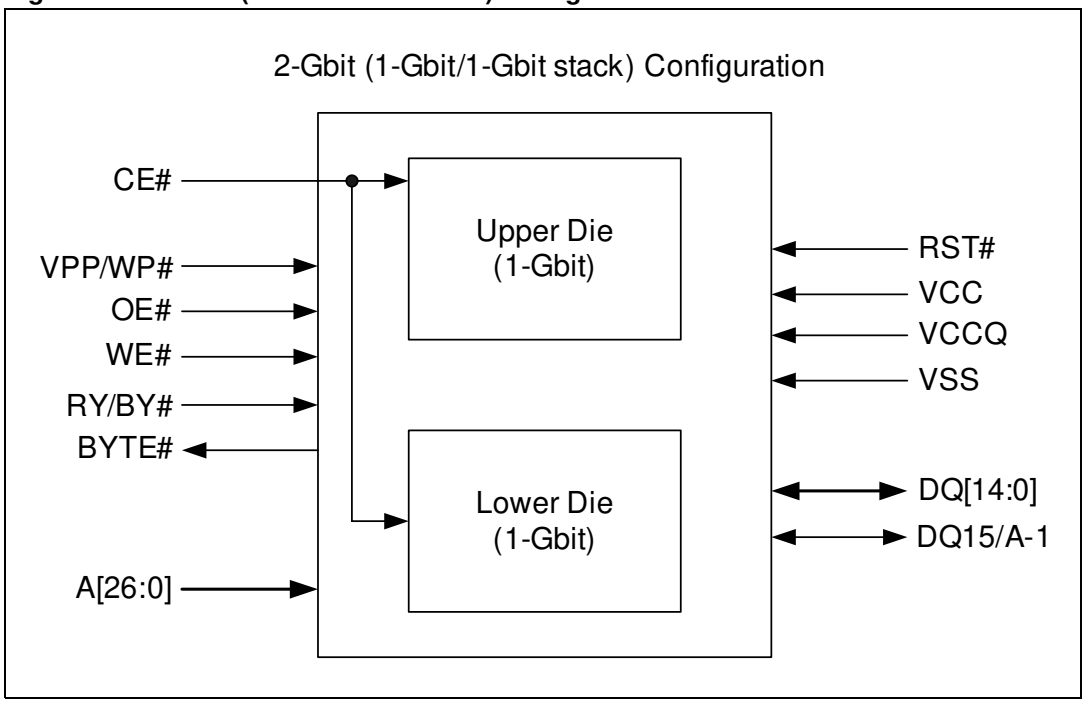
1. V_{PP}/WP# may be left unconnected as it is internally connected to a pull-up resistor, which enables Program/Erase operations.

Figure 1. Logic diagram



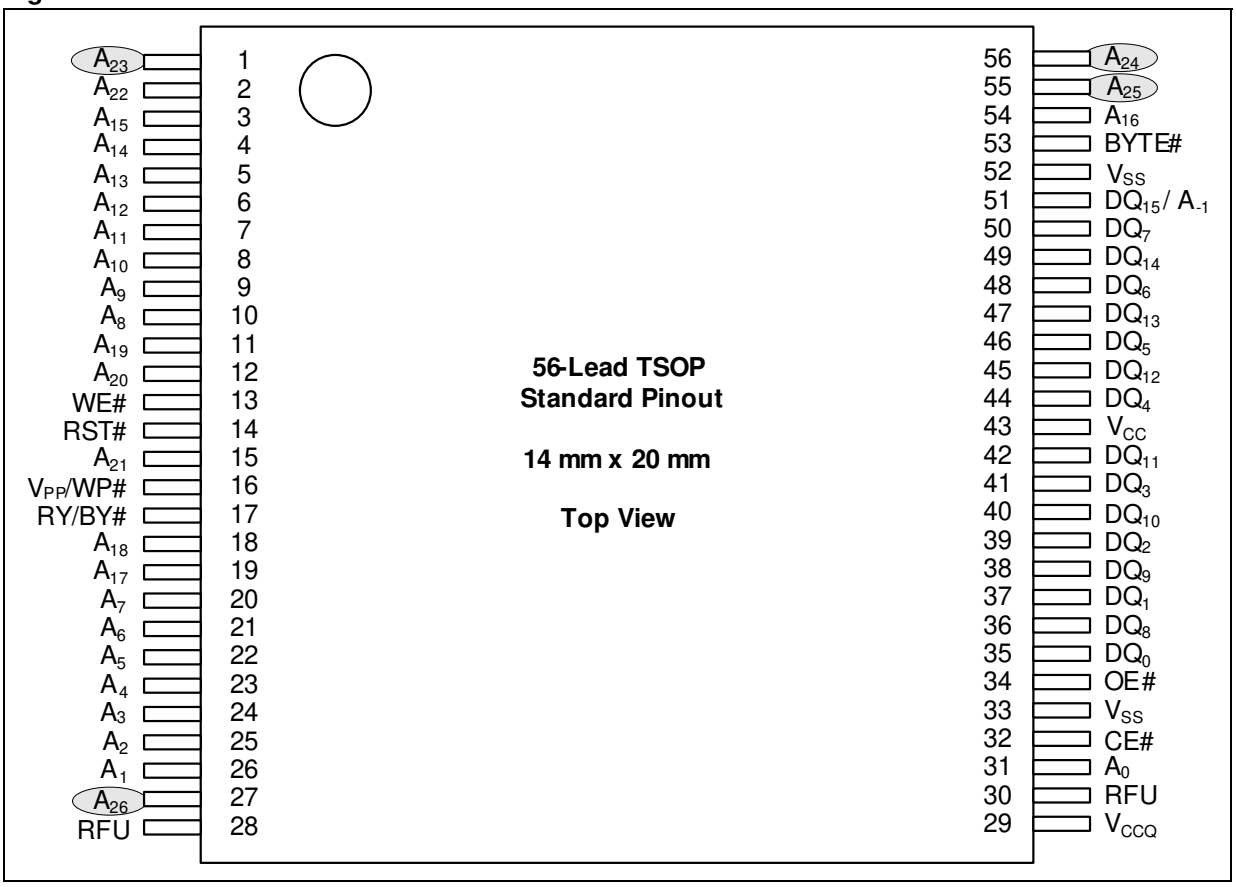
1. A23 is valid for 256-Mbit density and above; otherwise, it is RFU.
2. A24 is valid for 512-Mbit density and above; otherwise, it is RFU.
3. A25 is valid for 1-Gbit density and above; otherwise, it is RFU.
4. A26 is valid for 2-Gbit (1-Gbit/1-Gbit stack) density only; otherwise it's RFU.
5. RFU stands for Reserved for Future Use and should be not connect.

Figure 2. 2-Gbit (1-Gbit/1-Gbit stack) configurations



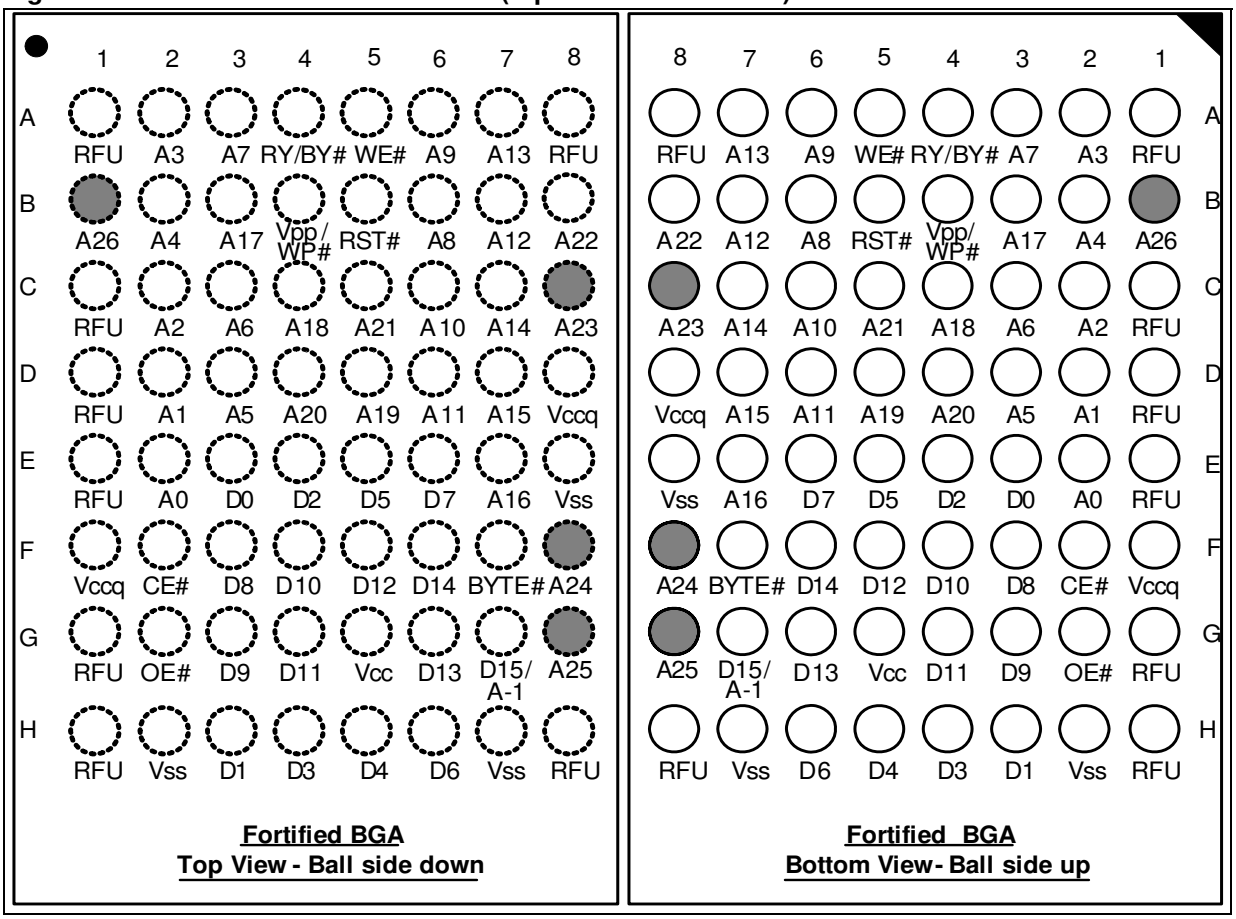
1. $A_{max} = V_{IH}$ selects the Upper Die; $A_{max} = V_{IL}$ selects the Lower Die.

Figure 3. TSOP connections



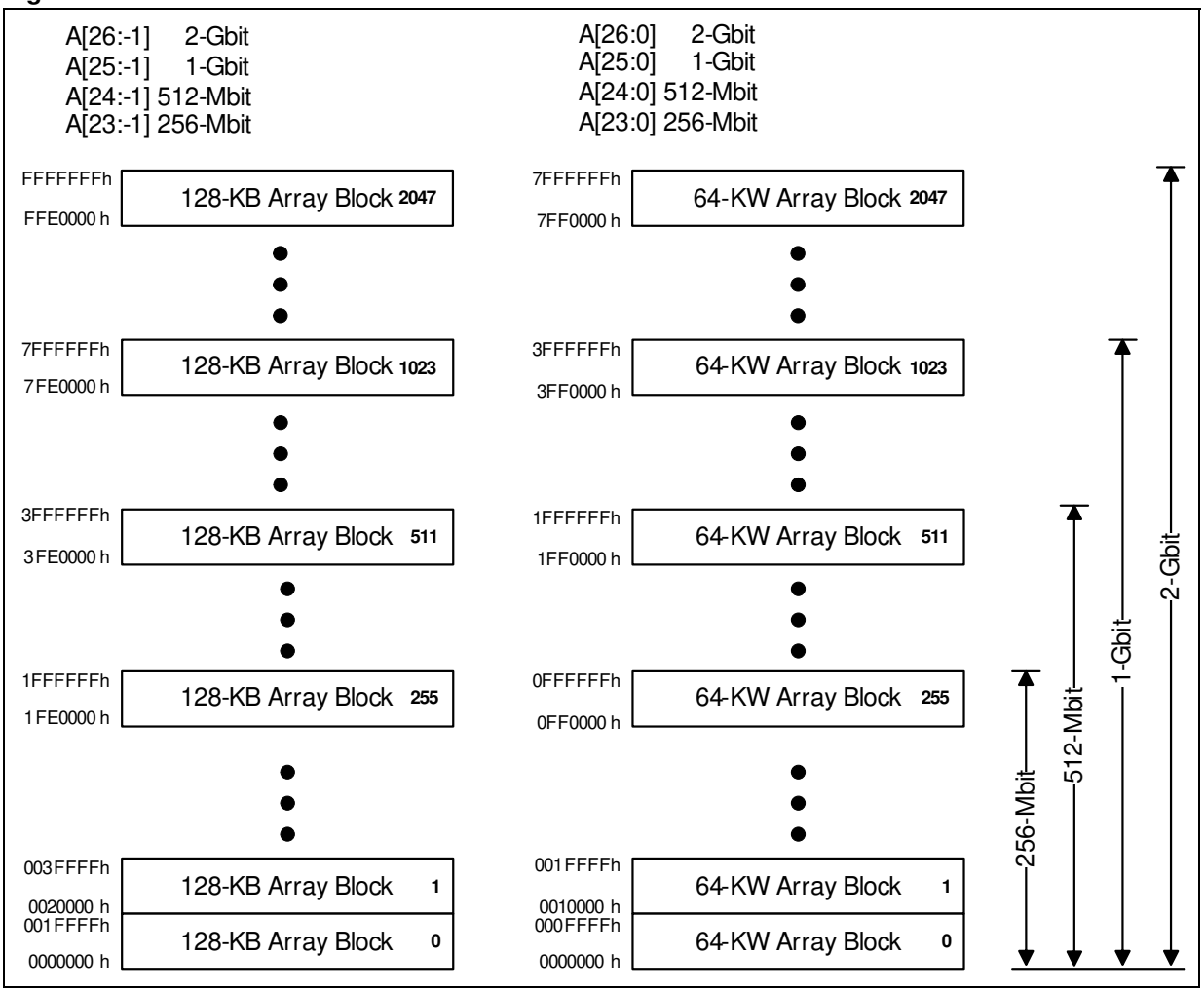
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256-Mbit density and above; otherwise, it is RFU.
3. A24 is valid for 512-Mbit density and above; otherwise, it is RFU.
4. A25 is valid for 1-Gbit density and above; otherwise, it is RFU.
5. A26 is valid for 2-Gbit (1-Gbit/1-Gbit stack) density only; otherwise it's RFU.
6. RFU stands for Reserved for Future Use and should be not connect.

Figure 4. Fortified BGA connections (top and bottom views)



1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256-Mbit density and above; otherwise, it is RFU.
3. A24 is valid for 512-Mbit density and above; otherwise, it is RFU.
4. A25 is valid for 1-Gbit density and above; otherwise, it is RFU.
5. A26 is valid for 2-Gbit (1-Gbit/1-Gbit stack) density only; otherwise it's RFU.
6. RFU stands for Reserved for Future Use and should be not connect.

Figure 5. Block addresses



2 Signal Descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal Descriptions*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-Amax)

The Address inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the command interface of the Program/Erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the command interface of the internal state machine.

2.3 Data inputs/outputs (DQ8-DQ14)

The Data I/O outputs the data stored at the selected address during a Bus Read operation when BYTE# is High, V_{IH}. When BYTE# is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

2.4 Data input/output or address input (DQ15/A–1)

When the device operates in x16 bus mode, this pin behaves as a Data input/output pin, together with DQ8-DQ14. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Throughout the text consider references to the Data input/output to include this pin when the device operates in x16 bus mode and references to the Address inputs to include this pin when the device operates in x8 bus mode except when stated explicitly otherwise.

2.5 Chip Enable (CE#)

The Chip Enable pin, CE#, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

2.6 Output Enable (OE#)

The Output Enable pin, OE#, controls the Bus Read operation of the memory.

2.7 Write Enable (WE#)

The Write Enable pin, WE#, controls the Bus Write operation of the memory's command interface.

2.8 V_{PP}/Write Protect (V_{PP}/WP#)

The V_{PP}/Write Protect pin provides two functions, Write Protect function and the V_{PPH} function, which protect the lowest or highest block and allow the memory to enter unlock bypass mode respectively.

The Write Protect function provides a hardware method of protecting the highest or lowest block (see *Section 1: Description*). When V_{PP}/Write Protect is Low, V_{IL}, the highest or lowest block is protected. Program and Erase operations on this block are ignored while V_{PP}/Write Protect is Low.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection status of the highest or lowest block. Program and Erase operations can now modify the data in this block unless the block is protected using Block protection.

When V_{PP}/Write Protect is raised to V_{PPH} the memory automatically enters the Unlock Bypass mode (see *Section 6.2.4*).

When V_{PP}/Write Protect returns to V_{IH} or V_{IL} normal operation resumes. See the description of the Unlock Bypass command in the command interface section. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than t_{VHVPP} (see *Figure 28: Accelerated program timing waveforms*).

Never raise V_{PP}/Write Protect to V_{PPH} from any mode except Read mode, otherwise the memory may be left in an indeterminate state. A 0.1 µF capacitor should be connected between the VPP/Write Protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program (see I_{PP1}, I_{PP2}, I_{PP3}, I_{PP4} in *Table 22: DC characteristics*).

The V_{PP}/Write Protect pin may be left unconnected as it features an internal pull-up resistor.

Note: For 2-Gbit (1-Gbit/1-Gbit stack) device, When VPP/WP# pin is low, both the highest block and the lowest block are hardware-protected, namely block 0 and block 2047.

Refer to *Table 2* for a summary of V_{PP}/WP# functions.

Table 2. V_{PP}/WP# functions

V_{PP}/WP#	Function
V_{IL}	Highest block protected or lowest block protected.(1)
V_{IH}	Highest and lowest block unprotected unless a software protection is activated (see *Section 4: Hardware Protection*).
V_{PPH}	Unlock bypass mode.

1. For 2-Gbit (1-Gbit/1-Gbit stack) device, both the highest block and the lowest block are hardware-protected, namely block 0 and block 2047.

2.9 Reset (RST#)

The Reset pin can be used to apply a Hardware Reset to the memory. A Hardware Reset is achieved by holding Reset Low, V_{IL}, for at least t_{PLPX}. After Reset goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.10: Ready/Busy output (RY/BY#)*, *Table 26: Reset AC characteristics*, *Figure 26* and *Figure 27* for more details.

2.10 Ready/Busy output (RY/BY#)

The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a program or erase operation. During program or erase operations Ready/Busy is Low, V_{OL} (see *Table 17: Status Register bits*). Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See *Table 26: Reset AC characteristics*, *Figure 26* and *Figure 27*.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A low value will then indicate that one, or more, of the memories is busy. The 10Kohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.

2.11 Byte/Word organization select (BYTE#)

The BYTE# pin is used to switch between the x8 and x16 Bus modes of the memory. When Byte/Word organization select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} supply voltage

V_{CC} provides the power supply for all operations (Read, Program and Erase). The command interface is disabled when the V_{CC} supply voltage is less than the Lockout voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power-up, power-down and power surges. If the Program/Erase controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations (see I_{CC1}, I_{CC2}, I_{CC3} in *Table 22: DC characteristics*).

2.13 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

2.14 V_{SS} ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins; both of which must be connected to the system ground.

3 Bus Operations

There are five standard bus operations that control the device. These are Bus Read (Random and Page modes), Bus Write, Output Disable and Standby.

See *Table 3: Bus operations, 8-bit mode* and *Table 4: Bus operations, 16-bit mode* for a summary. Typical glitches of less than 3ns on Chip Enable, Write Enable, and Reset pins are ignored by the memory and do not affect bus operations.

3.1 Bus Read

Bus Read operations read from the memory cells, or specific registers in the command interface. To speed up the read operation the memory array can be read in Page mode where data is internally read and stored in a page buffer. The page has a size of 16 words (or 32bytes) and is addressed by the address inputs A3-A0 in x16 bus mode and A3-A0 plus DQ15/A–1 in x8 bus mode.The page read mode is not supported for reading Extended Memory Blocks and CFI information.

A valid Bus Read operation involves setting the desired address on the Address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data inputs/outputs will output the value, see *Figure 17: Random Read AC waveforms (8-bit mode)*, *Figure 20: Page Read AC waveforms (16-bit mode)*, and *Table 23: Read AC characteristics*, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write to the command interface. A valid Bus Write operation begins by setting the desired address on the Address inputs. The Address inputs are latched by the command interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data inputs/outputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See *Figure 21*, and *Figure 22*, Write AC waveforms, and *Table 24* and *Table 25*, Write AC characteristics, for details of the timing requirements.

3.3 Output Disable

The Data inputs/outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.4 Standby

Driving Chip Enable High in Read mode, causes the memory to enter Standby mode and the data inputs/outputs pins are placed in the high-impedance state. To reduce the Supply current to the Standby Supply current, I_{CC2}, Chip Enable should be held within V_{CC} ± 0.3 V. For the Standby current level see *Table 22: DC characteristics*.

During program or erase operations the memory will continue to use the Program/Erase Supply current, I_{CC3}, for Program or Erase operations until the operation completes.

3.5 Reset

During Reset mode the memory is deselected and the outputs are high impedance. The memory is in Reset mode when RST# is at V_{IL}. The power consumption is reduced to the standby level, independently from the Chip Enable, Output Enable or Write Enable inputs.

3.6 Auto Select mode

The Auto Select mode allows the system or the programming equipment to read the electronic signature, verify the protection status of the Extended Memory Block, and apply/remove Block protection. For example, this mode can be used by programming equipment to automatically match a device and the application code to be programmed.

At power-up, the device is in Read mode, and can then be put in Auto Select mode by issuing the Auto Select command (see *Section 6.1.2*).

The device cannot enter Auto Select mode when a program or erase operation is in progress (RY/BY# Low). However, Auto Select mode can be entered if the program or erase operation has been suspended by issuing a Program Suspend or Erase Suspend command (see *Section 6.1.7*).

The Auto Select mode is exited by performing a reset. The device is returned to Read mode, except if the Auto Select mode was entered after an Erase Suspend or a Program Suspend command. In this case, it returns to the Erase or Program Suspend mode.

3.6.1 Read electronic signature

The memory has two codes, the manufacturer code and the device code used to identify the memory. These codes can be accessed by performing read operations with control signals and addresses set as shown in *Table 5: Read electronic signature - auto select mode - programmer method (8-bit mode)* and *Table 6: Read electronic signature - auto select mode - programmer method (16-bit mode)*.

These codes can also be accessed by issuing an Auto Select command (see *Section 6.1.2: Auto Select command*).

3.6.2 Verify Extended Memory Block protection indicator

The Extended Memory Block is either Numonyx pre-locked or customer-lockable.

The protection status of the Extended Memory Block (pre-locked or customer-lockable) can be accessed by reading the Extended Memory Block protection indicator. It can be read in Auto Select mode using either the programmer (see *Table 7* and *Table 8*) or the in-system method (see *Table 9* and *Table 10*).

The protection status of the Extended Memory Block is then output on bit DQ7 of the Data input/outputs (see *Table 3* and *Table 4*, Bus operations in 8-bit and 16-bit mode).

3.6.3 Verify block protection status

The protection status of a block can be determined by performing a read operation with control signals and addresses set as shown in *Table 7* and *Table 8*.

If the block is protected, then 01h (in x 8 mode) is output on Data input/outputs DQ0-DQ7, otherwise 00h is output.

3.6.4 Hardware Block Protect

The V_{PP}/WP# pin can be used to protect the highest or lowest block. When V_{PP}/WP# is at V_{IL}, the highest block (M29EWH) or the lowest block (M29EWL) is protected and the other blocks remain with their own protection status.

Table 3. Bus operations, 8-bit mode

Operation[1]	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs	Data Inputs/Outputs	
						Amax-A0, DQ15/A-1	DQ14-DQ8	DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Hi-Z	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}[2]	Command address	Hi-Z	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If WP# is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 4. Bus operations, 16-bit mode

Operation[1]	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs	Data Inputs/Outputs
						Amax-A0	DQ15/A-1, DQ14-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}[2]	Command address	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	X	Hi-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If WP# is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 5. Read electronic signature - auto select mode - programmer method (8-bit mode)

Read cycle(1)	CE#	OE#	WE#	Address inputs						Data inputs/outputs	
				Amax-A4	A3	A2	A1	A0	DQ15/A-1	DQ14-DQ8	DQ7-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	89h
Device code (cycle 1)					V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	7Eh
Device code (cycle 2)					V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	22h (256-Mbit) 23h (512-Mbit) 28h (1-Gbit) 48h (2-Gbit)
Device code (cycle 3)					V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	01h

1. X = V_{IL} or V_{IH}.

Table 6. Read electronic signature - auto select mode - programmer method (16-bit mode)

Read cycle(1)	CE#	OE#	WE#	Address inputs					Data inputs/outputs
				Amax-A4	A3	A2	A1	A0	DQ15/A-1, DQ14-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0089h
Device code (cycle 1)					V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Device code (cycle 2)					V_{IH}	V_{IH}	V_{IH}	V_{IL}	2222h (256-Mbit) 2223h (512-Mbit) 2228h (1-Gbit) 2248h (2-Gbit)
Device code (cycle 3)					V_{IH}	V_{IH}	V_{IH}	V_{IH}	2201h

1. X = V_{IL} or V_{IH}.

Table 7. Block protection - auto select mode - programmer method (8-bit mode)

Operation[1]		CE#	OE#	WE#	Address inputs					Data inputs/outputs	
					Amax-A16	A15-A2	A1	A0	DQ15/A-1	DQ14-DQ8	DQ7-DQ0
Verify Extended Memory Block protection indicator (bit DQ7)	M29EWL	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	89h (Numonyx pre-locked) 09h (customer-lockable)
	M29EWH										99h (Numonyx pre-locked) 19h (customer-lockable)
Verify block protection status					BBA			V_{IL}			01h (protected) 00h (unprotected)

1. X = V_{IL} or V_{IH}. BBA = Block Base Address.

Table 8. Block protection - auto select mode - programmer method (16-bit mode)

Operation[1]		CE#	OE#	WE#	Address inputs				Data inputs/outputs
					Amax-A16	A15-A2	A1	A0	DQ15/A-1, DQ14-DQ0
Verify Extended Memory Block indicator (bit DQ7)	M29EWL	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	0089h (Numonyx pre-locked) 0009h (customer-lockable)
	M29EWH								0099h (Numonyx pre-locked) 0019h (customer-lockable)
Verify block protection status					BBA			V_{IL}	0001h (protected) 0000h (unprotected)

1. X = V_{IL} or V_{IH}. BBA = Block Base Address.

4 Hardware Protection

The M29EW features a V_{PP}/WP# pin that protects the highest or lowest block. Refer to *Section 2: Signal Descriptions* for a detailed description of the signal.

5 Software Protection

The M29EW has four different software protection modes:

- Volatile Protection
- Non-Volatile Protection
- Password Protection
- Password Access

On first use all parts default to operate in non-volatile Protection mode and the customer is free to activate the non-volatile or the password protection mode.

The desired protection mode is activated by setting either the one-time programmable Non-Volatile Protection Mode Lock bit, or the Password Protection Mode Lock bit of the Lock Register (see *Section 7.1: Lock Register*). Programming the Non-Volatile Protection Mode Lock bit or the Password Protection Mode Lock bit, to '0' will permanently activate the Non-volatile or the Password Protection mode, respectively. These two bits are one-time programmable and non-volatile: once the protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected protection mode. It is recommended to activate the desired software protection mode when first programming the device.

The Non-volatile and Password Protection modes both provide non-volatile Protection. Volatilely protected blocks and non-volatilely protected blocks can co-exist within the memory array. However, the volatile Protection only control the protection scheme for blocks that are not protected using the non-volatile or password protection.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The device is shipped with all blocks unprotected. The block protection status can be read either by performing a read electronic signature (see *Table 5* and *Table 6*) or by issuing an Auto Select command (see *Table 16: Block Protection Status*).

For the lowest and highest blocks, an even higher level of block protection can be achieved by locking the blocks using the non-volatile Protection and then by holding the V_{PP}/WP# pin Low.

Password Access is a security enhancement offered on the M29EW device. This feature protects information stored in the main-array blocks by preventing content alteration or reads until a valid 64-bit password is received. Password Access may be combined with Non-Volatile and/or Volatile Protection to create a multi-tiered solution.

Please contact your Numonyx Sales for further details concerning Password Access feature.

5.1 Volatile Protection mode

The volatile Protection allows the software application to easily protect blocks against inadvertent change. However, the protection can be easily disabled when changes are needed. Volatile Protection bits, VPBs, are volatile and unique for each block and can be individually modified. VPBs only control the protection scheme for unprotected blocks that have their non-volatile Protection bits, NVPBs, cleared (erased to '1') (see *Section 5.2: Non-Volatile Protection mode* and *Section 6.3.5: Non-Volatile Protection mode command set*).

By issuing the VPB Program or VPB Clear commands, the VPBs are set (programmed to '0') or cleared (erased to '1'), thus placing associated blocks in the protected or unprotected state respectively. The VPBs can be set (programmed to '0') or cleared (erased to '1') as often as needed.

When the parts are first shipped, or after a power-up or hardware reset, the VPBs default to be cleared.

Refer to *Section 6.3.7* for a description of the volatile Protection mode command set.

5.2 Non-Volatile Protection mode

5.2.1 Non-Volatile Protection bits

A non-volatile Protection bit (NVPB) is assigned to each block.

When a NVPB is set to '0', the associated block is protected, preventing any program or erase operations in this block.

The NVPB bits can be set individually by issuing a NVPB Program command. They are non-volatile and will remain set through a hardware reset or a power-down/power-up sequence.

The NVPBs cannot be cleared individually, they can only be all cleared at the same time by issuing a Clear all Non-Volatile Protection bits command.

The NVPBs can be protected all at a time by setting a volatile bit, the NVPB Lock bit (see *Section 5.2.2: Non-Volatile Protection Bit Lock bit*).

If one of the non-volatile protected blocks needs to be unprotected (corresponding NVPB set to '1'), a few more steps are required:

1. First, the NVPB Lock bit must be '1' by either putting the device through a power cycle, or hardware reset.
2. The NVPBs can then be changed to reflect the desired settings.
3. The NVPB Lock bit must be set to '0' once again to lock the NVPBs by associated command. The device operates normally again.

Note: 1 To achieve the best protection, it is recommended to execute the NVPB Lock Bit Program command early in the boot code and to protect the boot code by holding V_{PP}/WP# Low, V_{IL}.

2 The NVPBs and VPBs have the same function when V_{PP}/WP# pin is High, V_{IH}, as they do when V_{PP} /WP# pin is at the voltage for program acceleration (V_{PPH}).

Refer to *Table 16: Block Protection Status* and *Figure 6: Software protection scheme* for details on the block protection mechanism, and to *Section 6.3.5* for a description of the Non-Volatile Protection mode command set.

5.2.2 Non-Volatile Protection Bit Lock bit

The Non-Volatile Protection Bit Lock bit (NVPB Lock bit) is a global volatile bit for all NVPBs.

When set (programmed to ‘0’), it prevents changing the state of the NVPBs. When reset to ‘1’, the NVPBs can be set and reset using the NVPB Program command and Clear all NVPBs command, respectively.

There is only one NVPB Lock bit per device.

Refer to *Section 6.3.6* for a description of the NVPB Lock bit command set.

Note: 1 No software command unlocks this bit unless the device is in password protection mode; in standard non-volatile Protection mode, it can be cleared only by taking the device through a hardware reset or a power-up.

2 The NVPB Lock bit must be set (programmed to ‘0’) only after all NVPBs are configured to the desired settings.

5.3 Password Protection mode

The password protection mode provides an even higher level of security than the Non-Volatile Protection mode by requiring a 64-bit password for unlocking the device NVPB Lock bit.

In addition to this password requirement, the NVPB Lock bit is set ‘0’ after power-up and reset to maintain the device in password protection mode. Successful execution of the Password Unlock command by entering the correct password clears the NVPB Lock bit, allowing for block NVPBs to be modified.

If the password provided is incorrect, the NVPB Lock bit remains locked and the state of the NVPBs cannot be modified.

To place the device in password protection mode, the following steps are required:

1. Prior to activating the password protection mode, it is necessary to set a 64-bit password and to verify it (see *Password Program command* and *Password Read command*). Password verification is only allowed before the password protection mode is activated.
2. The password protection mode is then activated by programming the Password Protection Mode Lock bit to ‘0’. This operation is not reversible and once the bit is programmed it cannot be erased, the device permanently remains in password protection mode, and the 64-bit password can neither be retrieved nor reprogrammed. Moreover, all commands to the address where the password is stored, are disabled. Refer to *Table 16: Block Protection Status* and *Figure 6: Software protection scheme* for details on the block protection scheme.

Refer to *Section 6.3.4* for a description of the Password Protection mode command set.

Note: There is no means to verify the password after Password Protection mode is enabled. If the password is lost after enabling the Password Protection mode, there is no way to clear the NVPB Lock bit.