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Numonyx™ Embedded Flash Memory (J3 v D)

32, 64, 128, and 256 Mbit (Monolithic)

Datasheet

Product Features

- Architecture
  - — Symmetrical 128-Kbyte blocks
  - — 256 Mbit (256 blocks)
  - — 128 Mbit (128 blocks)
  - — 64 Mbit (64 blocks)
  - — 32 Mbit (32 blocks)
- Performance
  - — 75 ns Initial Access Speed (32,64,128 Mbit densities)
  - — 95 ns Initial Access Speed (256Mbit only)
  - — 25 ns 8-word and 4-word Asynchronous page-mode reads
  - — 32-Byte Write buffer; 4 µs per Byte Effective programming time
- System Voltage
  - — V_{CC} = 2.7 V to 3.6 V
  - — V_{CCQ} = 2.7 V to 3.6 V
- Packaging
  - — 56-Lead TSOP (32, 64, 128, 256 Mbit)
  - — 64-Ball Numonyx Easy BGA package (32, 64, 128 and 256 Mbit)
- Security
  - — Enhanced security options for code protection
  - — 128-bit Protection Register: 64-bits Unique device identifier bits 64-bits User-programmable OTP bits
  - — Absolute protection with V_{PEN} = GND
  - — Individual block locking
  - — Block erase/program lockout during power transitions
- Software
  - — Program and erase suspend support
  - — Flash Data Integrator (FDI), Common Flash Interface (CFI) Compatible
- Quality and Reliability
  - — Operating temperature: -40 °C to +85 °C
  - — 100K Minimum erase cycles per block
  - — 0.13 µm ETOX™ VIII Process technology

316577-06
December 2007

Contents

Revision History

Date	Revision	Description
February 2007	001	Initial release
March 2007	002	Revised the following graphics to support 256Mbit: • Figure 1, "Intel® Embedded Flash Memory (J3 v. D) Memory Block Diagram (32, 64 and 128, 256Mbit)" on page 10. • Figure 5, "Easy BGA Ballout (32/64/128/256 Mbit)" on page 15. • Figure 28, "Decoder for Discrete Family, 32-, 64-, 128-, 256-Mbit (monolithic)" on page 67.
May 2007	003	Minor revisions
August 2007	004	Updated title page to reflect a 256-Mbit monolithic die.
November 2007	005	Updated the 65nm pre-enabling information
December 2007	006	Revised the Signal Description Table and clarified Chip Enable (CE) definitions Applied Numonyx branding.

1.0 Introduction

This document contains information pertaining to the Numonyx™ Embedded Flash Memory (J3 v D) device features, operation, and specifications.

The Numonyx™ Embedded Flash Memory J3 Version D (J3 v. D) provides improved mainstream performance with enhanced security features, taking advantage of the high quality and reliability of the NOR-based Intel 0.13 µm ETOX* VIII process technology. Offered in 256-Mbit, 128-Mbit, 64-Mbit, and 32-Mbit densities, theNumonyx™ Embedded Flash Memory (J3 v D, Monolithic) device brings reliable, low-voltage capability (3 V read, program, and erase) with high speed, low-power operation. The Numonyx™ Embedded Flash Memory (J3 v D, Monolithic) device takes advantage of proven manufacturing experience and is ideal for code and data applications where high density and low cost are required, such as in networking, telecommunications, digital set top boxes, audio recording, and digital imaging.Numonyx Flash Memory components also deliver a new generation of forward-compatible software support. By using the Common Flash Interface (CFI) and Scalable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Numonyx Flash Memory devices.

The J3v.D product family is also planned on the 65nm process lithography, 65nm AC timing changes are noted in this datasheet and should be taken into account for all new designs.

1.1 Nomenclature

AMIN	All Densities	AMIN = A0 for x8
	All Densities	AMIN = A1 for x16
AMAX	32 Mbit	AMAX = A21
	64 Mbit	AMAX = A22
	128 Mbit	AMAX = A23
	256 Mbit	AMAX = A24
Block	A group of flash cells that share common erase circuitry and erase simultaneously.	
Clear	Indicates a logic zero (0)	
Program	Writes data to the flash array	
Set	Indicates a logic one (1)	
VPEN	Refers to a signal or package connection name	
V_{PEN}	Refers to timing or voltage levels	

1.2 Acronyms

CUI	Command User Interface
OTP	One Time Programmable
PLR	Protection Lock Register

PR	Protection Register
PRD	Protection Register Data
RFU	Reserved for Future Use
SR	Status Register
SRD	Status Register Data
WSM	Write State Machine
ECR	Enhanced Configuration Register

1.3 Conventions

h: Hexadecimal Suffix

k (noun): 1,000

M (noun): 1,000,000

Nibble 4 bits

Byte: 8 bits

Word: 16 bits

Kword: 1,024 words

Kb: 1,024 bits

KB: 1,024 bytes

Mb: 1,048,576 bits

MB: 1,048,576 bytes

Brackets: Square brackets ([]) will be used to designate group membership or to define a group of signals with similar function (i.e. A[21:1], SR[4,1] and D[15:0]).

00FFh: Denotes 16-bit hexadecimal numbers

00FF 00FFh: Denotes 32-bit hexadecimal numbers

DQ[15:0]: Data I/O signals

2.0 Functional Overview

The Numonyx™ Embedded Flash Memory (J3 v D) family contains high-density memory organized in any of the following configurations:

- 32 Mbytes or 16 Mwords (256-Mbit), organized as two-hundred-fifty-six 128-Kbyte erase blocks.
- 16 Mbytes or 8 Mwords (128-Mbit), organized as one-hundred-twenty-eight 128-Kbyte erase blocks.
- 8 Mbytes or 4 Mwords (64-Mbit), organized as sixty-four 128-Kbyte erase blocks.
- 4 Mbytes or 2 Mwords (32-Mbit), organized as thirty-two 128-Kbyte erase blocks.

These devices can be accessed as 8- or 16-bit words. See Figure 1, "Memory Block Diagram, 32-, 64-, 128-, and 256-Mbit (monolithic)" on page 10 for further details.

A 128-bit Protection Register has multiple uses, including unique flash device identification.

The Numonyx™ Embedded Flash Memory (J3 v D) device includes new security features that were not available on the (previous) 0.25µm and 0.18µm versions of the J3 family. These new security features prevent altering of code through different protection schemes that can be implemented, based on user requirements.

The Numonyx™ Embedded Flash Memory (J3 v D, Monolithic) optimized architecture and interface dramatically increases read performance by supporting page-mode reads. This read mode is ideal for non-clock memory systems.

Its Common Flash Interface (CFI) permits software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

The Scalable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 128-Kbyte blocks typically within one second, independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or program data from any other block. Similarly, program suspend allows system software to suspend programming (byte/word program and write-to-buffer operations) to read data or execute code from any other block that is not being suspended.

Each device incorporates a Write Buffer of 32 bytes (16 words) to allow optimum programming performance. By using the Write Buffer data is programmed more efficiently in buffer increments.

Memory Blocks are selectively and individually lockable in-system. Individual block locking uses block lock-bits to lock and unlock blocks. Block lock-bits gate block erase and program operations. Lock-bit configuration operations set and clear lock-bits (using the Set Block Lock-Bit and Clear Block Lock-Bits commands).

The Status Register indicates when the WSM's block erase, program, or lock-bit configuration operation completes.

The STS (status) output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status indication using STS minimizes both CPU overhead and system power consumption. When configured in level mode (default mode), it acts as a RY/BY# signal. When low, STS indicates that the WSM is performing a block erase, program, or lock-bit configuration. STS-high indicates that the WSM is ready for a new command, block erase is suspended (and programming is inactive), program is suspended, or the device is in reset/power-down mode. Additionally, the configuration command allows the STS signal to be configured to pulse on completion of programming and/or block erases.

Three CE signals are used to enable and disable the device. A unique CE logic design (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31) reduces decoder logic typically required for multi-chip designs. External logic is not required when designing a single chip, a dual chip, or a 4-chip miniature card or SIMM module.

The BYTE# signal allows either x8 or x16 read/writes to the device:

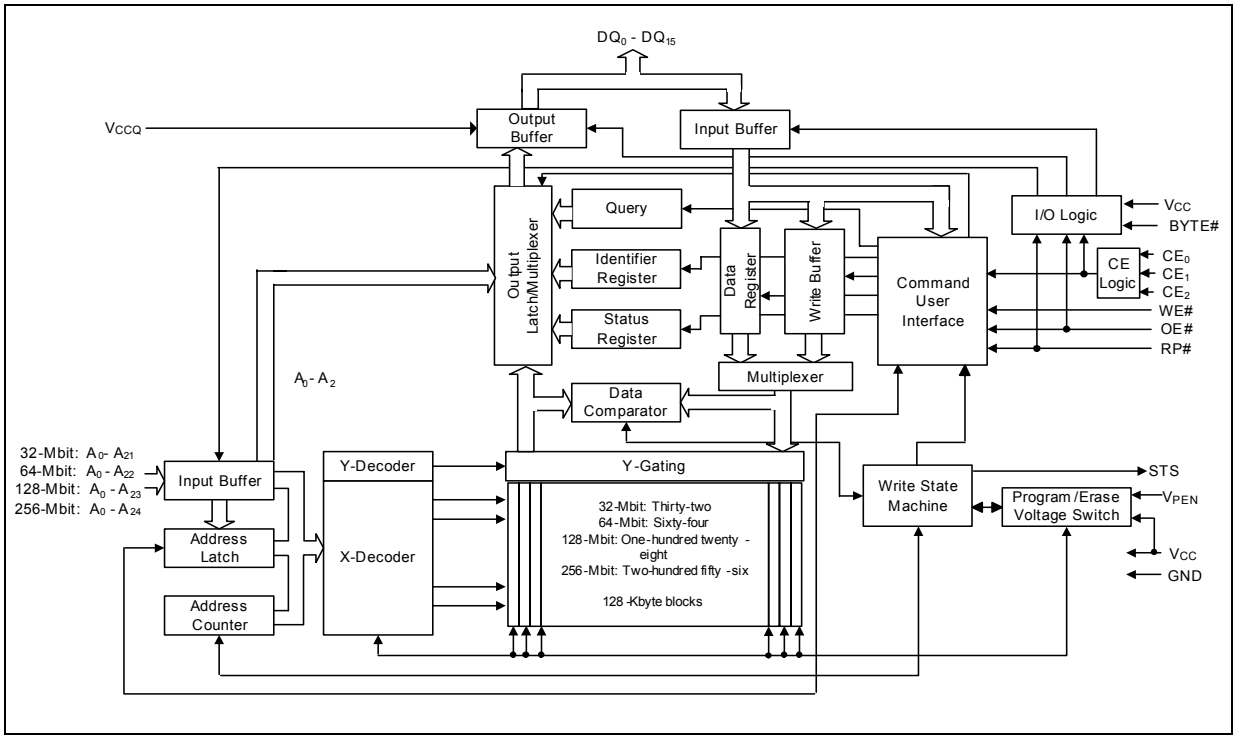
- BYTE#-low enables 8-bit mode; address A0 selects between the low byte and high byte.
- BYTE#-high enables16-bit operation; address A1 becomes the lowest order address and address A0 is not used (don't care).

Figure 1, "Memory Block Diagram, 32-, 64-, 128-, and 256-Mbit (monolithic)" on page 10 shows a device block diagram.

When the device is disabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31), with CEx at VIH and RP# at VIH, the standby mode is enabled. When RP# is at VIL, a further power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (tPHQV) is required from RP# going high until data outputs are valid. Likewise, the device has a wake time (tPHWL) from RP#-high until writes to the CUI are recognized. With RP# at VIL, the WSM is reset and the Status Register is cleared.

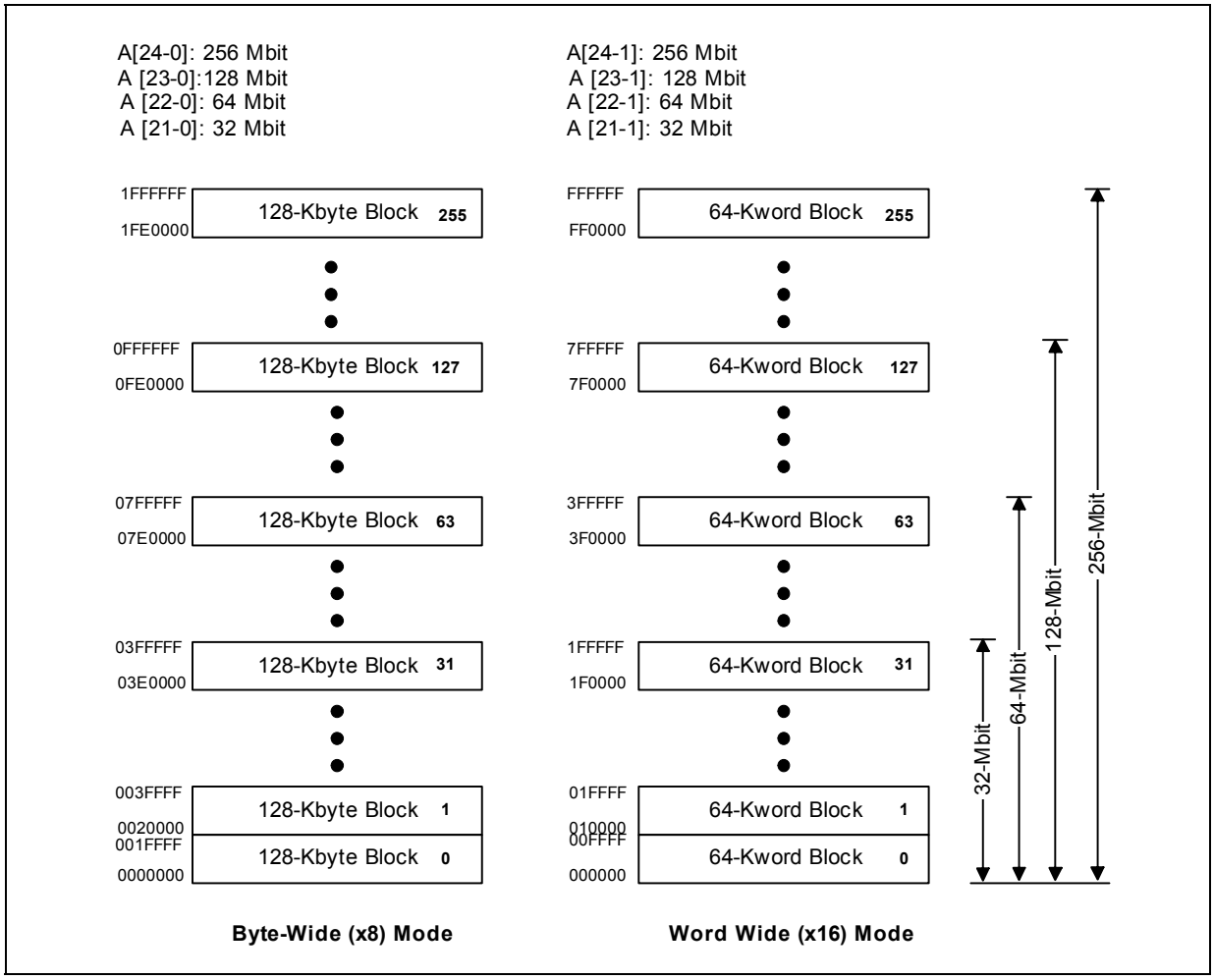
2.1 Block Diagram

Figure 1: Memory Block Diagram, 32-, 64-, 128-, and 256-Mbit (monolithic)



2.2 Memory Map

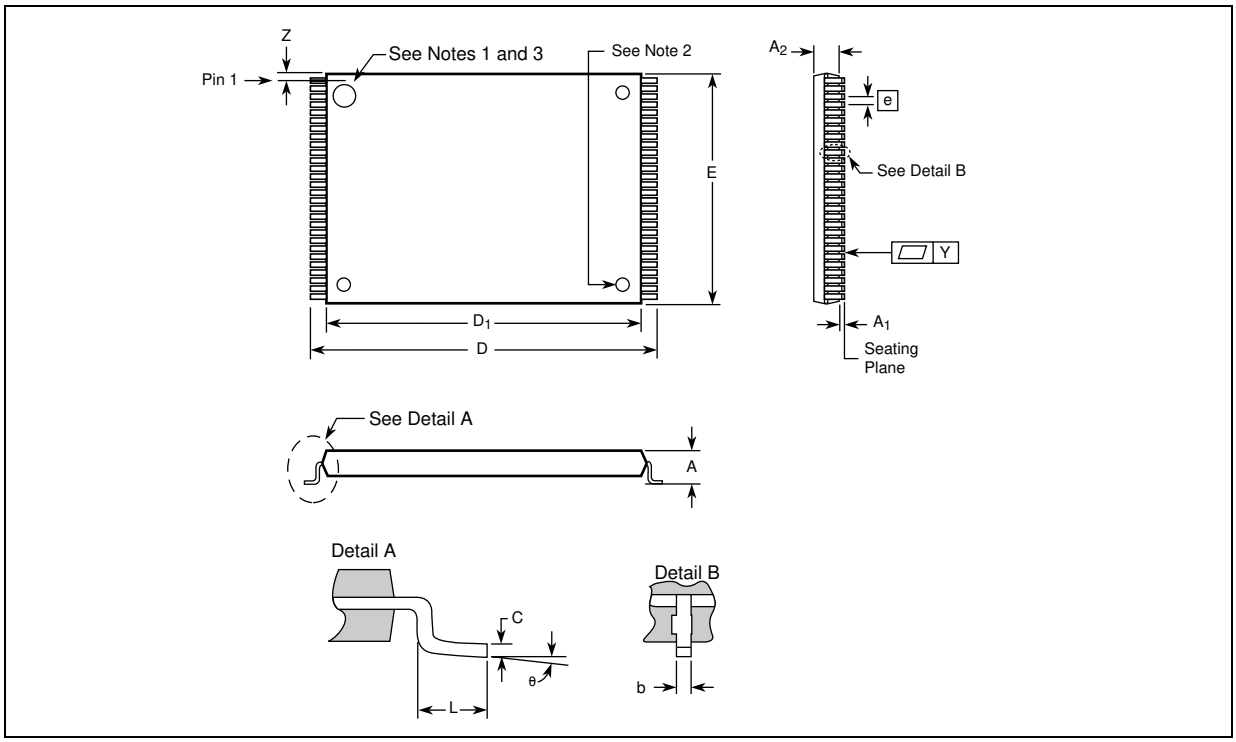
Figure 2: Numonyx™ Embedded Flash Memory (J3 v D, Monolithic) Memory Map



3.0 Package Information

3.1 56-Lead TSOP Package, 32-, 64-, 128-, and 256-Mbit

Figure 3: 56-Lead TSOP Package Mechanical



Notes:
1. One dimple on package denotes Pin 1.
2. If two dimples, then the larger dimple denotes Pin 1.
3. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.

Table 1: 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A			1.200			0.047
Standoff	A_1	0.050			0.002		
Package Body Thickness	A_2	0.965	0.995	1.025	0.038	0.039	0.040
Lead Width	b	0.100	0.150	0.200	0.004	0.006	0.008
Lead Thickness	c	0.100	0.150	0.200	0.004	0.006	0.008
Package Body Length	D_1	18.200	18.400	18.600	0.717	0.724	0.732
Package Body Width	E	13.800	14.000	14.200	0.543	0.551	0.559
Lead Pitch	e		0.500			0.0197	
Terminal Dimension	D	19.800	20.00	20.200	0.780	0.787	0.795
Lead Tip Length	L	0.500	0.600	0.700	0.020	0.024	0.028

Table 1: 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Lead Count	N		56			56	
Lead Tip Angle	q	0°	3°	5°	0°	3°	5°
Seating Plane Coplanarity	Y			0.100			0.004
Lead to Package Offset	Z	0.150	0.250	0.350	0.006	0.010	0.014

3.2 Easy BGA Package, 32-, 64-, 128-, and 256-Mbit

Figure 4: Easy BGA Mechanical Specifications

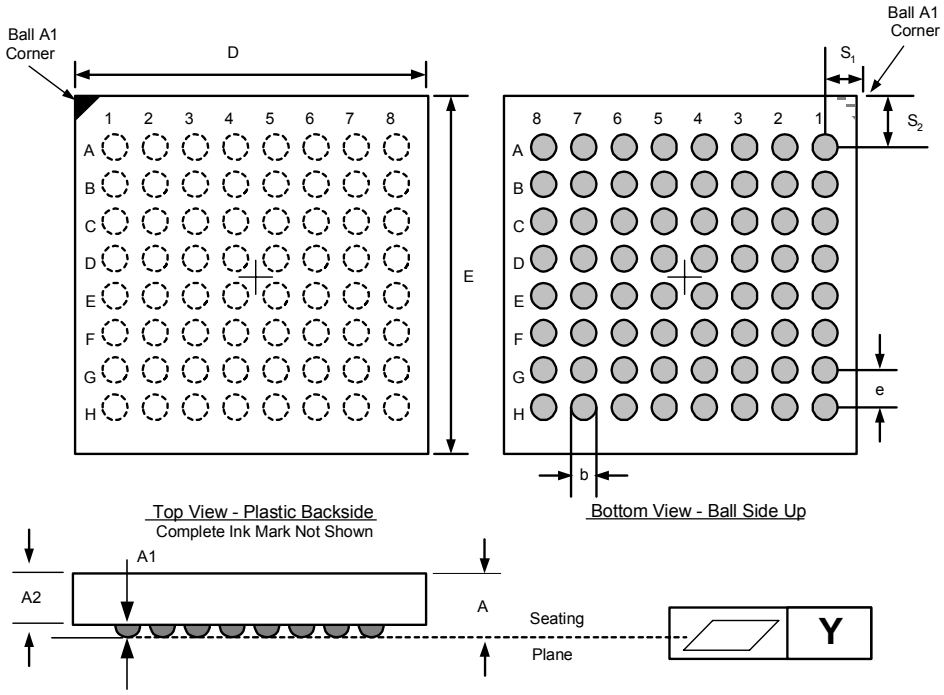


Table 2: Easy BGA Package Dimensions Table (Sheet 1 of 2)

Parameter	Symbol	Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Height (32, 64, 128, 256 Mbit)	A			1.200				0.0472
Ball Height	A1	0.250				0.0098		
Package Body Thickness (32, 64, 128, 256 Mbit)	A2		0.780				0.0307	
Ball (Lead) Width	b	0.330	0.430	0.530		0.0130	0.0169	0.0209

Table 2: Easy BGA Package Dimensions Table (Sheet 2 of 2)

Parameter	Symbol	Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Body Width	D	9.900	10.000	10.100	1	0.3898	0.3937	0.3976
Package Body Length	E	12.900	13.000	13.100	1	0.5079	0.5118	0.5157
Pitch	[e]		1.000				0.0394	
Ball (Lead) Count	N		64				64	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D (32/64/128/256 Mb)	S1	1.400	1.500	1.600	1	0.0551	0.0591	0.0630
Corner to Ball A1 Distance Along E (32/64/128/256 Mb)	S2	2.900	3.000	3.100	1	0.1142	0.1181	0.1220

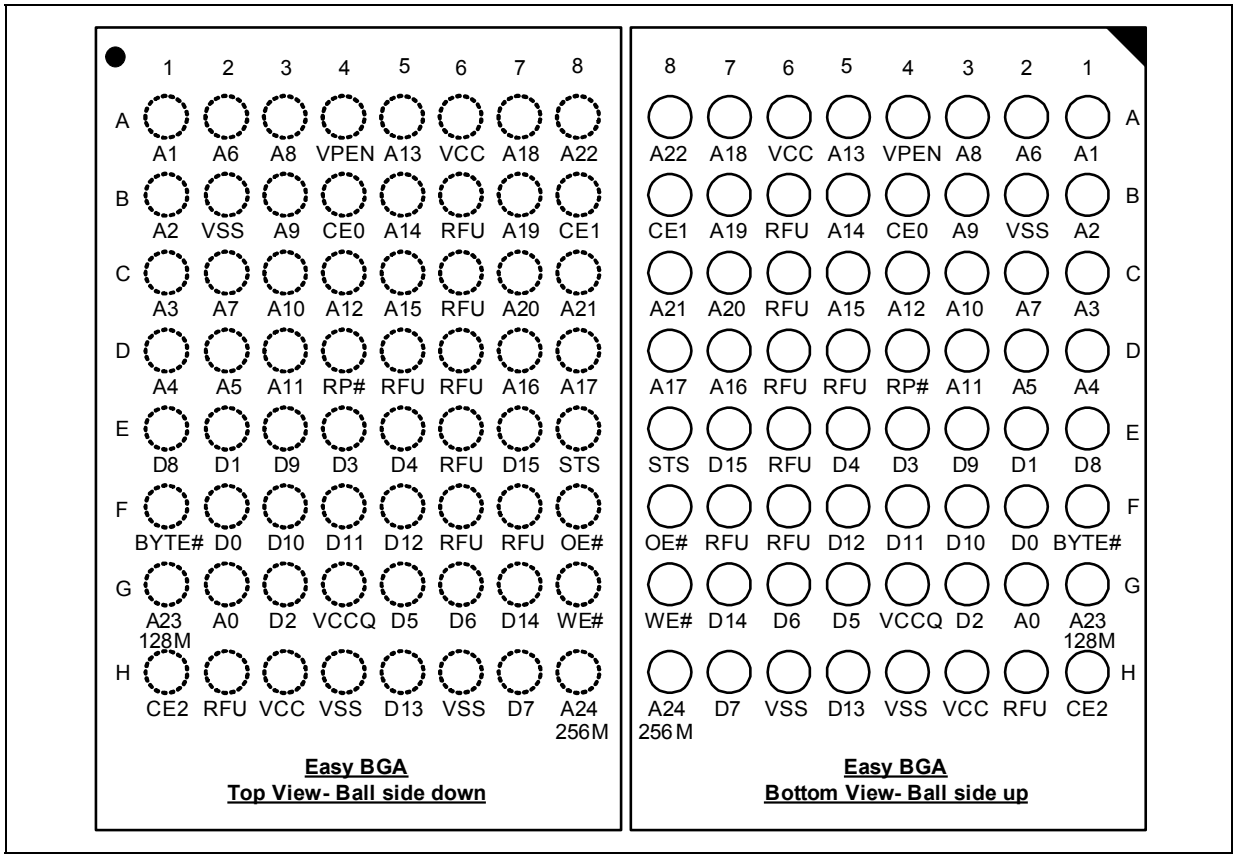
Notes:
1. For Daisy Chain Evaluation Unit information refer to packaging informaiton at: www.Numonyx.com.

4.0 Ballouts and Signal Descriptions

Numonyx™ Embedded Flash Memory (J3 v D) is available in two package types. All densities of the Numonyx™ Embedded Flash Memory (J3 v D, Monolithic) devices are supported on both 64-ball Easy BGA and 56-lead Thin Small Outline Package (TSOP) packages. The figures below show the ballouts.

4.1 Easy BGA Ballout, 32-, 64-,128-, 256-Mbit

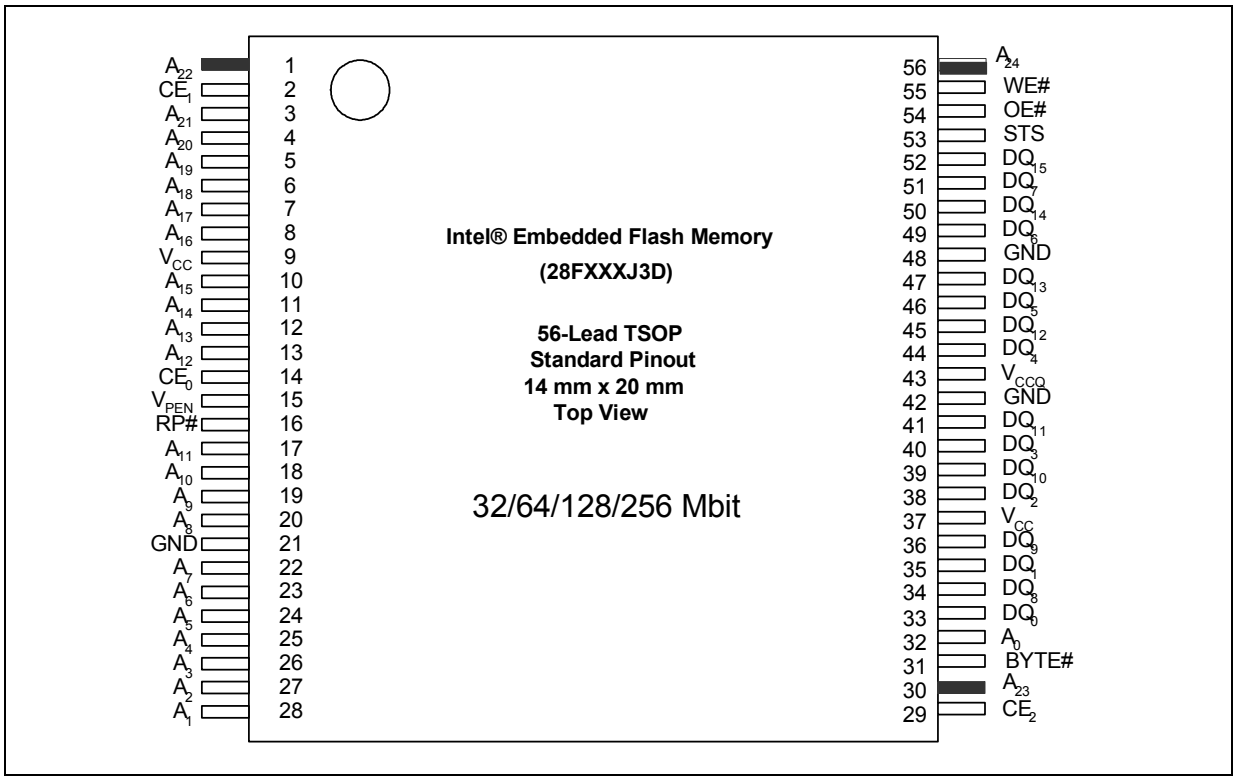
Figure 5: Easy BGA Ballout (32/64/128/256 Mbit)



Notes:
1. Address A22 is only valid on 64-Mbit densities and above, otherwise, it is a no connect (NC).
2. Address A23 is only valid on 128-Mbit densities and above, otherwise, it is a no connect (NC).
3. Address A24 is only valid on 256-Mbit density, otherwise, it is a no connect (NC).

4.2 56-Lead TSOP Package Pinout, 32-, 64-,128-, 256-Mbit

Figure 6: 56-Lead TSOP Package Pinout (32/64/128/256 Mbit)



Notes:
1. A22 exists on 64- and 128- densities. On 32-Mbit density this signal is a no-connect (NC).
2. A23 exists on 128-Mbit densities. On 32- and 64-Mbit densities this signal is a no-connect (NC)
3. A24 exists on 256-Mbit densities and on the other densities this signal is a no-connect (NC).

4.3 Signal Descriptions

Table 3 lists the active signals used on Numonyx™ Embedded Flash Memory (J3 v D, Monolithic) and provides a description of each.

Table 3: Signal Descriptions for Numonyx™ Embedded Flash Memory (J3 v D, Monolithic) (Sheet 1 of 2)

Symbol	Type	Name and Function
A0	Input	**BYTE-SELECT ADDRESS:** Selects between high and low byte when the device is in x8 mode. This address is latched during a x8 program cycle. Not used in x16 mode (i.e., the A0 input buffer is turned off when BYTE# is high).
A[MAX:1]	Input	**ADDRESS INPUTS:** Inputs for addresses during read and program operations. Addresses are internally latched during a program cycle: 32-Mbit — A[21:1] 64-Mbit— A[22:1] 128-Mbit — A[23:1] 256-Mbit — A[24:1]
D[7:0]	Input/ Output	**LOW-BYTE DATA BUS:** Inputs data during buffer writes and programming, and inputs commands during CUI writes. Outputs array, CFI, identifier, or status data in the appropriate read mode. Data is internally latched during write operations.

Table 3: Signal Descriptions for Numonyx™ Embedded Flash Memory (J3 v D, Monolithic) (Sheet 2 of 2)

Symbol	Type	Name and Function
D[15:8]	Input/ Output	**HIGH-BYTE DATA BUS:** Inputs data during x16 buffer writes and programming operations. Outputs array, CFI, or identifier data in the appropriate read mode; not used for Status Register reads. Data is internally latched during write operations in x16 mode. D[15-8] float in x8 mode
CE[2:0]	Input	**CHIP ENABLE:** Activate the 32-, 64-, 128-, and 256-Mbit devices' control logic, input buffers, decoders, and sense amplifiers. When the device is de-selected (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31), power reduces to standby levels. All timing specifications are the same for these three signals. Device selection occurs with the first edge of CE0, CE1, or CE2 that enables the device. Device deselection occurs with the first edge of CE0, CE1, or CE2 that disables the device (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31).
RP#	Input	**RESET:** RP#-low resets internal automation and puts the device in power-down mode. RP#-high enables normal operation. Exit from reset sets the device to read array mode. When driven low, RP# inhibits write operations which provides data protection during power transitions.
OE#	Input	**OUTPUT ENABLE:** Activates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	Input	**WRITE ENABLE:** Controls writes to the CUI, the Write Buffer, and array blocks. WE# is active low. Addresses and data are latched on the rising edge of WE#.
STS	Open Drain Output	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default), it acts as a RY/BY# signal. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. For alternate configurations of the Status signal, see the Configurations command and Section 9.6, "Status Signal" on page 42. STS is to be tied to VCCQ with a pull-up resistor.
BYTE#	Input	**BYTE ENABLE:** BYTE#-low places the device in x8 mode; data is input or output on D[7:0], while D[15:8] is placed in High-Z. Address A0 selects between the high and low byte. BYTE#-high places the device in x16 mode, and turns off the A0 input buffer. Address A1 becomes the lowest-order address bit.
VPEN	Input	**ERASE / PROGRAM / BLOCK LOCK ENABLE:** For erasing array blocks, programming data, or configuring lock-bits. With $V_{PEN} \le V_{PENLK}$, memory contents cannot be altered.
VCC	Power	**CORE Power Supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \le V_{\mathbf{lko}}$. Caution: Device operation at invalid Vcc voltages should not be attempted.
VCCQ	Power	**I/O Power Supply:** Power supply for Input/Output buffers.This ball can be tied directly to V_{CC}.
GND	Supply	**GROUND:** Ground reference for device logic voltages. Connect to system ground.
NC	—	**No Connect:** Lead is not internally connected; it may be driven or floated.
RFU	—	**Reserved for Future Use:** Balls designated as RFU are reserved by Numonyx for future device functionality and enhancement**.**

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Numonyx sales office that you have the latest datasheet before finalizing a design.

Table 4: Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Temperature under Bias Expanded (T_A, Ambient)	–40	+85	°C	—
Storage Temperature	–65	+125	°C	—
VCC Voltage	–2.0	+5.6	V	2
VCCQ	–2.0	+5.6	V	2
Voltage on any input/output signal (except VCC, VCCQ)	–2.0	V_{CCQ} (max) + 2.0	V	1
I_{SH} Output Short Circuit Current	—	100	mA	3

Notes:
1. Voltage is referenced to V_{SS}. During infrequent non-periodic transitions, the voltage potential between V_{SS} and input/output pins may undershoot to –2.0 V for periods < 20 ns or overshoot to V_{CCQ} (max) + 2.0 V for periods < 20 ns.
2. During infrequent non-periodic transitions, the voltage potential between V_{CC} and the supplies may undershoot to –2.0 V for periods < 20 ns or V_{SUPPLY} (max) + 2.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time

5.2 Operating Conditions

Warning: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability

Table 5: Temperature and V_{CC} Operating Condition

Symbol	Parameter	Min	Max	Unit	Test Condition
T_A		-40.0	+85	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage	2.70	3.6	V	—
V_{CCQ}	V_{CCQ} Supply Voltage	2.70	3.6	V	—

5.3 Power Up/Down

This section provides an overview of system level considerations with regards to the flash device. It includes a brief description of power-up, power-down and decoupling design considerations.

5.3.1 Power-Up/Down Characteristics

To prevent conditions that could result in spurious program or erase operations, the power-up/power-down sequence shown in Table 6 is recommended. For DC voltage characteristics refer to Table 8. Note that each power supply must reach its minimum voltage range before applying/removing the next supply voltage.

Table 6: Power-Up/Down Sequence

Power Supply Voltage	Power-UpSequence				Power-Down Sequence			
$V_{CC(min)}$	1st	1st	1st†	Sequencing not required†	3rd	2nd	2nd†	Sequencing not required†
$V_{CCQ(min)}$	2nd	2nd†			2nd	1st†		
$V_{PEN(min)}$	3rd		2nd		1st		1st	

† Power supplies connected or sequenced together.

Device inputs must not be driven until all supply voltages reach their minimum range. RP# should be low during power transitions.

5.3.2 Power Supply Decoupling

When the device is enabled, many internal conditions change. Circuits are energized, charge pumps are switched on, and internal voltage nodes are ramped. All of this internal activities produce transient signals. The magnitude of the transient signals depends on the device and system loading. To minimize the effect of these transient signals, a 0.1 µF ceramic capacitor is required across each VCC/VSS and VCCQ signal. Capacitors should be placed as close as possible to device connections.

Additionally, for every eight flash devices, a 4.7 µF electrolytic capacitor should be placed between VCC and VSS at the power supply connection. This 4.7 µF capacitor should help overcome voltage slumps caused by PCB trace inductance.

5.4 Reset

By holding the flash device in reset during power-up and power-down transitions, invalid bus conditions may be masked. The flash device enters reset mode when RP# is driven low. In reset, internal flash circuitry is disabled and outputs are placed in a high-impedance state. After return from reset, a certain amount of time is required before the flash device is able to perform normal operations. After return from reset, the flash device defaults to asynchronous page mode. If RP# is driven low during a program or erase operation, the program or erase operation will be aborted and the memory contents at the aborted block or address are no longer valid. See Figure 14, “AC Waveform for Reset Operation” on page 29 for detailed information regarding reset timings.

6.0 Electrical Characteristics

6.1 DC Current Specifications

Table 7: DC Current Characteristics (Sheet 1 of 2)

V_{CCQ}			2.7 - 3.6V			Test Conditions	Notes
V_{CC}			2.7 - 3.6V				
Symbol	**Parameter**		**Typ**	**Max**	**Unit**		
I_{LI}	Input and V_{PEN} Load Current			±1	µA	V_{CC} = V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{LO}	Output Leakage Current			±10	µA	V_{CC}= V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{CCS}	V_{CC} Standby Current	32, 64, 128, 256 Mbit	50	120	µA	CMOS Inputs, V_{CC} = V_{CC} Max; Vccq = VccqMax Device is disabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31), RP# = V_{CCQ} ± 0.2 V	1,2,3
		32, 64, 128, 256 Mbit	0.71	2	mA	TTL Inputs, V_{CC} = V_{CC} Max, Vccq = VccqMax Device is disabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31), RP# = V_{IH}	
I_{CCD}	V_{CC} Power-Down Current		50	120	µA	RP# = GND ± 0.2 V, I_{OUT} (STS) = 0 mA	
I_{CCR} V_{CC} Page Mode Read Current		4-Word Page	15	20	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max Device is enabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31) f = 5 MHz, I_{OUT} = 0 mA	1,3
			24	29	mA	CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max Device is enabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31) f = 33 MHz, I_{OUT} = 0 mA	
		8-Word Page	10	15	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. Device is enabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31) f = 5 MHz, I_{OUT} = 0 mA	
			30	54	mA	CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. Device is enabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31) f = 33 MHz, I_{OUT} = 0 mA	
I_{CCW}	V_{CC} Program or Set Lock-Bit Current		35	60	mA	CMOS Inputs, V_{PEN} = V_{CC}	1,4
			40	70	mA	TTL Inputs, V_{PEN} = V_{CC}	

Table 7: DC Current Characteristics (Sheet 2 of 2)

V_{CCQ}			2.7 - 3.6V			Test Conditions	Notes
V_{CC}			2.7 - 3.6V				
Symbol	**Parameter**		**Typ**	**Max**	**Unit**		
I_{CCE}	V_{CC} Block Erase or Clear Block Lock-Bits Current		35	70	mA	CMOS Inputs, $V_{PEN} = V_{CC}$	1,4
			40	80	mA	TTL Inputs, $V_{PEN} = V_{CC}$	
I_{CCWS} I_{CCES}	V_{CC} Program Suspend or Block Erase Suspend Current			10	mA	Device is enabled (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31)	1,5

Notes:
1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Numonyx or your local sales office for information about typical specifications.
2. Includes STS.
3. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
4. Sampled, not 100% tested.
5. I_{CCWS} and I_{CCES} are specified with the device selected. If the device is read or written while in erase suspend mode, the device's current draw is I_{CCR} and I_{CCWS}.

6.2 DC Voltage specifications

Table 8: DC Voltage Characteristics (Sheet 1 of 2)

V_{CCQ}		2.7 - 3.6 V			Test Conditions	Notes
V_{CC}		2.7 - 3.6 V				
Symbol	**Parameter**	**Min**	**Max**	**Unit**		
V_{IL}	Input Low Voltage	–0.5	0.8	V		2, 5, 6
V_{IH}	Input High Voltage	2.0	V_{CCQ} + 0.5V	V		2, 5, 6
V_{OL}	Output Low Voltage		0.4	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OL} = 2 mA	1, 2
			0.2	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OL} = 100 µA	
V_{OH}	Output High Voltage	0.85 × V_{CCQ}		V	$V_{CC} = V_{CCMIN}$ $V_{CCQ} = V_{CCQ}$ Min I_{OH} = –2.5 mA	1, 2
		V_{CCQ} – 0.2		V	$V_{CC} = V_{CCMIN}$ $V_{CCQ} = V_{CCQ}$ Min I_{OH} = –100 µA	
V_{PENLK}	V_{PEN} Lockout during Program, Erase and Lock-Bit Operations		2.2	V		2, 3

Table 8: DC Voltage Characteristics (Sheet 2 of 2)

V_{CCQ}		2.7 - 3.6 V			Test Conditions	Notes
V_{CC}		2.7 - 3.6 V				
Symbol	**Parameter**	**Min**	**Max**	**Unit**		
V_{PENH}	V_{PEN} during Block Erase, Program, or Lock-Bit Operations	2.7	3.6	V		3
V_{LKO}	V_{CC} Lockout Voltage		2.0	V		4

Notes:
1. Includes STS.
2. Sampled, not 100% tested.
3. Block erases, programming, and lock-bit configurations are inhibited when $V_{PEN} \leq V_{PENLK}$, and not guaranteed in the range between V_{PENLK} (max) and V_{PENH} (min), and above V_{PENH} (max).
4. Block erases, programming, and lock-bit configurations are inhibited when $V_{CC} < V_{LKO}$, and not guaranteed in the range between V_{LKO} (min) and V_{CC} (min), and above V_{CC} (max).
5. Includes all operational modes of the device including standby and power-up sequences
6. Input/Output signals can undershoot to -1.0v referenced to V_{SS} and can overshoot to V_{CCQ} = 1.0v for duration of 2ns or less, the V_{CCQ} valid range is referenced to V_{SS}.

6.3 Capacitance

Table 9: Capacitance

Symbol	Parameter[1]		Type	Max	Unit	Condition[2]
C_{IN}	Input Capacitance	32, 64, 128, 256 Mb	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	32, 64, 128, 256 Mb	8	12	pF	V_{OUT} = 0.0 V

Notes:
1. sampled.not 100% tested.
2. T_A = +25 °C, f = 1 MHZ

7.0 AC Characteristics

Timing symbols used in the timing diagrams within this document conform to the following convention

Figure 7: Timing Signal Naming Convention

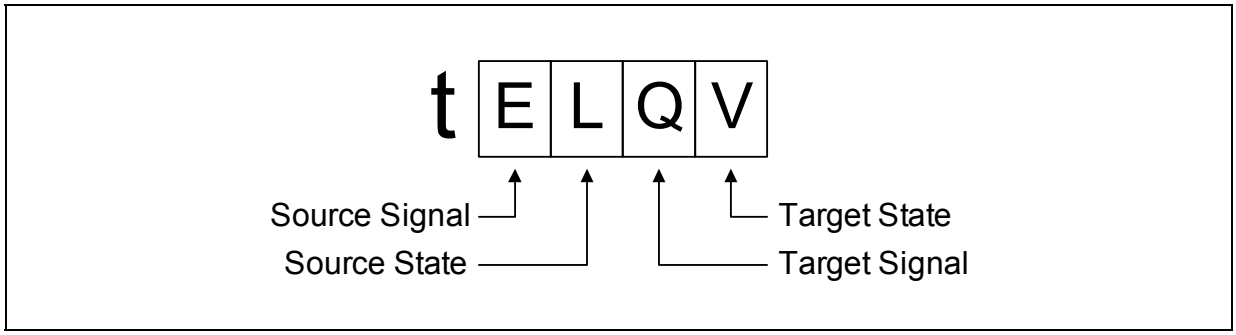


Figure 8: Timing Signal Name Decoder

Signal	Code	State	Code
Address	A	High	H
Data - Read	Q	Low	L
Data - Write	D	High-Z	Z
Chip Enable (CE)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Address Valid (ADV#)	V		
Reset (RP#)	P		
Clock (CLK)	C		
WAIT	T		

Note: Exceptions to this convention include t_{ACC} and t_{APA}. t_{ACC} is a generic timing symbol that refers to the aggregate initial-access delay as determined by t_{AVQV}, t_{ELQV}, and t_{GLQV} (whichever is satisfied last) of the flash device. t_{APA} is specified in the flash device's data sheet, and is the address-to-data delay for subsequent page-mode reads.

7.1 Read Specifications

Table 10: Read Operations (Sheet 1 of 2)

Asynchronous Specifications V_{CC} = 2.7 V–3.6 V (3) and V_{CCQ} = 2.7 V–3.6 V(3)							
#	**Sym**	**Parameter**	**Density**	**Min**	**Max**	**Unit**	**Notes**
R1	t_{AVAV}	Read/Write Cycle Time	32 Mbit	75		ns	1,2
			64 Mbit	75			1,2
			128 Mbit	75			1,2
			256 Mbit	95			1,2

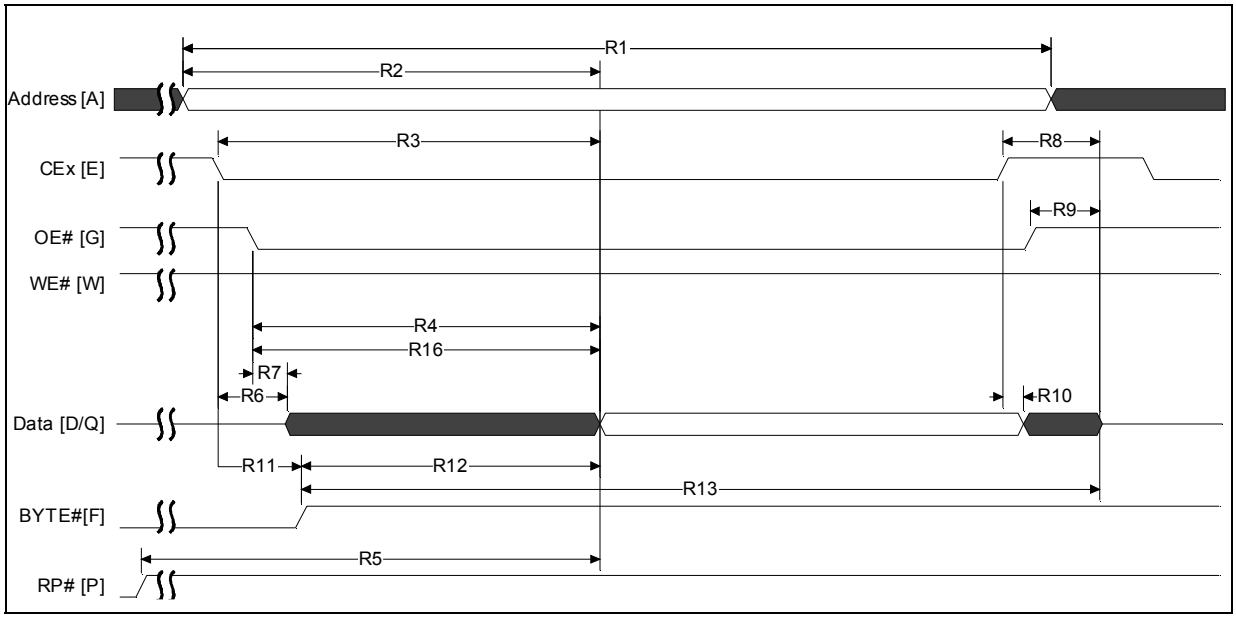
Table 10: Read Operations (Sheet 2 of 2)

Asynchronous Specifications V_{CC} = 2.7 V–3.6 V (3) and V_{CCQ} = 2.7 V–3.6 V(3)							
#	**Sym**	**Parameter**	**Density**	**Min**	**Max**	**Unit**	**Notes**
R2	t_{AVQV}	Address to Output Delay	32 Mbit		75	ns	1,2
			64 Mbit		75		1,2
			128 Mbit		75		1,2
			256 Mbit		95		1,2
R3	t_{ELQV}	CEx to Output Delay	32 Mbit		75	ns	1,2
			64 Mbit		75		1,2
			128 Mbit		75		1,2
			256 Mbit		95		1,2
R4	t_{GLQV}	OE# to Non-Array Output Delay	All		25	ns	1,2,4
R5	t_{PHQV}	RP# High to Output Delay	32 Mbit		150	ns	1,2
			64 Mbit		180		1,2
			128 Mbit		210		1,2
			256 Mbit		210		1,2
R6	t_{ELQX}	CEx to Output in Low Z	All	0		ns	1,2,5
R7	t_{GLQX}	OE# to Output in Low Z		0		ns	1,2,5
R8	t_{EHQZ}	CEx High to Output in High Z			25	ns	1,2,5
R9	t_{GHQZ}	OE# High to Output in High Z			15	ns	1,2,5
R10	t_{OH}	Output Hold from Address, CEx, or OE# Change, Whichever Occurs First		0		ns	1,2,5
R11	t_{ELFL}/t_{ELFH}	CEx Low to BYTE# High or Low			10	ns	1,2,5
R12	t_{FLQV}/t_{FHQV}	BYTE# to Output Delay			1	µs	1,2
R13	t_{FLQZ}	BYTE# to Output in High Z			1	µs	1,2,5
R14	t_{EHEL}	CEx High to CEx Low	All	0		ns	1,2,5
R15	t_{APA}	Page Address Access Time			25	ns	5, 6
R16	t_{GLQV}	OE# to Array Output Delay	All		25	ns	1,2,4

Notes:

1. CE_X low is defined as the first edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined as the first edge of CE0, CE1, or CE2 that disables the device (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31).
2. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.
3. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the first edge of CE0, CE1, or CE2 that enables the device (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31) without impact on t_{ELQV}.
4. See Figure 15, "AC Input/Output Reference Waveform" on page 30 and Figure 16, "Transient Equivalent Testing Load Circuit" on page 30 for testing characteristics.
5. Sampled, not 100% tested.
6. For devices configured to standard word/byte read mode, R15 (t_{APA}) will equal R2 (t_{AVQV}).

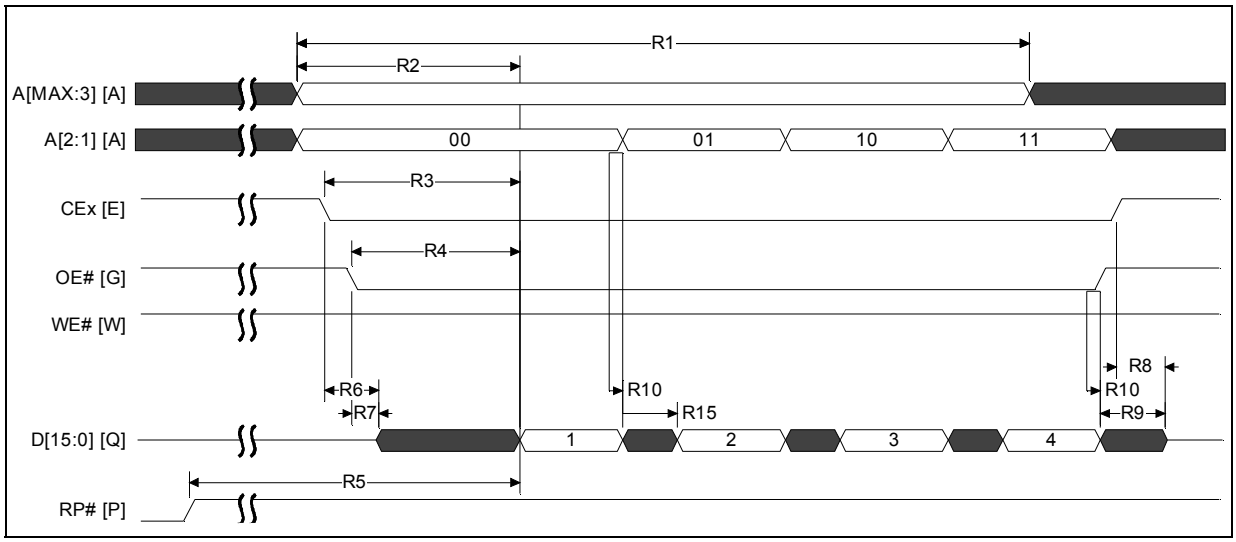
Figure 9: Single Word Asynchronous Read Waveform



Notes:

1. CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined as the first edge of CE0, CE1, or CE2 that disables the device (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31).
2. When reading the flash array a faster t_{GLQV} (R16) applies. For non-array reads, R4 applies (i.e., Status Register reads, query reads, or device identifier reads).

Figure 10: 4-Word Asynchronous Page Mode Read Waveform



Note: CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined as the first edge of CE0, CE1, or CE2 that disables the device (see Table 16, "Chip Enable Truth Table for 32-, 64-, 128- and 256-Mb" on page 31).