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Intel® Advanced+ Boot Block Flash Memory (C3)

28F800C3, 28F160C3, 28F320C3, 28F640C3 (x16)

Datasheet

Product Features

- **Flexible SmartVoltage Technology**
  - —2.7 V– 3.6 V Read/Program/Erase
  - —12 V for Fast Production Programming
- **1.65 V–2.5 V or 2.7 V–3.6 V I/O Option**
  - —Reduces Overall System Power
- **High Performance**
  - —2.7 V– 3.6 V: 70 ns Max Access Time
- **Optimized Architecture for Code Plus Data Storage**
  - —Eight 4 Kword Blocks, Top or Bottom Parameter Boot
  - —Up to One Hundred-Twenty-Seven 32 Kword Blocks
  - —Fast Program Suspend Capability
  - —Fast Erase Suspend Capability
- **Flexible Block Locking**
  - —Lock/Unlock Any Block
  - —Full Protection on Power-Up
  - —WP# Pin for Hardware Block Protection
- **Low Power Consumption**
  - —9 mA Typical Read
  - —7 A Typical Standby with Automatic Power Savings Feature (APS)
- **Extended Temperature Operation**
  - —–40 °C to +85 °C
- **128-bit Protection Register**
  - —64 bit Unique Device Identifier
  - —64 bit User Programmable OTP Cells
- **Extended Cycling Capability**
  - —Minimum 100,000 Block Erase Cycles
- **Software**
  - —Intel® Flash Data Integrator (FDI)
  - —Supports Top or Bottom Boot Storage, Streaming Data (e.g., voice)
  - —Intel Basic Command Set
  - —Common Flash Interface (CFI)
- **Standard Surface Mount Packaging**
  - —48-Ball µBGA*/VFBGA
  - —64-Ball Easy BGA Packages
  - —48-Lead TSOP Package
- **ETOX™ VIII (0.13 µm) Flash Technology**
  - —16, 32 Mbit
- **ETOX™ VII (0.18 µm) Flash Technology**
  - —16, 32, 64 Mbit
- **ETOX™ VI (0.25 µm) Flash Technology**
  - —8, 16 and 32 Mbit

The Intel® Advanced+ Book Block Flash Memory (C3) device, manufactured on Intel's latest 0.13 µm and 0.18 µm technologies, represents a feature-rich solution for low-power applications. The C3 device incorporates low-voltage capability (3 V read, program, and erase) with high-speed, low-power operation. Flexible block locking allows any block to be independently locked or unlocked. Add to this the Intel® Flash Data Integrator (FDI) software and you have a cost-effective, flexible, monolithic code plus data storage solution. Intel® Advanced+ Boot Block Flash Memory (C3) products will be available in 48-lead TSOP, 48-ball CSP, and 64-ball Easy BGA packages. Additional information on this product family can be obtained by accessing the Intel® Flash website: http://www.intel.com/design/flash.

Notice: This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 290645-017
October 2003

Contents

Revision History

Date of Revision	Version	Description
05/12/98	-001	Original version
07/21/98	-002	48-Lead TSOP package diagram change µBGA package diagrams change 32-Mbit ordering information change (Section 6) CFI Query Structure Output Table Change (Table C2) CFI Primary-Vendor Specific Extended Query Table Change for Optional Features and Command Support change (Table C8) Protection Register Address Change I_{PPD} test conditions clarification (Section 4.3) µBGA package top side mark information clarification (Section 6)
10/03/98	-003	Byte-Wide Protection Register Address change V_{IH} Specification change (Section 4.3) V_{IL} Maximum Specification change (Section 4.3) I_{CCS} test conditions clarification (Section 4.3) Added Command Sequence Error Note (Table 7) Datasheet renamed from *3 Volt Advanced Boot Block, 8-, 16-, 32-Mbit Flash Memory Family.*
12/04/98	-004	Added t_{BHWH}/t_{BHEH} and t_{QVBL} (Section 4.6) Programming the Protection Register clarification (Section 3.4.2)
12/31/98	-005	Removed all references to x8 configurations
02/24/99	-006	Removed reference to 40-Lead TSOP from front page
06/10/99	-007	Added Easy BGA package (Section 1.2) Removed 1.8 V I/O references *Locking Operations Flowchart* changed (Appendix B) Added t_{WHGL} (Section 4.6) CFI Primary Vendor-Specific Extended Query changed (Appendix C)
03/20/00	-008	Max I_{CCD} changed to 25 µA Table 10, added note indicating V_{CC}Max = 3.3 V for 32-Mbit device
04/24/00	-009	Added specifications for 0.18 micron product offerings throughout document Added 64-Mbit density
10/12/00	-010	Changed references of 32Mbit 80ns devices to 70ns devices to reflect the faster product offering. Changed VccMax=3.3V reference to indicate that the affected product is the 0.25µm 32Mbit device. Minor text edits throughout document.
7/20/01	-011	Added 1.8v I/O operation documentation where applicable Added TSOP PCN ‘Pin-1’ indicator information Changed references in 8 x 8 BGA pinout diagrams from ‘GND’ to ‘Vssq’ Added ‘Vssq’ to Pin Descriptions Information Removed 0.4 µm references in DC characteristics table Corrected 64Mb package Ordering Information from 48-uBGA to 48-VFBGA Corrected ‘bottom’ parameter block sizes to on 8Mb device to 8 x 4KWords Minor text edits throughout document
10/02/01	-012	Added specifications for 0.13 micron product offerings throughout document
2/05/02	-013	Corrected Iccw / Ippw / Icces /Ippes values. Added mechanicals for 16Mb and 64Mb Minor text edits throughout document.

Date of Revision	Version	Description
4/05/02	-014	Updated 64Mb product offerings. Updated 16Mb product offerings. Revised and corrected DC Characteristics Table. Added mechanicals for Easy BGA. Minor text edits throughout document.
3/06/03	-016	Complete technical update.
10/03	-017	Corrected information in the Device Geometry Details table, address 0x34.

1.0 Introduction

1.1 Document Purpose

This datasheet contains the specifications for the Intel® Advanced+ Boot Block Flash Memory (C3) device family. These flash memories add features such as instant block locking and protection registers that can be used to enhance the security of systems.

1.2 Nomenclature

0x	Hexadecimal prefix
0b	Binary prefix
Byte	8 bits
Word	16 bits
Kword	1024 words
Mword	1,048,576 words
Kb	1024 bits
KB	1024 bytes
Mb	1,048,576 bits
MB	1,048,576 bytes
APS	Automatic Power Savings
CUI	Command User Interface
OTP	One Time Programmable
PR	Protection Register
PRD	Protection Register Data
PLR	Protection Lock Register
RFU	Reserved for Future Use
SR	Status Register
SRD	Status Register Data
WSM	Write State Machine

1.3 Conventions

The terms **pin** and **signal** are often used interchangeably to refer to the external signal connections on the package. (*ball* is the term used for CSP).

Group Membership Brackets: Square brackets will be used to designate group membership or to define a group of signals with similar function (i.e. A[21:1], SR[4:1])

Set: When referring to registers, the term set means the bit is a logical 1.

Clear: When referring to registers, the term clear means the bit is a logical 0.

Block: A group of bits (or words) that erase simultaneously with one block erase instruction.

Main Block: A block that contains 32 Kwords.

Parameter Block: A block that contains 4 Kwords.

2.0 Device Description

This section provides an overview of the Intel® Advanced+ Boot Block Flash Memory (C3) device features, packaging, signal naming, and device architecture.

2.1 Product Overview

The C3 device provides high-performance asynchronous reads in package-compatible densities with a 16 bit data bus. Individually-erasable memory blocks are optimally sized for code and data storage. Eight 4 Kword parameter blocks are located in the boot block at either the top or bottom of the device's memory map. The rest of the memory array is grouped into 32 Kword main blocks.

The device supports read-array mode operations at various I/O voltages (1.8 V and 3 V) and erase and program operations at 3 V or 12 V VPP. With the 3 V I/O option, VCC and VPP can be tied together for a simple, ultra-low-power design. In addition to I/O voltage flexibility, the dedicated VPP input provides complete data protection when $V_{PP} \leq V_{PPLK}$.

The device features a 128-bit protection register enabling security techniques and data protection schemes through a combination of factory-programmed and user-programmable OTP data registers. Zero-latency locking/unlocking on any memory block provides instant and complete protection for critical system code and data. Additional block lock-down capability provides hardware protection where software commands alone cannot change the block's protection status.

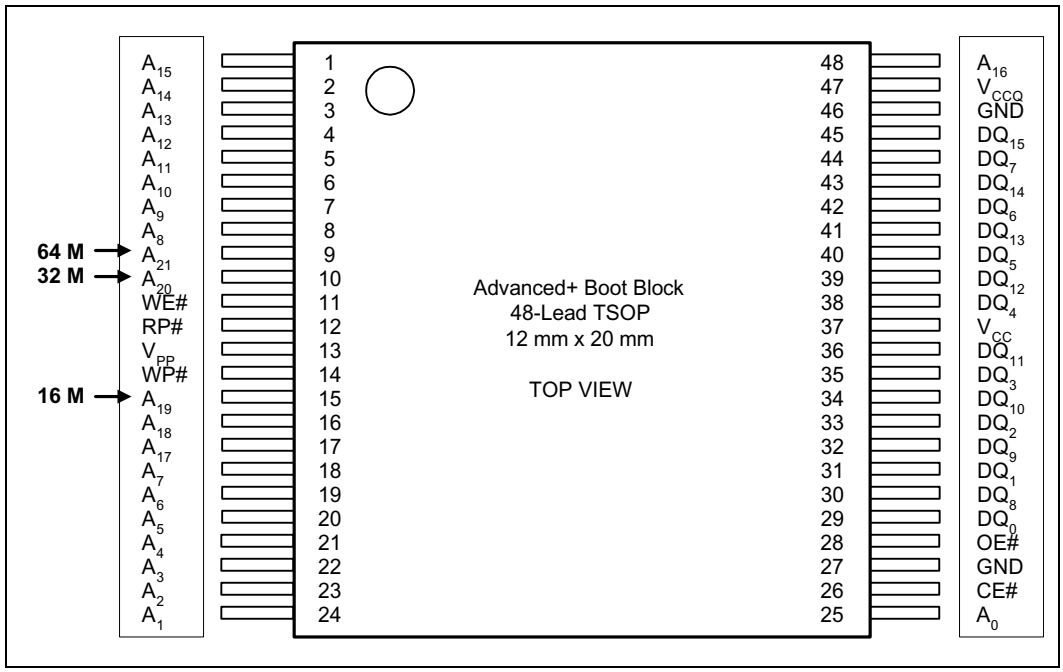
A command User Interface(CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence issued to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

The device offers three low-power saving features: Automatic Power Savings (APS), standby mode, and deep power-down mode. The device automatically enters APS mode following read cycle completion. Standby mode begins when the system deselects the flash memory by deasserting CE#. The deep power-down mode begins when RP# is asserted, which deselects the memory and places the outputs in a high-impedance state, producing ultra-low power savings. Combined, these three power-savings features significantly enhanced power consumption flexibility.

2.2 Ballout Diagram

The C3 device is available in 48-lead TSOP, 48-ball VF BGA, 48-ball µBGA, and Easy BGA packages. (Refer to Figure 1 on page 9, Figure 3 on page 11, and Figure 4 on page 12, respectively.)

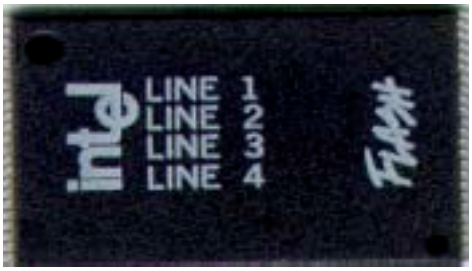
Figure 1. 48-Lead TSOP Package



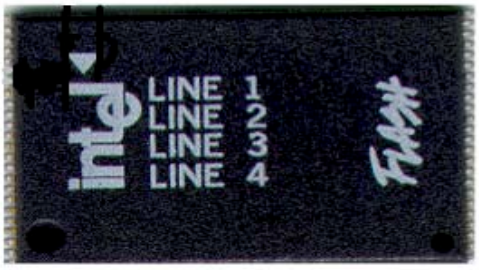
NOTES:
1. For lower densities, upper address should be treated as NC. For example, a 16-Mbit device will have NC on Pins 9 and 10.

Figure 2. Mark for Pin-1 indicator on 48-Lead 8Mb, 16Mb and 32Mb TSOP

Current Mark:



New Mark:

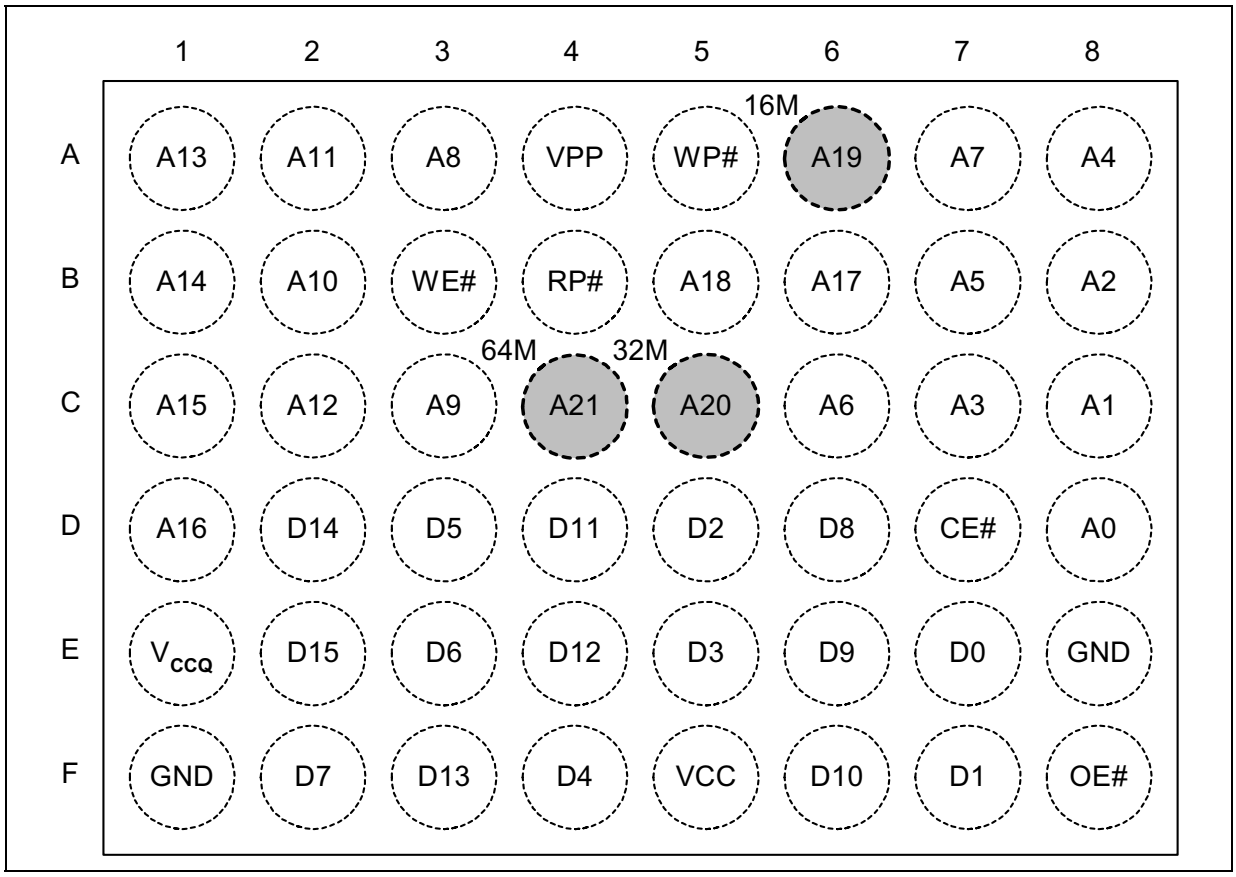


Note: The topside marking on 8 Mb, 16 Mb, and 32 Mb Intel® Advanced and Advanced + Boot Block 48L TSOP products will convert to a white ink triangle as a Pin 1 indicator. Products without the white triangle will continue to use a dimple as a Pin 1 indicator. There are no other changes in package size, materials, functionality, customer handling, or manufacturability. Product will continue to meet Intel stringent quality requirements. Products affected are Intel Ordering Codes shown in Table 1.

Table 1. 48-Lead TSOP

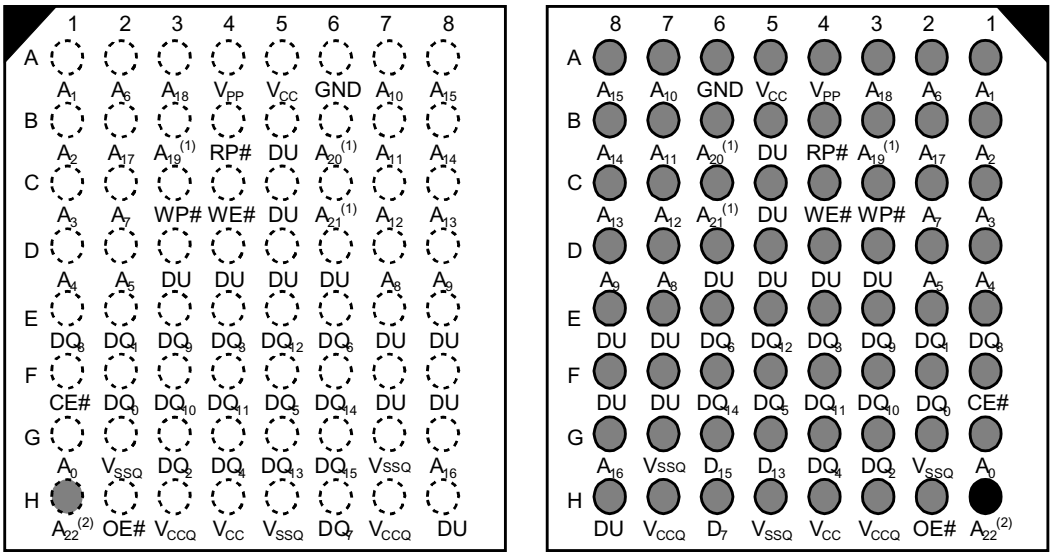
Extended 64 Mbit	Extended 32 Mbit	Extended 16 Mbit	Extended 8 Mbit
TE28F640C3TC80 TE28F640C3BC80	TE28F320C3TD70 TE28F320C3BD70 TE28F320C3TC70 TE28F320C3BC70 TE28F320C3TC90 TE28F320C3BC90 TE28F320C3TA100 TE28F320C3BA100 TE28F320C3TA110 TE28F320C3BA110	TE28F160C3TD70 TE28F160C3BD70 TE28F160C3TC80 TE28F160C3BC80 TE28F160C3TA90 TE28F160C3BA90 TE28F160C3TA110 TE28F160C3BA110	TE28F800C3TA90 TE28F800C3BA90 TE28F800C3TA110 TE28F800C3BA110

Figure 3. 48-Ball µBGA* and 48-Ball Very Fine Pitch BGA (VF BGA) Chip Size Package (Top View, Ball Down)[1,2,3]



NOTES:
1. Shaded connections indicate the upgrade address connections. Routing is not recommended in this area.
2. A19 denotes 16 Mbit; A20 denotes 32 Mbit; A21 denotes 64 Mbit.
3. Unused address balls are not populated.

Figure 4. 64-Ball Easy BGA Package[1,2]



Top View - Ball Side

Bottom View - Ball Side

NOTES:
1. A19 denotes 16 Mbit; A20 denotes 32 Mbit; A21 denotes 64 Mbit.
2. Unused address balls are not populated.

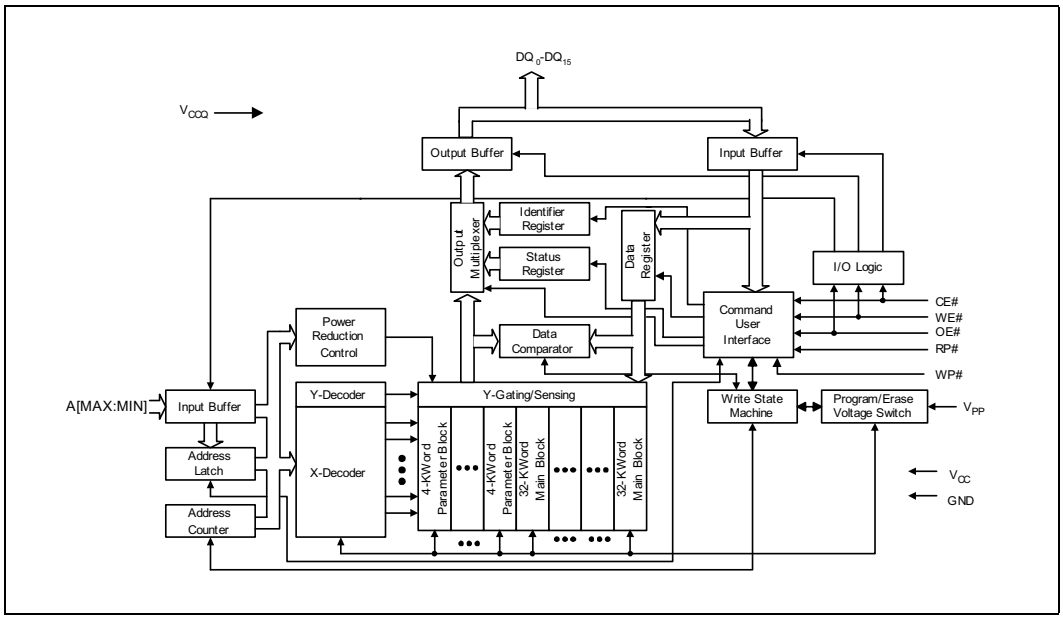
2.3 Signal Descriptions

Table 2 lists the active signals used and provides a brief description of each.

Table 2. Signal Descriptions

Symbol	Type	Name and Function
A[MAX:0]	INPUT	**ADDRESS INPUTS** for memory addresses. Address are internally latched during a program or erase cycle. 8 Mbit: AMAX= A18 16 Mbit: AMAX = A19 32 Mbit: AMAX = A20 64 Mbit: AMAX = A21
DQ[15:0]	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs data and commands during a write cycle; outputs data during read cycles. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
CE#	INPUT	**CHIP ENABLE:** Active-low input. Activates the internal control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels.
OE#	INPUT	**OUTPUT ENABLE:** Active-low input. Enables the device's outputs through the data buffers during a Read operation.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Active-low input. When RP# is at logic low, the device is in reset/deep power-down mode, which drives the outputs to High-Z, resets the Write State Machine, and minimizes current levels (I_{CCD}). When RP# is at logic high, the device is in standard operation. When RP# transitions from logic-low to logic-high, the device resets all blocks to locked and defaults to the read array mode.
WE#	INPUT	**WRITE ENABLE:** Active-low input. WE# controls writes to the device. Address and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	**WRITE PROTECT:** Active-low input. When WP# is a logic low, the lock-down mechanism is enabled and blocks marked lock-down cannot be unlocked through software. When WP# is logic high, the lock-down mechanism is disabled and blocks previously locked-down are now locked and can be unlocked and locked through software. After WP# goes low, any blocks previously marked lock-down revert to the lock-down state. See Section 5.0, "Security Modes" on page 27 for details on block locking.
VPP	INPUT/ POWER	**PROGRAM/ERASE POWER SUPPLY:** Operates as an input at logic levels to control complete device protection. Supplies power for accelerated Program and Erase operations in 12 V ± 5% range. This pin cannot be left floating. Lower VPP ≤ VPPLK to protect all contents against Program and Erase commands. Set VPP = VCC for in-system Read, Program and Erase operations. In this configuration, VPP can drop as low as 1.65 V to allow for resistor or diode drop from the system supply. Apply VPP to 12 V ± 5% for faster program and erase in a production environment. Applying 12 V ± 5% to VPP can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the boot blocks. VPP may be connected to 12 V for a total of 80 hours maximum. See Section 5.6 for details on VPP voltage configurations.
VCC	POWER	**DEVICE CORE POWER SUPPLY:** Supplies power for device operations.
VCCQ	POWER	**OUTPUT POWER SUPPLY:** Output-driven source voltage. This ball can be tied directly to V_{CC} if operating within V_{CC} range.
GND	POWER	**GROUND:** For all internal circuitry. All ground inputs must be connected.
DU	-	**DON'T USE:** Do not use this ball. This ball should not be connected to any power supplies, signals or other balls, and must be left floating.
NC	-	**NO CONNECT:** Pin must be left floating.

2.4 Block Diagram



2.5 Memory Map

The C3 device is asymmetrically blocked, which enables system code and data integration within a single flash device. The bulk of the array is divided into 32 Kword main blocks that can store code or data, and 4 Kword boot blocks to facilitate storage of boot code or for frequently changing small parameters. See Table 3, "Top Boot Memory Map" on page 15 and Table 4, "Bottom Boot Memory Map" on page 16 for details.

Table 3. Top Boot Memory Map

Size (KW)	Blk	8-Mbit Memory Addressing (HEX)	Size (KW)	Blk	16-Mbit Memory Addressing (HEX)	Size (KW)	Blk	32-Mbit Memory Addressing (HEX)	Size (KW)	Blk	64-Mbit Memory Addressing (HEX)
4	22	7F000-7FFFF	4	38	FF000-FFFFF	4	70	1FF000-1FFFFF	4	134	3FF000-3FFFFF
4	21	7E000-7EFFF	4	37	FE000-FEFFF	4	69	1FE000-1FEFFF	4	133	3FE000-3FEFFF
4	20	7D000-7DFFF	4	36	FD000-FDFFF	4	68	1FD000-1FDFFF	4	132	3FD000-3FDFFF
4	19	7C000-7CFFF	4	35	FC000-FCFFF	4	67	1FC000-1FCFFF	4	131	3FC000-3FCFFF
4	18	7B000-7BFFF	4	34	FB000-FBFFF	4	66	1FB000-1FBFFF	4	130	3FB000-3FBFFF
4	17	7A000-7AFFF	4	33	FA000-FAFFF	4	65	1FA000-1FAFFF	4	129	3FA000-3FAFFF
4	16	79000-79FFF	4	32	F9000-F9FFF	4	64	1F9000-1F9FFF	4	128	3F9000-3F9FFF
4	15	78000-78FFF	4	31	F8000-F8FFF	4	63	1F8000-1F8FFF	4	127	3F8000-3F8FFF
32	14	70000-77FFF	32	30	F0000-F7FFF	32	62	1F0000-1F7FFF	32	126	3F0000-3F7FFF
32	13	68000-6FFFF	32	29	E8000-EFFFF	32	61	1E8000-1EFFFF	32	125	3E8000-3EFFFF
32	12	60000-67FFF	32	28	E0000-E7FFF	32	60	1E0000-1E7FFF	32	124	3E0000-3E7FFF
32	11	58000-5FFFF	32	27	D8000-DFFFF	32	59	1D8000-1DFFFF	32	123	3D8000-3DFFFF
...	...	...	...	...	...	...	...	...	...	...	...
32	2	10000-17FFF	32	2	10000-17FFF	32	2	10000-17FFF	32	2	10000-17FFF
32	1	8000-0FFFF	32	1	08000-0FFFF	32	1	08000-0FFFF	32	1	08000-0FFFF
32	0	0000-07FFF	32	0	00000-07FFF	32	0	00000-07FFF	32	0	00000-07FFF

Table 4. Bottom Boot Memory Map

Size (KW)	Blk	8-Mbit Memory Addressing (HEX)	Size (KW)	Blk	16-Mbit Memory Addressing (HEX)	Size (KW)	Blk	32-Mbit Memory Addressing (HEX)	Size (KW)	Blk	64-Mbit Memory Addressing (HEX)
32	22	78000-7FFFF	32	38	F8000-FFFFF	32	70	1F8000-1FFFFF	32	134	3F8000-3FFFFF
32	21	70000-77FFF	32	37	F0000-F7FFF	32	69	1F0000-1F7FFF	32	133	3F0000-3F7FFF
32	20	68000-6FFFF	32	36	E8000-EFFFF	32	68	1E8000-1EFFFF	32	132	3E8000-3EFFFF
32	19	60000-67FFF	32	35	E0000-E7FFF	32	67	1E0000-1E7FFF	32	131	3E0000-3E7FFF
...	...	...	...	...	...	...	...	...	.	...	...
32	10	18000-1FFFF	32	10	18000-1FFFF	32	10	18000-1FFFF	32	10	18000-1FFFF
32	9	10000-17FFF	32	9	10000-17FFF	32	9	10000-17FFF	32	9	10000-17FFF
32	8	08000-0FFFF	32	8	08000-0FFFF	32	8	08000-0FFFF	32	8	08000-0FFFF
4	7	07000-07FFF	4	7	07000-07FFF	4	7	07000-07FFF	4	7	07000-07FFF
4	6	06000-06FFF	4	6	06000-06FFF	4	6	06000-06FFF	4	6	06000-06FFF
4	5	05000-05FFF	4	5	05000-05FFF	4	5	05000-05FFF	4	5	05000-05FFF
4	4	04000-04FFF	4	4	04000-04FFF	4	4	04000-04FFF	4	4	04000-04FFF
4	3	03000-03FFF	4	3	03000-03FFF	4	3	03000-03FFF	4	3	03000-03FFF
4	2	02000-02FFF	4	2	02000-02FFF	4	2	02000-02FFF	4	2	02000-02FFF
4	1	01000-01FFF	4	1	01000-01FFF	4	1	01000-01FFF	4	1	01000-01FFF
4	0	00000-00FFF	4	0	00000-00FFF	4	0	00000-00FFF	4	0	00000-00FFF

3.0 Device Operations

The C3 device uses a CUI and automated algorithms to simplify Program and Erase operations. The CUI allows for 100% CMOS-level control inputs and fixed power supplies during erasure and programming.

The internal WSM completely automates Program and Erase operations while the CUI signals the start of an operation and the status register reports device status. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

3.1 Bus Operations

The C3 device performs read, program, and erase operations in-system via the local CPU or microcontroller. Four control pins (CE#, OE#, WE#, and RP#) manage the data flow in and out of the flash device. Table 5 on page 17 summarizes these bus operations.

Table 5. Bus Operations

Mode	RP#	CE#	OE#	WE#	DQ[15:0]
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	High-Z
Standby	V_{IH}	V_{IH}	X	X	High-Z
Reset	V_{IL}	X	X	X	High-Z

NOTE: X = Don't Care (V_{IL} or V_{IH})

3.1.1 Read

When performing a read cycle, CE# and OE# must be asserted; WE# and RP# must be deasserted. CE# is the device selection control; when active low, it enables the flash memory device. OE# is the data output control; when low, data is output on DQ[15:0]. See Figure 8, "Read Operation Waveform" on page 42.

3.1.2 Write

A write cycle occurs when both CE# and WE# are low; RP# and OE# are high. Commands are issued to the Command User Interface (CUI). The CUI does not occupy an addressable memory location. Address and data are latched on the rising edge of the WE# or CE# pulse, whichever occurs first. See Figure 9, "Write Operations Waveform" on page 47.

3.1.3 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. DQ[15:0] are placed in a high-impedance state.

3.1.4 Standby

Deselecting the device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode, which substantially reduces device power consumption without any latency for subsequent read accesses. In standby, outputs are placed in a high-impedance state independent of OE#. If deselected during a Program or Erase operation, the device continues to consume active power until the Program or Erase operation is complete.

3.1.5 Reset

From read mode, RP# at V_{IL} for time t_{PLPH} deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from reset, a time t_{PHQV} is required until the initial read-access outputs are valid. A delay (t_{PHWL} or t_{PHEL}) is required after return from reset before a write cycle can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read-array mode, the status register is set to 0x80, and all blocks are locked. See Figure 10, “Reset Operations Waveforms” on page 48.

If RP# is taken low for time t_{PLPH} during a Program or Erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence:

1. When RP# goes low, the device shuts down the operation in progress, a process which takes time t_{PLRH} to complete.

2. After time t_{PLRH}, the part will either reset to read-array mode (if RP# is asserted during t_{PLRH}) or enter reset mode (if RP# is deasserted after t_{PLRH}). See Figure 10, “Reset Operations Waveforms” on page 48.

In both cases, after returning from an aborted operation, the relevant time t_{PHQV} or t_{PHWL}/t_{PHEL} must be observed before a Read or Write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of t_{PLRH} rather than when RP# goes high.

As with any automated device, it is important to assert RP# during a system reset. When the system comes out of reset, the processor expects to read from the flash memory. Automated flash memories provide status information when read during program or Block-Erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel® Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

4.0 Modes of Operation

4.1 Read Mode

The flash memory has four read modes (read array, read identifier, read status, and CFI query), and two write modes (program and erase). Three additional modes (erase suspend to program, erase suspend to read, and program suspend to read) are available only during suspended operations. Table 7, “Command Bus Operations” on page 24 and Table 8, “Command Codes and Descriptions” on page 25 summarize the commands used to reach these modes. Appendix A, “Write State Machine States” on page 50 is a comprehensive chart showing the state transitions.

4.1.1 Read Array

When RP# transitions from V_{IL} (reset) to V_{IH}, the device defaults to read-array mode and will respond to the read-control inputs (CE#, address inputs, and OE#) without any additional CUI commands.

When the device is in read array mode, four control signals control data output.

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE# must be logic low (V_{IL})
- RP# must be logic high (V_{IH})

In addition, the address of the desired location must be applied to the address pins. If the device is not in read-array mode, as would be the case after a Program or Erase operation, the Read Array command (0xFF) must be issued to the CUI before array reads can occur.

4.1.2 Read Identifier

The read-identifier mode outputs three types of information: the manufacturer/device identifier, the block locking status, and the protection register. The device is switched to this mode by issuing the Read Identifier command (0x90). Once in this mode, read cycles from addresses shown in Table 6 retrieve the specified information. To return to read-array mode, issue the Read Array command (0xFF).

Table 6. Device Identification Codes

Item	Address[1]		Data	Description
	Base	Offset		
Manufacturer ID	Block	0x00	0x0089	
Device ID	Block	0x01	0x88C0	8-Mbit Top Boot Device
			0x88C1	8-Mbit Bottom Boot Device
			0x88C2	16-Mbit Top Boot Device
			0x88C3	16-Mbit Bottom Boot Device
			0x88C4	32-Mbit Top Boot Device
			0x88C5	32-Mbit Bottom Boot Device
			0x88CC	64-Mbit Top Boot Device
			0x88CD	64-Mbit Bottom Boot Device
Block Lock Status[2]	Block	0x02	DQ0 = 0b0	Block is unlocked
			DQ0 = 0b1	Block is locked
Block Lock-Down Status[2]	Block	0x02	DQ1 = 0b0	Block is not locked-down
			DQ1 = 0b1	Block is locked down
Protection Register Lock Status	Block	0x80	Lock Data	
Protection Register	Block	0x81 - 0x88	Register Data	Multiple reads required to read the entire 128-bit Protection Register.

NOTES:
1. The address is constructed from a base address plus an offset. For example, to read the Block Lock Status for block number 38 in a bottom boot device, set the address to 0x0F8000 plus the *offset* (0x02), i.e. 0x0F8002. Then examine DQ0 of the data to determine if the block is locked.
2. See Section 5.2, "Reading Block-Lock Status" on page 28 for valid lock status.

4.1.3 CFI Query

The CFI query mode outputs Common Flash Interface (CFI) data after issuing the Read Query Command (0x98). The CFI data structure contains information such as block size, density, command set, and electrical specifications. Once in this mode, read cycles from addresses shown in Appendix C, "Common Flash Interface," retrieve the specified information. To return to read-array mode, issue the Read Array command (0xFF).

4.1.4 Read Status Register

The status register indicates the status of device operations, and the success/failure of that operation. The Read Status Register (0x70) command causes subsequent reads to output data from the status register until another command is issued. To return to reading from the array, issue a Read Array (0xFF) command.

The status-register bits are output on DQ[7:0]. The upper byte, DQ[15:8], outputs 0x00 when a Read Status Register command is issued.

The contents of the status register are latched on the falling edge of OE# or CE# (whichever occurs last) which prevents possible bus errors that might occur if Status Register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the Status Register will not indicate completion of a Program or Erase operation.

When the WSM is active, SR[7] will indicate the status of the WSM; the remaining bits in the status register indicate whether the WSM was successful in performing the preferred operation (see Table 9, "Status Register Bit Definition" on page 26).

4.1.4.1 Clear Status Register

The WSM can set Status Register bits 1 through 7 and can clear bits 2, 6, and 7; but, the WSM cannot clear Status Register bits 1, 3, 4 or 5. Because bits 1, 3, 4, and 5 indicate various error conditions, these bits can be cleared only through the Clear Status Register (0x50) command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the status register to determine if an error occurred during that series. Clear the status register before beginning another command or sequence. The Read Array command must be issued before data can be read from the memory array. Resetting the device also clears the Status Register.

4.2 Program Mode

Programming is executed using a two-write cycle sequence. The Program Setup command (0x40) is issued to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to program preferred bits of the addressed location, then verify the bits are sufficiently programmed. Programming the memory results in specific bits within an address location being changed to a "0." If users attempt to program "1"s, the memory cell contents do not change and no error occurs.

The Status Register indicates programming status. While the program sequence executes, status bit 7 is "0." The status register can be polled by toggling either CE# or OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the program-status bits should be checked. If the programming operation was unsuccessful, bit SR[4] of the Status Register is set to indicate a program failure. If SR[3] is set, then V_{PP} was not within acceptable limits, and the WSM did not execute the program command. If SR[1] is set, a program operation was attempted on a locked block and the operation was aborted.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent status-register reads, be sure to reset the CUI to read-array mode.

4.2.1 12-Volt Production Programming

When V_{PP} is between 1.65 V and 3.6 V, all program and erase current is drawn through the VCC pin. Note that if V_{PP} is driven by a logic signal, V_{IH} min = 1.65 V. That is, V_{PP} must remain above 1.65 V to perform in-system flash modifications. When V_{PP} is connected to a 12 V power supply, the device draws program and erase current directly from the VPP pin. This eliminates the need for an external switching transistor to control V_{PP}. Figure 7 on page 31 shows examples of how the flash power supplies can be configured for various usage models.

The 12 V V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to VPP during Program and Erase operations for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. VPP may be connected to 12 V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

4.2.2 Suspending and Resuming Program

The Program Suspend command halts an in-progress program operation so that data can be read from other locations of memory. Once the programming process starts, issuing the Program Suspend command to the CUI requests that the WSM suspend the program sequence at predetermined points in the program algorithm. The device continues to output status-register data after the Program Suspend command is issued. Polling status-register bits SR[7] and SR[2] will determine when the program operation has been suspended (both will be set to "1"). t_{WHRH1}/ t_{EHRH1} specify the program-suspend latency.

A Read-Array command can now be issued to the CUI to read data from blocks other than that which is suspended. The only other valid commands while program is suspended are Read Status Register, Read Identifier, CFI Query, and Program Resume.

After the Program Resume command is issued to the flash memory, the WSM will continue with the programming process and status register bits SR[2] and SR[7] will automatically be cleared. The device automatically outputs status register data when read (see Figure 14, "Program Suspend / Resume Flowchart" on page 53) after the Program Resume command is issued. V_{PP} must remain at the same V_{PP} level used for program while in program-suspend mode. RP# must also remain at V_{IH}.

4.3 Erase Mode

To erase a block, issue the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1." Only one block can be erased at a time. The WSM will execute a sequence of internally timed events to program all bits within the block to "0," erase all bits within the block to "1," then verify that all bits within the block are sufficiently erased. While the erase executes, status bit 7 is a "0."

When the status register indicates that erasure is complete, check the erase-status bit to verify that the Erase operation was successful. If the Erase operation was unsuccessful, SR[5] of the status register will be set to a "1," indicating an erase failure. If V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR[5] of the status register is set to indicate an erase error, and SR[3] is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits.

After an Erase operation, clear the status register (0x50) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status-register reads, it is advisable to place the flash in read-array mode after the erase is complete.

4.3.1 Suspending and Resuming Erase

Since an Erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from—or program data to—another block in memory. Once the erase sequence is started, issuing the Erase Suspend command to the CUI suspends the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the Erase operation has been suspended. Erase-suspend latency is specified by t_{WHRH2}/t_{EHRH2}.

A Read Array or Program command can now be issued to the CUI to read/program data from/to blocks other than that which is suspended. This nested Program command can subsequently be suspended to read yet another location. The only valid commands while Erase is suspended are Read Status Register, Read Identifier, CFI Query, Program Setup, Program Resume, Erase Resume, Lock Block, Unlock Block, and Lock-Down Block. During erase-suspend mode, the chip can be placed in a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current consumption.

Erase Resume continues the erase sequence when CE# = V_{IL}. Similar to the end of a standard Erase operation, the status register should be read and cleared before the next instruction is issued.

Table 7. Command Bus Operations

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array	1,3	Write	X	0xFF			
Read Identifier	1,3	Write	X	0x90	Read	IA	ID
CFI Query	1,3	Write	X	0x98	Read	QA	QD
Read Status Register	1,3	Write	X	0x70	Read	X	SRD
Clear Status Register	1,3	Write	X	0x50			
Program	2,3	Write	X	0x40/ 0x10	Write	PA	PD
Block Erase/Confirm	1,3	Write	X	0x20	Write	BA	D0H
Program/Erase Suspend	1,3	Write	X	0xB0			
Program/Erase Resume	1,3	Write	X	0xD0			
Lock Block	1,3	Write	X	0x60	Write	BA	0x01
Unlock Block	1,3	Write	X	0x60	Write	BA	0xD0
Lock-Down Block	1,3	Write	X	0x60	Write	BA	0x2F
Protection Program	1,3	Write	X	0xC0	Write	PA	PD

X = "Don't Care"	PA = Prog Addr	BA = Block Addr	IA = Identifier Addr.	QA = Query Addr.
SRD = Status Reg. Data	PD = Prog Data		ID = Identifier Data	QD = Query Data

NOTES:
1. Following the Read Identifier or CFI Query commands, read operations output device identification data or CFI query information, respectively. See Section 4.1.2 and Section 4.1.3.
2. Either 0x40 or 0x10 command is valid, but the Intel standard is 0x40.
3. When writing commands, the upper data bus [DQ8-DQ15] should be either V_{IL} or V_{IH}, to minimize current draw.

Bus operations are defined in Table 5, "Bus Operations" on page 17.

Table 8. Command Codes and Descriptions

Code (HEX)	Device Mode	Command Description
FF	Read Array	This command places the device in read-array mode, which outputs array data on the data pins.
40	Program Set-Up	This is a two-cycle command. The first cycle prepares the CUI for a program operation. The second cycle latches addresses and data information and initiates the WSM to execute the Program algorithm. The flash outputs status-register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 4.2, “Program Mode” on page 21.
20	Erase Set-Up	This is a two-cycle command. Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will (a) set both SR.4 and SR.5 of the status register to a “1,” (b) place the device into the read-status-register mode, and (c) wait for another command. See Section 4.3, “Erase Mode” on page 22.
D0	Erase Confirm Program/Erase Resume Unlock Block	If the previous command was an Erase Set-Up command, then the CUI will close the address and data latches and begin erasing the block indicated on the address pins. During program/erase, the device will respond only to the Read Status Register, Program Suspend and Erase Suspend commands, and will output status-register data when CE# or OE# is toggled. If a Program or Erase operation was previously suspended, this command will resume that operation. If the previous command was Block Unlock Set-Up, the CUI will latch the address and unlock the block indicated on the address pins. If the block had been previously set to Lock-Down, this operation will have no effect. (See Section 5.1)
B0	Program Suspend Erase Suspend	Issuing this command will begin to suspend the currently executing Program/Erase operation. The status register will indicate when the operation has been successfully suspended by setting either the program-suspend SR[2] or erase-suspend SR[6] and the WSM status bit SR[7] to a “1” (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input-control pins except RP#, which will immediately shut down the WSM and the remainder of the chip if RP# is driven to V_{IL}. See Sections 3.2.5.1 and 3.2.6.1.
70	Read Status Register	This command places the device into read-status-register mode. Reading the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after a Program or Erase operation has been initiated. See Section 4.1.4, “Read Status Register” on page 20.
50	Clear Status Register	The WSM can set the block-lock status SR[1], V_{PP} Status SR[3], program status SR[4], and erase-status SR[5] bits in the status register to “1,” but it cannot clear them to “0.” Issuing this command clears those bits to “0.”
90	Read Identifier	Puts the device into the read-identifier mode so that reading the device will output the manufacturer/device codes or block-lock status. See Section 4.1.2, “Read Identifier” on page 19.
60	Block Lock, Block Unlock, Block Lock-Down Set-Up	Prepares the CUI for block-locking changes. If the next command is not Block Unlock, Block Lock, or Block Lock-Down, then the CUI will set both the program and erase-status-register bits to indicate a command-sequence error. See Section 5.0, “Security Modes” on page 27.
01	Lock-Block	If the previous command was Lock Set-Up, the CUI will latch the address and lock the block indicated on the address pins. (See Section 5.1)
2F	Lock-Down	If the previous command was a Lock-Down Set-Up command, the CUI will latch the address and lock-down the block indicated on the address pins. (See Section 5.1)
98	CFI Query	Puts the device into the CFI-Query mode so that reading the device will output Common Flash Interface information. See Section 4.1.3 and Appendix C, “Common Flash Interface”.
C0	Protection Program Set-Up	This is a two-cycle command. The first cycle prepares the CUI for a program operation to the protection register. The second cycle latches addresses and data information and initiates the WSM to execute the Protection Program algorithm to the protection register. The flash outputs status-register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 5.5.