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Numonyx™ StrataFlash® Embedded Memory (J3-65nm)

256-Mbit

Datasheet

Product Features

- Architecture
  - — Multi-Level Cell Technology: Highest Density at Lowest Cost
  - — 256 symmetrically-sized blocks of 128 Kbytes
- Performance
  - — 95 ns initial access time for Easy BGA
  - — 105 ns initial accsss time for TSOP
  - — 25 ns 16-word Asynchronous page-mode reads
  - — 512-Word Buffer Programming at 1.46MByte/s (Typ)
- Voltage and Power
  - — V_{CC} (Core) = 2.7 V to 3.6 V
  - — V_{CCQ} (I/O) = 2.7 V to 3.6 V
  - — Standby Current: 65 µA (Typ)
  - — Erase & Program Current: 35 mA (Typ)
  - — Page Read: 12 mA (Typ)
- Quality and Reliability
  - — Operating temperature: -40 °C to +85 °C
  - — 100K Minimum erase cycles per block
  - — 65 nm Numonyx™ ETOX™ X Process technology
- Security
  - — Enhanced security options for code protection
  - — Absolute protection with V_{PEN} = GND
  - — Individual block locking
  - — Block erase/program lockout during power transition
  - — Password Access feature
  - — One-Time Programmable Register: 64 OTP bits, programmed with unique information by Numonyx 64 OTP bits, available for customer programming
- Software
  - — 20 µs (Typ) program suspend
  - — 20 µs (Typ) erase suspend
  - — Numonyx™ Flash Data Integrator (FDI)
  - — Common Flash Interface (CFI) Compatible
- Packaging
  - — 56-Lead TSOP
  - — 64-Ball Easy BGA package

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Contents

1.0 Functional Overview

The Numonyx™ StrataFlash® Embedded Memory (J3-65nm) provides improved mainstream performance with enhanced security features, taking advantage of the high quality and reliability of the NOR-based Numonyx 65 nm ETOX™ X process technology. Offered in 32-Mbit up through 256-Mbit densities, the Numonyx™ Embedded Memory (J3-65nm) device brings reliable, low-voltage capability (3 V read, program, and erase) with high speed, low-power operation. The Numonyx™ StrataFlash® Embedded Memory (J3-65nm) device is ideal for code and data applications where high density and low cost are required, such as in networking, telecommunications, digital set top boxes, audio recording, and digital imaging. Numonyx Flash Memory components also deliver a new generation of forward-compatible software support. By using the Common Flash Interface (CFI) and Scalable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Numonyx Flash Memory devices.

1.1 Document purpose

This document contains information pertaining to the Numonyx™ StrataFlash® Embedded Memory (J3-65nm) device features, operation, and specifications.

The Numonyx™ Embedded Memory (J3-65nm) device is offered in Single Bit Cell technology for 32-, 64-, 128-Mbit densities. The Numonyx™ StrataFlash® Embedded Memory (J3-65nm) device is offered in Multi-Level Cell technology for 256-Mbit density. This document just covers 256-Mbit die information.

Unless otherwise indicated throughout the rest of this document, Numonyx™ StrataFlash® Embedded Memory (J3-65nm) is referred to as J3-65nm.

1.2 Product overview

The 256-Mbit J3-65nm is organized as 256 individual 128Kbyte symmetrical blocks.

A 128-bit Protection Register has multiple uses, including unique flash device identification.

The J3-65nm device includes new security features that were not available on the (previous) 0.25µm, 0.18µm, and 0.13µm versions of the J3 family. The new security features can be implemented to protect critical code and data from unwanted modification (program or erase). Usage can be defined to fit the specific needs of each customer.

The J3-65nm optimized architecture and interface dramatically increases read performance by supporting page-mode reads. This read mode is ideal for non-clock memory systems.

The J3-65nm Common Flash Interface (CFI) permits software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

The Scalable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 128-Kbyte blocks typically within one second, independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or program data from any other block. Similarly, program suspend allows system software to suspend programming (byte/word program and write-to-buffer operations) to read data or execute code from any other block that is not being suspended.

Each device incorporates a Write Buffer of 512 words to allow optimum programming performance. By using the Write Buffer data is programmed more efficiently in buffer increments.

Memory Blocks are selectively and individually lockable in-system. Individual block locking uses block lock-bits to lock and unlock blocks. Block lock-bits gate block erase and program operations. Lock-bit configuration operations set and clear lock-bits (using the Set Block Lock-Bit and Clear Block Lock-Bits commands).

The Status Register indicates when the WSM's block erase, program, or lock-bit configuration operation completes.

The STS (status) output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status indication using STS minimizes both CPU overhead and system power consumption. When configured in level mode (default mode), it acts as a RY/BY# signal. When low, STS indicates that the WSM is performing a block erase, program, or lock-bit configuration. STS-high indicates that the WSM is ready for a new command, block erase is suspended (and programming is inactive), program is suspended, or the device is in reset/power-down mode. Additionally, the configuration command allows the STS signal to be configured to pulse on completion of programming and/or block erases.

Three CE signals are used to enable and disable the device. A unique CE logic design (see Table 6, "Chip Enable Truth Table for 256-Mb" on page 15) reduces decoder logic typically required for multi-chip designs. External logic is not required when designing a single chip, a dual chip, or a 4-chip miniature card or SIMM module.

The BYTE# signal allows either x8 or x16 read/writes to the device:

- BYTE#-low enables 8-bit mode; address A0 selects between the low byte and high byte.
- BYTE#-high enables 16-bit operation; address A1 becomes the lowest order address and address A0 is not used (don't care).

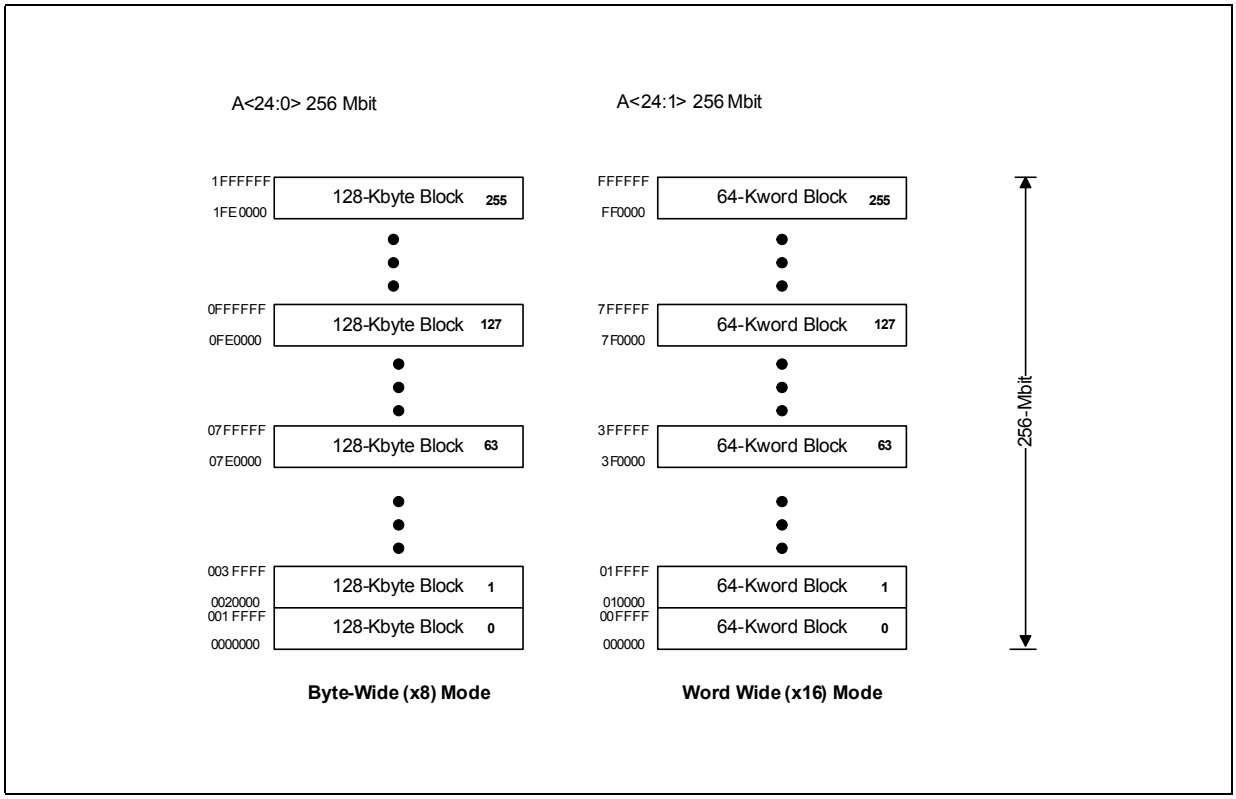
When the device is disabled (see Table 6, "Chip Enable Truth Table for 256-Mb" on page 15), with CEx at V_{IH} and RP# at V_{IH}, the standby mode is enabled. When RP# is at V_{IL}, a further power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# going high until data outputs are valid. Likewise, the device has a wake time (t_{PHWL}) from RP#-high until writes to the CUI are recognized. With RP# at V_{IL}, the WSM is reset and the Status Register is cleared.

1.3 Configuration & Memory Map

The J3-65nm device features a symmetrically-blocked architecture. The flash device main array is divided as follows:

- 256-Mbit, organized into *two-hundred-fifty-six* 128-Kbyte blocks.

Figure 1: J3-65nm Memory Map



1.4 Device ID

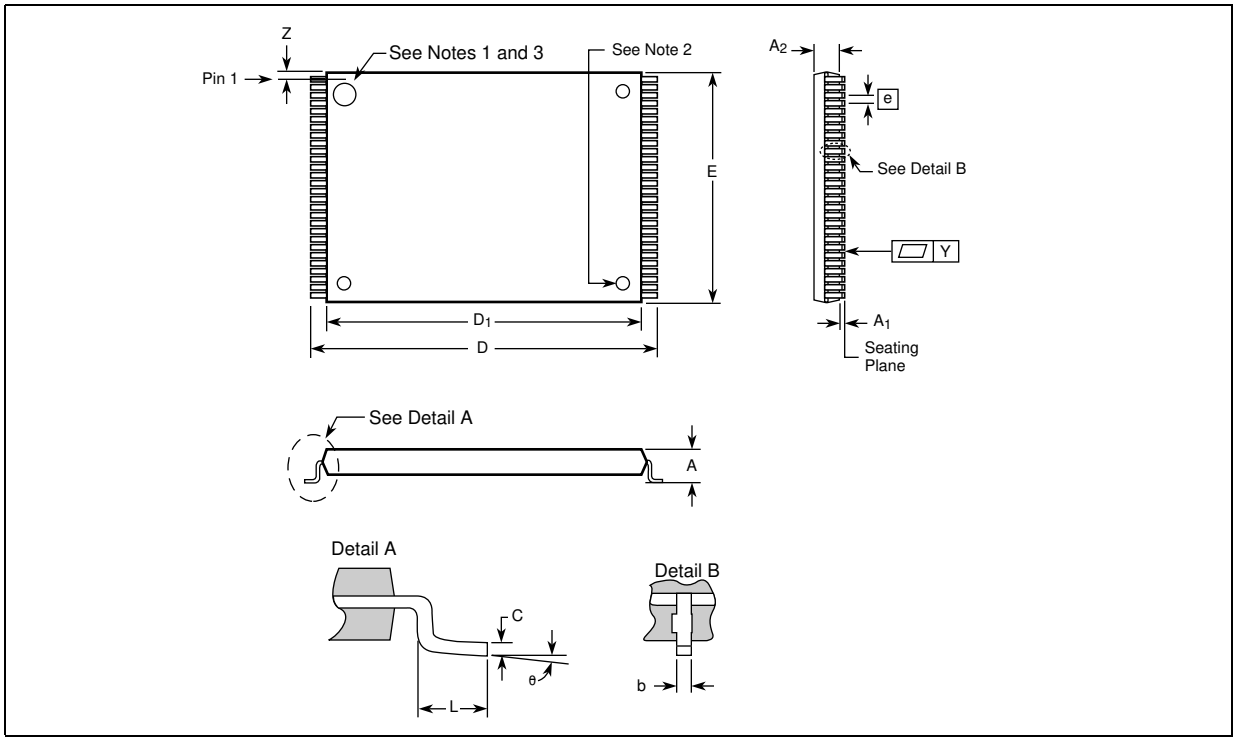
Table 1: Device Identifier Codes

Code		Address	Data
Device Code	256-Mbit	00001h	001Dh

2.0 Package Information

2.1 56-Lead TSOP Package, 256-Mbit

Figure 2: 56-Lead TSOP Package Mechanical



Notes:
1. One dimple on package denotes Pin 1.
2. If two dimples, then the larger dimple denotes Pin 1.
3. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.

Table 2: 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A			1.200			0.047
Standoff	A_1	0.050			0.002		
Package Body Thickness	A_2	0.965	0.995	1.025	0.038	0.039	0.040
Lead Width	b	0.100	0.150	0.200	0.004	0.006	0.008
Lead Thickness	c	0.100	0.150	0.200	0.004	0.006	0.008
Package Body Length	D_1	18.200	18.400	18.600	0.717	0.724	0.732
Package Body Width	E	13.800	14.000	14.200	0.543	0.551	0.559
Lead Pitch	e		0.500			0.0197	

Table 2: 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Terminal Dimension	D	19.800	20.00	20.200	0.780	0.787	0.795
Lead Tip Length	L	0.500	0.600	0.700	0.020	0.024	0.028
Lead Count	N		56			56	
Lead Tip Angle	θ	0°	3°	5°	0°	3°	5°
Seating Plane Coplanarity	Y			0.100			0.004
Lead to Package Offset	Z	0.150	0.250	0.350	0.006	0.010	0.014

2.2 Easy BGA Package, 256-Mbit

Figure 3: Easy BGA Mechanical Specifications

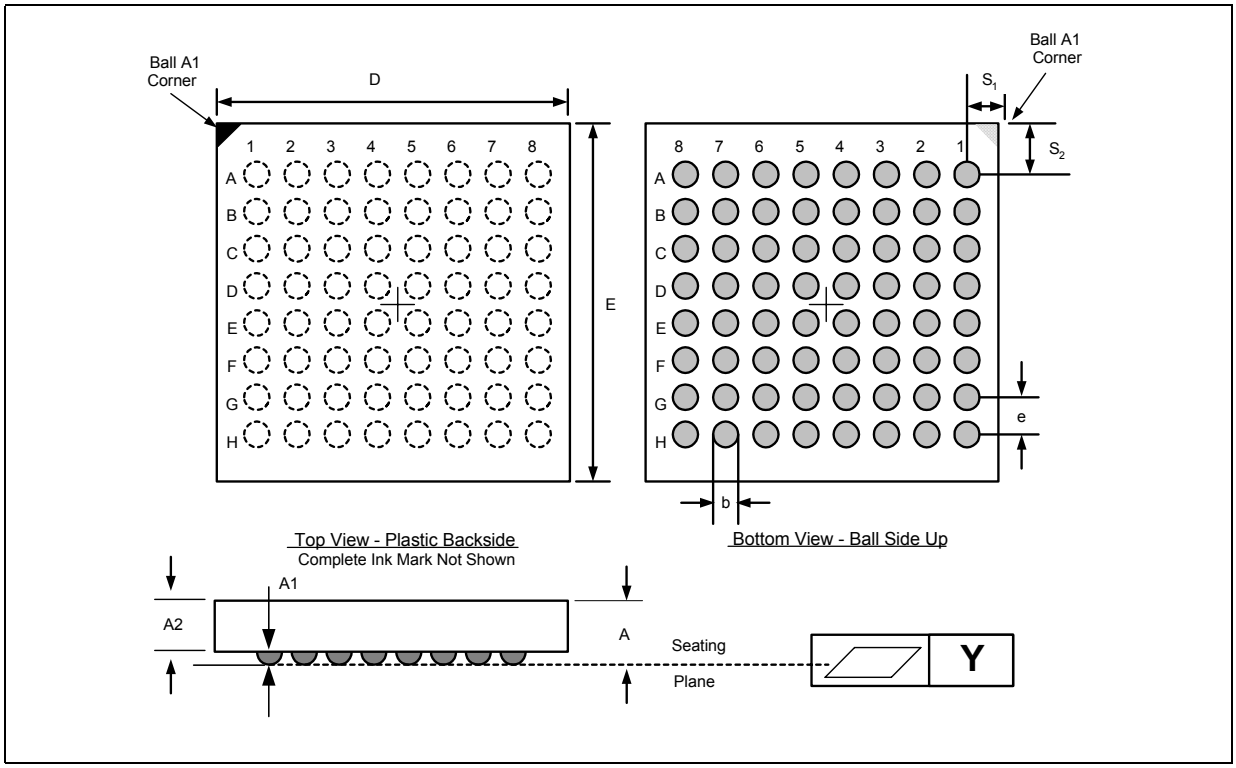


Table 3: Easy BGA Package Dimensions Table

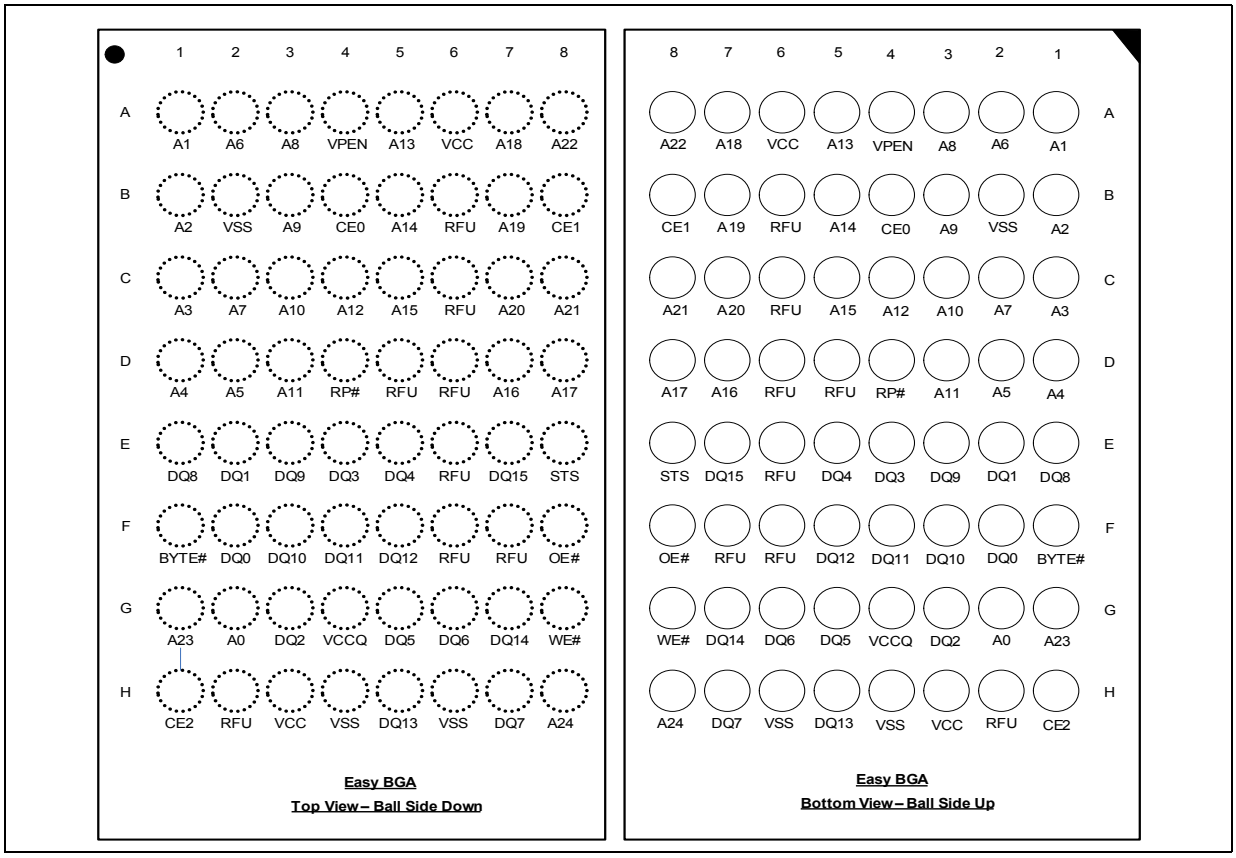
Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height (256 Mbit)	A			1.200			0.0472
Ball Height	A1	0.250			0.0098		
Package Body Thickness (256 Mbit)	A2		0.780			0.0307	
Ball (Lead) Width	b	0.330	0.430	0.530	0.0130	0.0169	0.0209
Package Body Width	D	9.900	10.000	10.100	0.3898	0.3937	0.3976
Package Body Length	E	12.900	13.000	13.100	0.5079	0.5118	0.5157
Pitch	e		1.000			0.0394	
Ball (Lead) Count	N		64			64	
Seating Plane Coplanarity	Y			0.100			0.0039
Corner to Ball A1 Distance Along D (256 Mb)	S1	1.400	1.500	1.600	0.0551	0.0591	0.0630
Corner to Ball A1 Distance Along E (256 Mb)	S2	2.900	3.000	3.100	0.1142	0.1181	0.1220

3.0 Ballout

J3-65nm is available in two package types. All densities of the J3-65nm devices are supported on both 64-ball Easy BGA and 56-lead Thin Small Outline Package (TSOP) packages. The figures below show the ballouts.

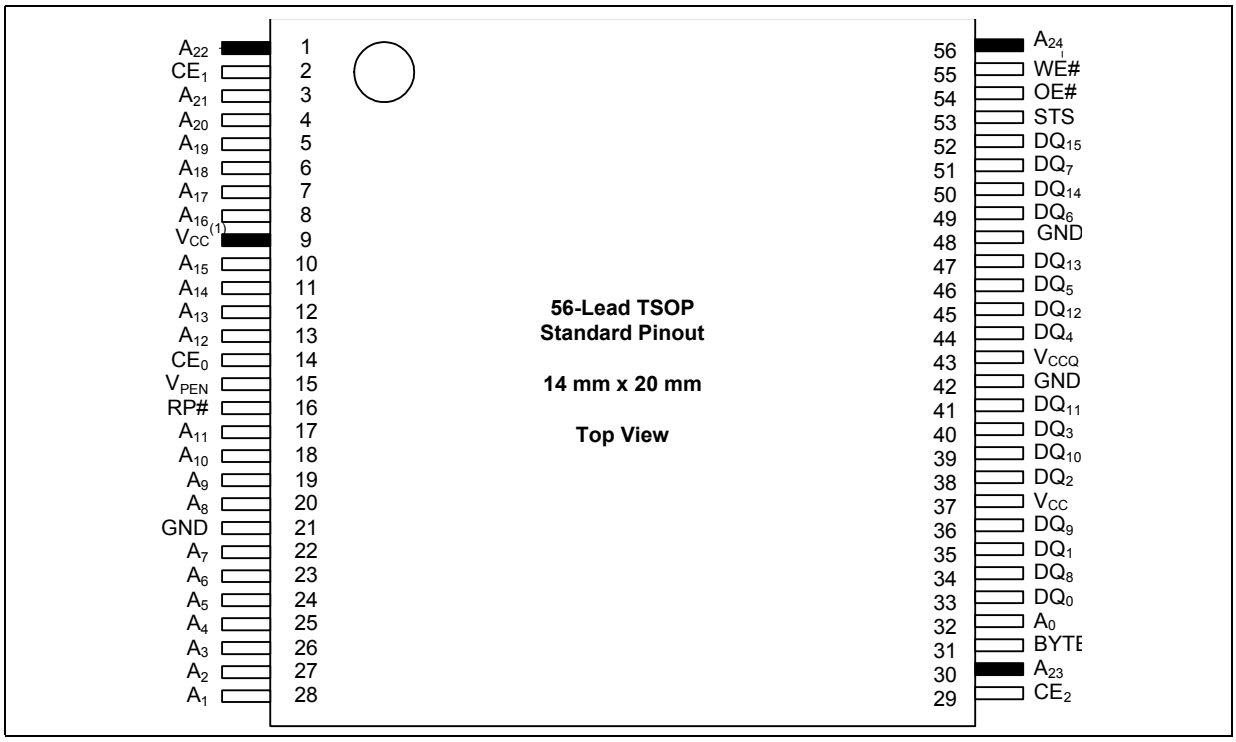
3.1 Easy BGA Ballout

Figure 4: Easy BGA Ballout



3.2 56-Lead TSOP Package Pinout, 256-Mbit

Figure 5: 56-Lead TSOP Package Pinout (256 Mbit)



Notes:
1. No internal connection on Pin 9; it may be driven or floated. For legacy designs, pin can be tied to Vcc.

4.0 Signal Descriptions

Table 4 lists the active signals used on J3-65nm and provides a description of each.

Table 4: TSOP & Easy BGA Signal Descriptions

Symbol	Type	Name and Function
A0	Input	**BYTE-SELECT ADDRESS:** Selects between high and low byte when the device is in x8 mode. This address is latched during a x8 program cycle. Not used in x16 mode (i.e., the A0 input buffer is turned off when BYTE# is high).
A[MAX:1]	Input	**ADDRESS INPUTS:** Inputs for addresses during read and program operations. Addresses are internally latched during a program cycle: 256-Mbit — A[24:1]
DQ[7:0]	Input/ Output	**LOW-BYTE DATA BUS:** Inputs data during buffer writes and programming, and inputs commands during CUI writes. Outputs array, CFI, identifier, or status data in the appropriate read mode. Data is internally latched during write operations.
DQ[15:8]	Input/ Output	**HIGH-BYTE DATA BUS:** Inputs data during x16 buffer writes and programming operations. Outputs array, CFI, or identifier data in the appropriate read mode; not used for Status Register reads. Data is internally latched during write operations in x16 mode. DQ[15:8] float in x8 mode
CE[2:0]	Input	**CHIP ENABLE:** Activate the 256-Mbit devices' control logic, input buffers, decoders, and sense amplifiers. When the device is de-selected (see Table 6, "Chip Enable Truth Table for 256-Mb" on page 15), power reduces to standby levels. All timing specifications are the same for these three signals. Device selection occurs with the falling edge of CE0, CE1, or CE2 that enables the device. Device deselection occurs with the rising edge of CE0, CE1, or CE2 that disables the device (see Table 6, "Chip Enable Truth Table for 256-Mb" on page 15).
RP#	Input	**RESET:** RP#-low resets internal automation and puts the device in power-down mode. RP#-high enables normal operation. Exit from reset sets the device to read array mode. When driven low, RP# inhibits write operations which provides data protection during power transitions.
OE#	Input	**OUTPUT ENABLE:** Activates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	Input	**WRITE ENABLE:** Controls writes to the CUI, the Write Buffer, and array blocks. WE# is active low. Addresses and data are latched on the rising edge of WE#.
STS	Open Drain Output	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default), it acts as a RY/BY# signal. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. For alternate configurations of the Status signal, see the Configurations command and Section 11.2, "Status Signal" on page 31. STS is to be tied to VCCQ with a pull-up resistor.
BYTE#	Input	**BYTE ENABLE:** BYTE#-low places the device in x8 mode; data is input or output on DQ[7:0], while DQ[15:8] is placed in High-Z. Address A0 selects between the high and low byte. BYTE#-high places the device in x16 mode, and turns off the A0 input buffer. Address A1 becomes the lowest-order address bit.
VPEN	Input	**ERASE / PROGRAM / BLOCK LOCK ENABLE:** For erasing array blocks, programming data, or configuring lock-bits. With $V_{PEN} \le V_{PENLK}$, memory contents cannot be altered.
VCC	Power	**CORE Power Supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \le V_{LKO}$. Caution: Device operation at invalid Vcc voltages should not be attempted.
VCCQ	Power	**I/O Power Supply:** Power supply for Input/Output buffers.This ball can be tied directly to V_{CC}.
GND/VSS	Supply	**GROUND:** Ground reference for device logic voltages. Connect to system ground.
NC	—	**No Connect:** Lead is not internally connected; it may be driven or floated.
RFU	—	**Reserved for Future Use:** Balls designated as RFU are reserved by Numonyx for future device functionality and enhancement**.**

5.0 Bus Interface

This section provides an overview of Bus operations. There are three operations flash memory: Read, Program (Write), and Erase.

CE[2:0]-enable, OE#-low, WE#-high and RP#-high enable device read operations. Addresses are always assumed to be valid. OE#-low activates the outputs and gates selected data onto the I/O bus. WE#-low enables device write operations. Table 5 summarizes the necessary states of each control signal for different modes of operations.

Table 5: Bus Operations

Mode	RP#	CE_x(1)	OE#(2)	WE#(2)	$DQ_{15:0}$(3)	STS (Default Mode)	V_{PEN}	Notes
Reads: Async., Status, Query and Identifier	V_{IH}	Enabled	V_{IL}	V_{IH}	D_{OUT}	High-Z	X	4,6
Output Disable	V_{IH}	V_{IH}	Enabled	V_{IH}	High-Z	High-Z	X	
Command Writes	V_{IH}	Enabled	V_{IH}	V_{IL}	D_{IN}	High Z	X	6,7
Array Writes(8)	V_{IH}	Enabled	V_{IH}	V_{IL}	D_{IN}	V_{IL}	V_{PENH}	8,5
Standby	V_{IH}	Disabled	X	X	High Z	High Z	X	
Reset/Power-down	V_{IL}	X	X	X	High Z	High Z	X	

Notes:
1. See Table 6 for valid CE_x Configurations.
2. OE# and WE# should never be asserted simultaneously. If done so, OE# overrides WE#.
3. DQ refers to DQ[7:0] when BYTE# is low and DQ[15:0] if BYTE# is high.
4. Refer to DC characteristics. When $V_{PEN} \leq V_{PENLK}$, memory contents can be read but not altered.
5. X should be V_{IL} or V_{IH} for the control pins and V_{PENLK} or V_{PENH} for V_{PEN}. For outputs, X should be V_{OL} or V_{OH}.
6. In default mode, STS is V_{OL} when the WSM is executing internal block erase, program, or a lock-bit configuration algorithm. It is V_{OH} (pulled up by an external pull up resistance ≈10k) when the WSM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or reset power-down mode.
7. See Table 7 for valid DIN (user commands) during a Write operation
8. Array writes are either program or erase operations.

CE0, CE1 and CE2 control device activation. With the proper input (see Figure 6, "Chip Enable Truth Table for 256-Mb) the device gets selected, which in turn activates its internal circuits. WE# and OE# determine the direction of the data buffers (input or output).

Table 6: Chip Enable Truth Table for 256-Mb

CE2	CE1	CE0	DEVICE
V_{IL}	V_{IL}	V_{IL}	Enabled
V_{IL}	V_{IL}	V_{IH}	Disabled
V_{IL}	V_{IH}	V_{IL}	Disabled
V_{IL}	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Enabled
V_{IH}	V_{IL}	V_{IH}	Enabled
V_{IH}	V_{IH}	V_{IL}	Enabled
V_{IH}	V_{IH}	V_{IH}	Disabled

Note: For single-chip applications, CE2 and CE1 can be connected to GND.

5.1 Reads

Reading from flash memory outputs stored information to the processor or chipset, and does not change any contents. Reading can be performed an unlimited number of times. Besides array data, other types of data such as device information or device status are available from the flash.

To perform a bus read operation, CEx (refer to Table 6 on page 15) and OE# must be asserted. CEx is the device-select control; when active, it enables the flash memory device. OE# is the data-output control; when active, the addressed flash memory data is driven onto the I/O bus. For all read states, WE# and RP# must be de-asserted. See Section 7.0, "Read operation" on page 21.

5.2 Writes

Writing or Programming to the device is where the host writes information or data into the flash device for non-volatile storage. When the flash device is programmed, 'ones' are changed to 'zeros'. 'Zeros' cannot be programmed back to 'ones'. To do so, an erase operation must be performed. Writing commands to the Command User Interface (CUI) enables various modes of operation, including the following:

- Reading of array data
- Common Flash Interface (CFI) data
- Identifier codes, inspection, and clearing of the Status Register
- Block Erasure, Program, and Lock-bit Configuration (when $V_{PEN} = V_{PENH}$)

Erasing is performed on a block basis – all flash cells within a block are erased together. Any information or data previously stored in the block will be lost. Erasing is typically done prior to programming. The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Program command requires the command and address of the location to be written. Set Block Lock-Bit commands require the command and block within the device to be locked. The Clear Block Lock-Bits command requires the command and address within the device to be cleared.

The CUI does not occupy an addressable memory location. It is written when the device is enabled and WE# is active. The address and data needed to execute a command are latched on the rising edge of WE# or the first edge of CE0, CE1, or CE2 that disables the device (see Table 6 on page 15). Standard microprocessor write timings are used.

5.3 Output Disable

With CEx asserted, and OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output signals D[15:0] are placed in a high-impedance state.

5.4 Standby

CE0, CE1, and CE2 can disable the device (see Table 6 on page 15) and place it in standby mode. This manipulation of CEx substantially reduces device power consumption. D[15:0] outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, program, or lock-bit configuration, the WSM continues functioning, and consuming active power until the operation completes.

5.5 Reset

RP# at V_{IL} initiates the reset/power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state, and turns off numerous internal circuits. RP# must be held low for a minimum of t_{PLPH}. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and Status Register is set to 0080h.

During Block Erase, Program, or Lock-Bit Configuration modes, RP#-low will abort the operation. In default mode, STS transitions low and remains low for a maximum time of t_{PLPH} + t_{PHRH} until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after a program or partially altered after an erase or lock-bit configuration. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during Block Erase, Program, or Lock-Bit Configuration modes. If a CPU reset occurs with no flash memory reset, proper initialization may not occur because the flash memory may be providing status information instead of array data. Numonyx Flash memories allow proper initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

6.0 Command Set

6.1 Device Command Codes

The system Central Processing Unit provides control of all in-system read, write, and erase operations of the device via the system bus. The on-chip WSM manages all block-erase and program algorithms.

Device commands are written to the CUI to control all flash memory device operations. The CUI does not occupy an addressable memory location; it is the mechanism through which the flash device is controlled. Table 7 shows valid device command codes and descriptions.

Table 7: Command Codes and Definitions (Sheet 1 of 2)

Mode	Code	Device Mode	Description
Read	0xFF	Read Array	Places the device in Read Array mode. Array data is output on DQ[15:0].
	0x70	Read Status Register	Places the device in Read Status Register mode. The device enters this mode after a program or erase command is issued. SR data is output on DQ[7:0].
	0x90	Read Device ID or Configuration Register	Places device in Read Device Identifier mode. Subsequent reads output manufacturer/device codes, Configuration Register data, Block Lock status, or OTP register data on DQ[15:0].
	0x98	Read Query	Places the device in Read Query mode. Subsequent reads output Common Flash Interface information on DQ[7:0].
	0x50	Clear Status Register	The WSM can only set SR error bits. The Clear Status Register command is used to clear the SR error bits.
Program	0x40	Word/Byte Program Setup	First cycle of a 2-cycle programming command, prepares the CUI for a write operation. On the next write cycle, the address and data are latched and the WSM executes the programming algorithm at the addressed location. During program operations, the device responds only to Read Status Register and Program Suspend commands. CE_X or OE# must be toggled to update the Status Register in asynchronous read. CE_X must be toggled to update the SR Data for synchronous Non-array reads. The Read Array command must be issued to read array data after programming has finished.
	0xE8	Buffered Program	This command loads a variable number of words up to the buffer size of 512 words onto the program buffer in x16 mode. (1)
	0xD0	Program Confirm	The confirm command is Issued after the data streaming for writing into the buffer is done. This instructs the WSM to perform the Buffered Program algorithm, writing the data from the buffer to the flash memory array.
Erase	0x20	Block Erase Setup	First cycle of a 2-cycle command; prepares the CUI for a block-erase operation. The WSM performs the erase algorithm on the block addressed by the Erase Confirm command. If the next command *is not* the Erase Confirm (0xD0) command, the CUI sets Status Register bits SR [5,4], and places the device in Read Status Register mode.
	0xD0	Block Erase Confirm	If the first command was Block Erase Setup (0x20), the CUI latches the address and data, and the WSM erases the addressed block. During block-erase operations, the device responds only to Read Status Register and Erase Suspend commands. CE_X or OE# must be toggled to update the Status Register in asynchronous read. CE_X must be toggled to update the SR Data for synchronous Non-array reads.
Suspend	0xB0	Program or Erase Suspend	This command issued to any device address initiates a suspend of the currently-executing program or block erase operation. The Status Register indicates successful suspend operation by setting either SR.2 (program suspended) or SR 6 (erase suspended), along with SR.7 (ready). The WSM remains in the suspend mode regardless of control signal states (except for RPRP# asserted).
	0xD0	Suspend Resume	This command issued to any device address resumes the suspended program or block-erase operation.

Table 7: Command Codes and Definitions (Sheet 2 of 2)

Mode	Code	Device Mode	Description
Protection	0x60	Block lock Setup	First cycle of a 2-cycle command; prepares the CUI for block lock configuration changes. If the next command is not Block Lock (0x01), Block Unlock (0xD0), the CUI sets SR.5 and SR.4, indicating a command sequence error.
	0x01	Block lock	If the previous command was Block Lock Setup (0x60), the addressed block is locked.
	0xD0	Unlock Block	If the previous command was Block Lock Setup (0x60), on issuing this command, all of the Block lock bits that are set are cleared in parallel.
	0xC0	Protection program setup	First cycle of a 2-cycle command; prepares the device for a OTP register or Lock Register program operation. The second cycle latches the register address and data, and starts the programming algorithm to program data the OTP array.
	0xEB	Extended Function Interface (EFI)	This command is used in security features. first cycle of a multiple-cycle command second cycle is a Sub-Op-Code, the data written on third cycle is one less than the word count; the allowable value on this cycle are 0 through 511. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved. For additional information and collateral request, please contact your filed.
STS Configuration	B8h	Configuration Set-Up	Configures the STS pin to different states. The default operation of the STS pin is the level mode, just like RY/BY# which indicates if the Write State Machine is Busy or Available. Using this command the STS pin can be configured to generate an Erase/Program interrupt pulse once the operation is done.
	00h	Configuration Code	Configures the STS pin in level mode. Makes the STS pin function like a RY/BY# pin.
	01h		Configures the STS pin to generate a pulse once an erase operation is completed.
	02h		The STS pin is configured to generate a pulse once a program operation completes.
	03h		The STS pin is configured to generate a pulse when either a program or erase operation completes.

6.2 Device Command Bus Cycle

Device operations are initiated by writing specific device commands to the CUI. See Table 8, "Command Bus Cycles" on page 19. Several commands are used to modify array data including Word Program and Block Erase commands. Writing either command to the CUI initiates a sequence of internally-timed functions that culminate in the completion of the requested task. However, the operation can be aborted by either asserting RP# or by issuing an appropriate suspend command.

Table 8: Command Bus Cycles (Sheet 1 of 2)

Mode	Command	Bus Cycles	First Bus Cycle		Second Bus Cycle		Last Bus Cycle	
			Addr(1)	Data(2)	Addr(1)	Data(2)	Addr(1)	Data(2)
Read	Read Array	1	DnA	0xFF	---	---	---	---
	Read Status Register	2	DnA	0x70	DnA	SRD	---	---
	Read Device Identifier	≥ 2	DnA	0x90	DBA + IA	ID	---	---
	Read CFI	≥ 2	DnA	0x98	DBA + CFI-A	CFI-D	---	---
	Clear Status Register	1	DnA	0x50	---	---	---	---
Program	Word Program	2	WA	0x40	WA	WD	---	---
	Buffered Program(3)	> 2	WA	0xE8	WA	N - 1	WA	0xD0

Table 8: Command Bus Cycles (Sheet 2 of 2)

Mode	Command	Bus Cycles	First Bus Cycle		Second Bus Cycle		Last Bus Cycle	
			Addr(1)	Data(2)	Addr(1)	Data(2)	Addr(1)	Data(2)
Erase	Block Erase	2	BA	0x20	BA	0xD0	---	---
Suspend	Program/Erase Suspend	1	DnA	0xB0	---	---	---	---
	Program/Erase Resume	1	DnA	0xD0	---	---	---	---
Protection	Lock Block	2	BA	0x60	BA	0x01	---	---
	Unlock Block	2	BA	0x60	BA	0xD0	---	---
	Program OTP register	2	OTP-RA	0xC0	OTP-RA	OTP-D	---	---
	Program Lock Register	2	LRA	0xC0	LRA	LRD	---	---
	STS Configuration	2	BA	0xB8	BA	Register Data	---	---
	Extended Flash Interface (4)	> 2	WA	0xEB	WA	Sub-Op code	WA	0xD0

Notes:

1. First command cycle address should be the same as the operation's target address.
   DBA = Device Base Address
   DnA = Address within the device.
   IA = Identification code address offset.
   CFI-A = Read CFI address offset.
   WA = Word address of memory location to be written.
   BA = Address within the block.
   OTP-RA = OTP register address.
   LRA = Lock Register address.
   RCD = Read Configuration Register data on A[15:0].
2. ID = Identifier data.
   CFI-D = CFI data on DQ[15:0].
   SRD = Status Register data.
   WD = Word data.
   N = Word count of data to be loaded into the write buffer.
   OTP-D = OTP register data.
   LRD = Lock Register data.
3. The second cycle of the Buffered Program Command is the word count of the data to be loaded into the write buffer. This is followed by up to 512 words of data.Then the confirm command (0xD0) is issued, triggering the array programming operation.
4. The second cycle is a Sub-Op-Code, the data written on third cycle is N-1; 1=<N<=512. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved, after the data words are loaded, the final cycle is the confirm cycle 0xD0)

7.0 Read operation

The device can be in any of four read states: Read Array, Read Identifier, Read Status Register or Read Query. Upon power-up, or after a reset, the device defaults to Read Array mode. To change the read state, the appropriate read command must be written to the device (see Section 6.1, "Device Command Codes" on page 18). The following sections describe read-mode operations in detail.

7.1 Read Array

Upon power-up or return from reset, the device defaults to Read Array mode. Issuing the Read Array command places the device in Read Array mode. Subsequent reads output array data on DQ[15:0]. The device remains in Read Array mode until a different read command is issued, or a program or erase operation is performed, in which case, the read mode is automatically changed to Read Status.

To change the device to Read Array mode while it is programming or erasing, first issue the Suspend command. After the operation has been suspended, issue the Read Array command. When the program or erase operation is subsequently resumed, the device will automatically revert back to Read Status mode.

Note: Issuing the Read Array command to the device while it is actively programming or erasing causes subsequent reads from the device to output invalid data. Valid array data is output only after the program or erase operation has finished.

The Read Array command functions independent of the voltage level on VPEN.

7.2 Asynchronous Page Mode Read

J3-65nm supports asynchronous page mode read access only. J3-65nm also supports Byte or Word accesses depending on the level of BYTE#.

- If BYTE# is at V_{IL} then the data will be outputted on the DQ_{7-0}. This read access is called "x8 mode". The DQ_{15-8} signals will be in high-z.
- If BYTE# is at V_{IH} then the data will be outputted on DQ_{15-0}.This read access is called "x16 mode."

The default read mode of the device after power up or hardware reset is read array mode.The Read Array/ Software Reset command returns the device to read array mode. Any following read accesses to devices returns main array data.

The page size is sixteen words (32 bytes). Each read operation internally retrieves sixteen words of data, which are determined by addressed bits A[MAX:5].In x16 mode, the first word of data, defined by A[4:1], is output to the data bus within t_{AVQV}. After this initial access time, subsequent words can be output to the data bus by changing address bits A[4:1]. In x8 mode, the first byte of data, defined by A[4:0], is output to the data bus within t_{AVQV}. After this initial access time, subsequent bytes can be output to the data bus by changing address bits A[4:0]. Any subsequent data word(s) within the page can be output to the data bus within t_{APA}, which is much shorter than t_{AVQV}. The internal read operation can also be initiated by asserting CE_X while addresses are valid or changing the A[MAX:5] while CE_X is asserted.

7.3 Read Status Register

Issuing the Read Status Register command places the device in Read Status Register mode. Subsequent reads output Status Register information on DQ[7:0], and 00h on DQ[15:8]. The device remains in Read Status Register mode until a different read-mode command is issued. Performing a program, erase, or block-lock operation also changes the device's read mode to Read Status Register mode.

The Status Register is updated on the falling edge of CE, or OE# when CE is active. Status Register contents are valid only when SR.7 = 1. When WSM is busy, SR.7 indicates the WSM's state and SR[6:0] are in high-Z state.

The Read Status Register command functions independent of the voltage level on VPEN.

7.4 Read Device Information

Issuing the Read Device Information command places the device in Read Device Information mode. Subsequent reads output device information on DQ[15:0].

The device remains in Read Device Information mode until a different read command is issued. Also, performing a program, erase, or block-lock operation changes the device to Read Status Register mode.

The Read Device Information command functions independent of the voltage level on VPEN.

Table 9: Device Identifier Information

Item	Address(1,2,3)	Data
Manufacturer Code	0x00	0x89h
Device ID Code	0x01	ID (see Table 1)
Block Lock Configuration: • Block Is Unlocked • Block Is Locked	BBA + 0x02	Lock Bit: DQ0 = 0b0 DQ0 = 0b1
J3A Block Lock Compatibility	0x03	0x000 (4)
General Purpose Register(5)	DBA + 0x07	general data
Lock Register 0	0x80	PR-LK0
64-bit Factory-Programmed OTP register	0x81–0x84	Factory OTP register data
64-bit User-Programmable OTP Register	0x85–0x88	User OTP register data

Notes:
1. BBA = Block Base Address.
2. DBA = Device base Address, Numonyx reserves other configuration address locations
3. A_0 is not used in either x8 or x16 modes during manufacturer and device ID reads. The lowest order address line is A_1.
4. When reading Block Base Address + 00003h, the user needs to read 0000h to be backward compatibly to J3A.
5. The GPR is used as read out register for Extended Functional Interface (EFI) command.

7.5 CFI Query

The CFI query table contains an assortment of flash product information such as block size, density, allowable command sets, electrical specifications, and other product information. The data contained in this table conforms to the CFI protocol.

Issuing the CFI Query command places the device in CFI Query mode. Subsequent reads output CFI information on DQ[15:0]. The device remains in CFI Query mode until a different read command is issued, or a program or erase operation is performed, which changes the read mode to Read Status Register mode.

The CFI Query command functions independent of the voltage level on VPEN.

8.0 Program operation

All programming operations require the addressed block to be unlocked, and a valid VPEN voltage applied throughout the programming operation. Otherwise, the programming operation will abort, setting the appropriate Status Register error bit(s).

The following sections describe each programming method.

8.1 Single-Word/Byte Programming

Array programming is performed by first issuing the Single-Word/Byte Program command. This is followed by writing the desired data at the desired array address. The read mode of the device is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued.

During programming, STS and the Status Register indicate a busy status (SR.7 = 0). Upon completion, STS and the Status Register indicate a ready status (SR.7 = 1). The Status Register should be checked for any errors (SR.4), then cleared.

Note: Issuing the Read Array command to the device while it is actively programming causes subsequent reads from the device to output invalid data. Valid array data is output only after the program operation has finished.

Standby power levels are not realized until the programming operation has finished. Also, asserting RP# aborts the programming operation, and array contents at the addressed location are indeterminate. The addressed block should be erased, and the data re-programmed. If a Single-Word/Byte program is attempted when the corresponding block lock-bit is set, SR.1 and SR.4 will be set.

8.2 Buffered Programming

The device features a 512-word buffer to enable optimum programming performance. For Buffered Programming, data is first written to an on-chip write buffer. Then the buffer data is programmed into the flash memory array in buffer-size increments. This can improve system programming performance significantly over non-buffered programming. (see Figure 19, “Buffer Program Flowchart” on page 59).

When the Buffered Programming Setup command is issued, Status Register information is updated and reflects the availability of the buffer. SR.7 indicates buffer availability: if set, the buffer is available; if cleared, the buffer is not available. To retry, issue the Buffered Programming Setup command again, and re-check SR.7. When SR.7 is set, the buffer is ready for loading.

On the next write, a word count is written to the device at the buffer address. This tells the device how many data words will be written to the buffer, up to the maximum size of the buffer.

On the next write, a device start address is given along with the first data to be written to the flash memory array. Subsequent writes provide additional device addresses and data. All data addresses must lie within the start address plus the word count.

Optimum programming performance and lower power usage are obtained by aligning the starting address at the beginning of a 512-word boundary (A[9:1] = 0x00). The maximum buffer size would be 256-word if the misaligned address range is crossing a 512-word boundary during programming.

After the last data is written to the buffer, the Buffered Programming Confirm command must be issued to the original block address. The WSM begins to program buffer contents to the flash memory array. If a command other than the Buffered

Programming Confirm command is written to the device, a command sequence error occurs and SR[7,5,4] are set. If an error occurs while writing to the array, the device stops programming, and SR[7,4] are set, indicating a programming failure.

When Buffered Programming has completed, additional buffer writes can be initiated by issuing another Buffered Programming Setup command and repeating the buffered program sequence.

If an attempt is made to program past an erase-block boundary using the Buffered Program command, the device aborts the operation. This generates a command sequence error, and SR[5,4] are set.

If Buffered programming is attempted while VPEN is below V_{PENLK}, SR[4,3] are set. If any errors are detected that have set Status Register bits, the Status Register should be cleared using the Clear Status Register command.

Note: In x8 mode, a maximum of 256 bytes of data can be loaded into the write buffer as N can have a max value of FFh.

8.3 Suspend/Resume

An erase or programming operation can be suspended to perform other operations, and then subsequently resumed. Please refer to Chapter 9.0, "Suspend/Resume" for details.