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Numonyx® Embedded Flash Memory (J3 65 nm) Single Bit per Cell (SBC)

32, 64, and 128 Mbit

Datasheet

Product Features

- Architecture
  - Symmetrical 128-KB blocks
  - 128 Mbit (128 blocks)
  - 64 Mbit (64 blocks)
  - 32 Mbit (32 blocks)
  - Blank Check to verify an erased block
- Performance
  - Initial Access Speed: 75ns
  - 25 ns 8-word Asynchronous page-mode reads
  - 256-Word write buffer for x16 mode, 256-Byte write buffer for x8 mode; 1.41 µs per Byte Effective programming time
- System Voltage
  - V_{CC} = 2.7 V to 3.6 V
  - V_{CCQ} = 2.7 V to 3.6 V
- Packaging
  - 56-Lead TSOP
  - 64-Ball Easy BGA package
- Security
  - Enhanced security options for code protection
  - Absolute protection with V_{PEN} = Vss
  - Individual block locking
  - Block erase/program lockout during power transitions
  - Password Access feature
  - One-Time Programmable Register: 64 OTP bits, programmed with unique information by Numonyx 64 OTP bits, available for customer programming
- Software
  - Program and erase suspend support
  - Numonyx® Flash Data Integrator (FDI)
  - Common Flash Interface (CFI) Compatible
  - Scalable Command Set
- Quality and Reliability
  - Operating temperature: -40 °C to +85 °C
  - 100K Minimum erase cycles per block
  - 65 nm Flash Technology
  - JESD47E Compliant

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Jan 2011

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

Contents

Revision History

Date	Revision	Description
May 2009	01	Initial release
March 2010	02	Add Blank Check function and command. Add Blank Check specification tBC/MB, update Clear Block Lock-Bits Max Time and Program time in Table 13, "Configuration Performance" on page 28. Update I_{CCR} in Table 7, "DC Current Characteristics" on page 21. Order information with device features digit. Update part number information in Valid Combination table. Add a note to clarify the SR output after E8 command in Figure 16, "Write to Buffer Flowchart" on page 48. State JESD47E Compliant at front page. Update ECR.13 description in Table 18, "Enhanced Configuration Register" on page 32.
Jan 2011	03	Correct the typo of comment for offset 24h at CFI from 2048µs to 1024µs. Correct the typo of t_{AVQV} and t_{ELQV} to Max Specifications. Emphasize the valid and legal command usage at Section 11.0, "Device Command Codes" on page 47. Put a link for part numbers after Table 46, "Valid Combinations" on page 65. Add Buffer Program Time for 128 Words (256 Bytes) at Table 13, "Configuration Performance" on page 28. Add JEDEC standard lead width for TSOP56 package at Table 1, "56-Lead TSOP Dimension Table" on page 13.

1.0 Introduction

This document contains information pertaining to the Numonyx® Embedded Flash Memory (J3 65 nm) Single Bit per Cell (SBC) device features, operation, and specifications.

Unless otherwise indicated throughout the rest of this document, the Numonyx® Embedded Flash Memory (J3 65 nm) Single Bit per Cell (SBC) device is referred to as J3 65 nm SBC.

The J3 65 nm SBC device provides improved mainstream performance with enhanced security features, taking advantage of the high quality and reliability of the NOR-based 65 nm technology. Offered in 128-Mbit, 64-Mbit, and 32-Mbit densities, the J3 65 nm SBC device brings reliable, low-voltage capability (3 V read, program, and erase) with high speed, low-power operation. The J3 65 nm SBC device takes advantage of proven manufacturing experience and is ideal for code and data applications where high density and low cost are required, such as in networking, telecommunications, digital set top boxes, audio recording, and digital imaging. Numonyx Flash Memory components also deliver a new generation of forward-compatible software support. By using the Common Flash Interface (CFI) and Scalable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Numonyx Flash Memory devices.

1.1 Nomenclature

J3 65 nm SBC	Numonyx® Embedded Flash Memory (J3 65 nm) Single Bit per Cell (SBC)	
AMIN	All Densities	AMIN = A0 for x8
	All Densities	AMIN = A1 for x16
AMAX	32 Mbit	AMAX = A21
	64 Mbit	AMAX = A22
	128 Mbit	AMAX = A23
Block	A group of flash cells that share common erase circuitry and erase simultaneously.	
Clear	Indicates a logic zero (0)	
Program	Writes data to the flash array	
Set	Indicates a logic one (1)	
VPEN	Refers to a signal or package connection name	
V_{PEN}	Refers to timing or voltage levels	

1.2 Acronyms

SBC	Single Bit per Cell
FDI	Flash Data Integrator
CFI	Common Flash Interface
SCS	Scalable Command Set
CUI	Command User Interface
OTP	One Time Programmable
PLR	Protection Lock Register
PR	Protection Register
PRD	Protection Register Data
RFU	Reserved for Future Use
SR	Status Register
SRD	Status Register Data
WSM	Write State Machine
ECR	Enhanced Configuration Register
ECD	Enhanced Configuration Register Data

1.3 Conventions

h	Hexadecimal Suffix
K(noun)	1,000
M (noun)	1,000,000
Nibble	4 bits
Byte	8 bits
Word	16 bits
Kb	1,024 bits
KB	1,024 bytes
KW	1,024 words
Mb	1,048,576 bits
MB	1,048,576 bytes
MW	1,048,576 words
Kbit	1,024 bits
Mbit	1,048,576 bits

Brackets	Square brackets ([]) will be used to designate group membership or to define a group of signals with similar function (i.e. A[21:1], SR[4,1] and D[15:0]).
00FFh	Denotes 16-bit hexadecimal numbers
00FF 00FFh	Denotes 32-bit hexadecimal numbers
DQ[15:0]	Data I/O signals

2.0 Functional Overview

The J3 65 nm SBC family contains high-density memory organized in any of the following configurations:

- 16-MB or 8-MW (128-Mbit), organized as one-hundred-twenty-eight 128-KB erase blocks.
- 8-MB or 4-MW (64-Mbit), organized as sixty-four 128-KB erase blocks.
- 4-MB or 2-MW (32-Mbit), organized as thirty-two 128-KB erase blocks.

These devices can be accessed as 8- or 16-bit words. See Figure 1, “Memory Block Diagram for 32-, 64-, 128-Mbit” on page 11 for further details.

A 128-bit Protection Register has multiple uses, including unique flash device identification.

The J3 65 nm SBC device includes new security features that were not available on the (previous) 0.13µm versions of the J3 family. These new security features prevent altering of code through different protection schemes that can be implemented, based on user requirements.

The J3 65 nm SBC optimized architecture and interface dramatically increases read performance by supporting page-mode reads. This read mode is ideal for non-clock memory systems.

Its Common Flash Interface (CFI) permits software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

The Scalable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device’s 128-KB blocks typically within one second, independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or program data from any other block. Similarly, program suspend allows system software to suspend programming (byte/word program and write-to-buffer operations) to read data or execute code from any other block that is not being suspended.

Each device incorporates a Write Buffer of 256-Byte (x8 mode) or 256-Word (x16 mode) to allow optimum programming performance. By using the Write Buffer data is programmed more efficiently in buffer increments.

Memory Blocks are selectively and individually lockable in-system. Individual block locking uses block lock-bits to lock and unlock blocks. Block lock-bits gate block erase and program operations. Lock-bit configuration operations set and clear lock-bits (using the Set Block Lock-Bit and Clear Block Lock-Bits commands).

The Status Register indicates when the WSM's block erase, program, or lock-bit configuration operation completes.

The STS (status) output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status indication using STS minimizes both CPU overhead and system power consumption. When configured in level mode (default mode), it acts as a RY/BY# signal. When low, STS indicates that the WSM is performing a block erase, program, or lock-bit configuration. STS-high indicates that the WSM is ready for a new command, block erase is suspended (and programming is inactive), program is suspended, or the device is in reset/power-down mode. Additionally, the configuration command allows the STS signal to be configured to pulse on completion of programming and/or block erases.

Three CE signals are used to enable and disable the device. A unique CE logic design (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30) reduces decoder logic typically required for multi-chip designs. External logic is not required when designing a single chip, a dual chip, or a 4-chip miniature card or SIMM module.

The BYTE# signal allows either x8 or x16 read/writes to the device:

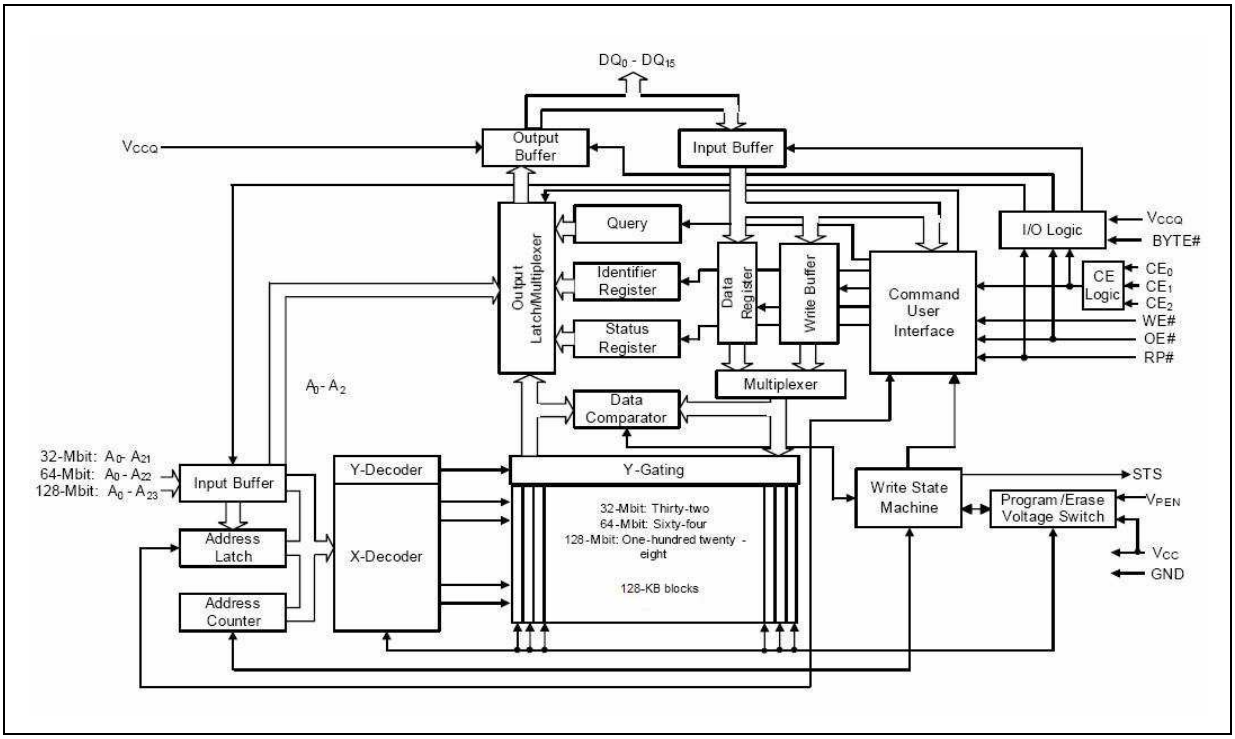
- BYTE#-low enables 8-bit mode; address A0 selects between the low byte and high byte.
- BYTE#-high enables16-bit operation; address A1 becomes the lowest order address and address A0 is not used (don't care).

Figure 1, "Memory Block Diagram for 32-, 64-, 128-Mbit" on page 11 shows a device block diagram.

When the device is disabled (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30), with CEx at V_{IH} and RP# at V_{IH}, the standby mode is enabled. When RP# is at V_{IL}, a further power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# going high until data outputs are valid. Likewise, the device has a wake time (t_{PHWL}) from RP#-high until writes to the CUI are recognized. With RP# at V_{IL}, the WSM is reset and the Status Register is cleared.

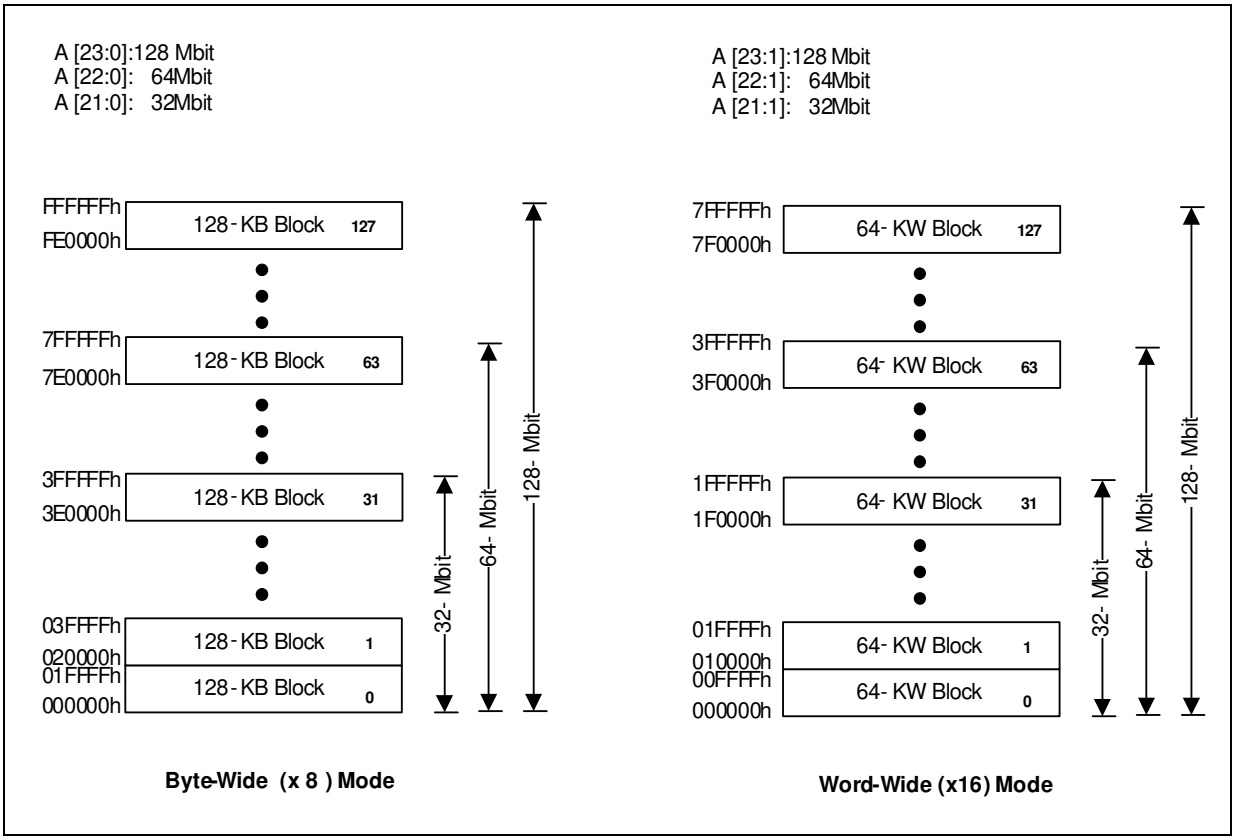
2.1 Block Diagram

Figure 1: Memory Block Diagram for 32-, 64-, 128-Mbit



2.2 Memory Map

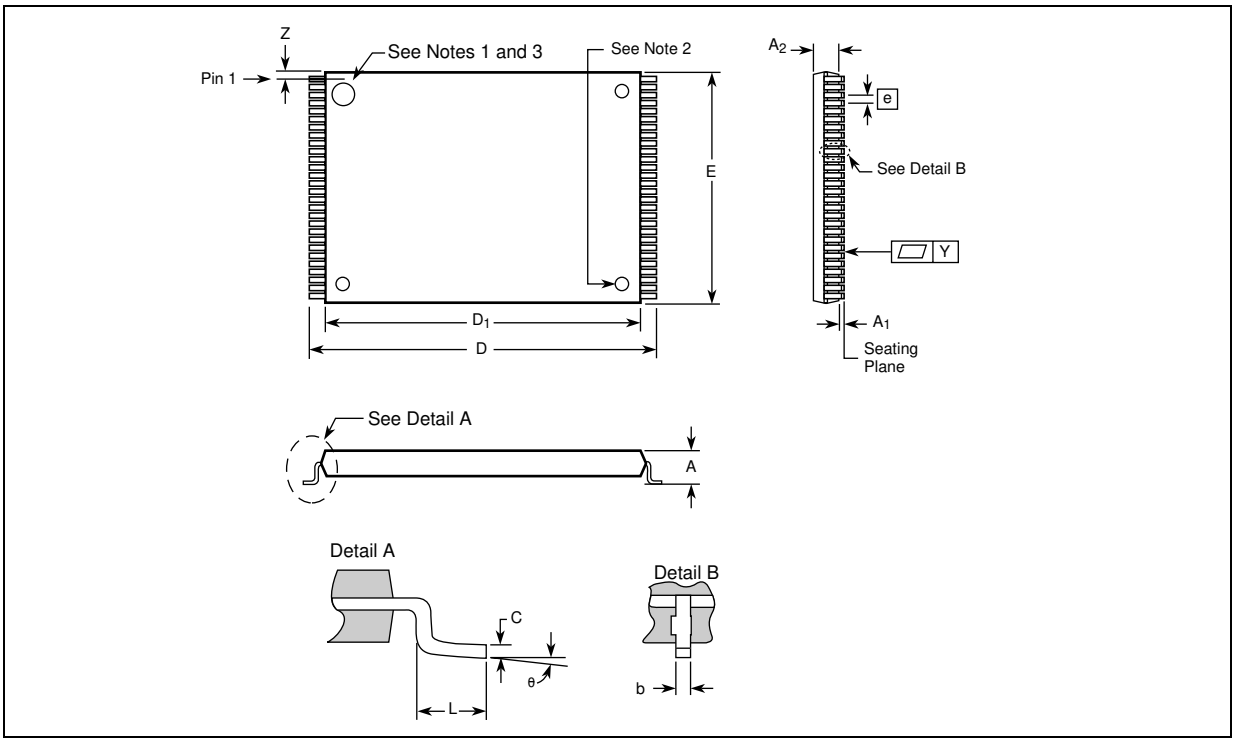
Figure 2: J3 65 nm SBC Memory Map



3.0 Package Information

3.1 56-Lead TSOP Package for 32-, 64-, 128-Mbit

Figure 3: 56-Lead TSOP Package Mechanical



Notes:
1. One dimple on package denotes Pin 1.
2. If two dimples, then the larger dimple denotes Pin 1.
3. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.

Table 1: 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	—	—	1.200	—	—	0.047
Standoff	A_1	0.050	—	—	0.002	—	—
Package Body Thickness	A_2	0.965	0.995	1.025	0.038	0.039	0.040
Lead Width[1]	b	0.170	0.220	0.270	0.0067	0.0087	0.0106
Lead Thickness	c	0.100	0.150	0.200	0.004	0.006	0.008
Package Body Length	D_1	18.200	18.400	18.600	0.717	0.724	0.732
Package Body Width	E	13.800	14.000	14.200	0.543	0.551	0.559
Lead Pitch	e	—	0.500	—	—	0.0197	—
Terminal Dimension	D	19.800	20.00	20.200	0.780	0.787	0.795
Lead Tip Length	L	0.500	0.600	0.700	0.020	0.024	0.028

Table 1: 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Lead Count	N	—	56	—	—	56	—
Lead Tip Angle	θ	0°	3°	5°	0°	3°	5°
Seating Plane Coplanarity	Y	—	—	0.100	—	—	0.004
Lead to Package Offset	Z	0.150	0.250	0.350	0.006	0.010	0.014

1. For legacy lead width, 0.15mm (Typ), 0.10mm (Min), 0.20mm (Max).

3.2 64-Ball Easy BGA Package for 32-, 64-, 128-Mbit

Figure 4: 64-Ball Easy BGA Mechanical Specifications

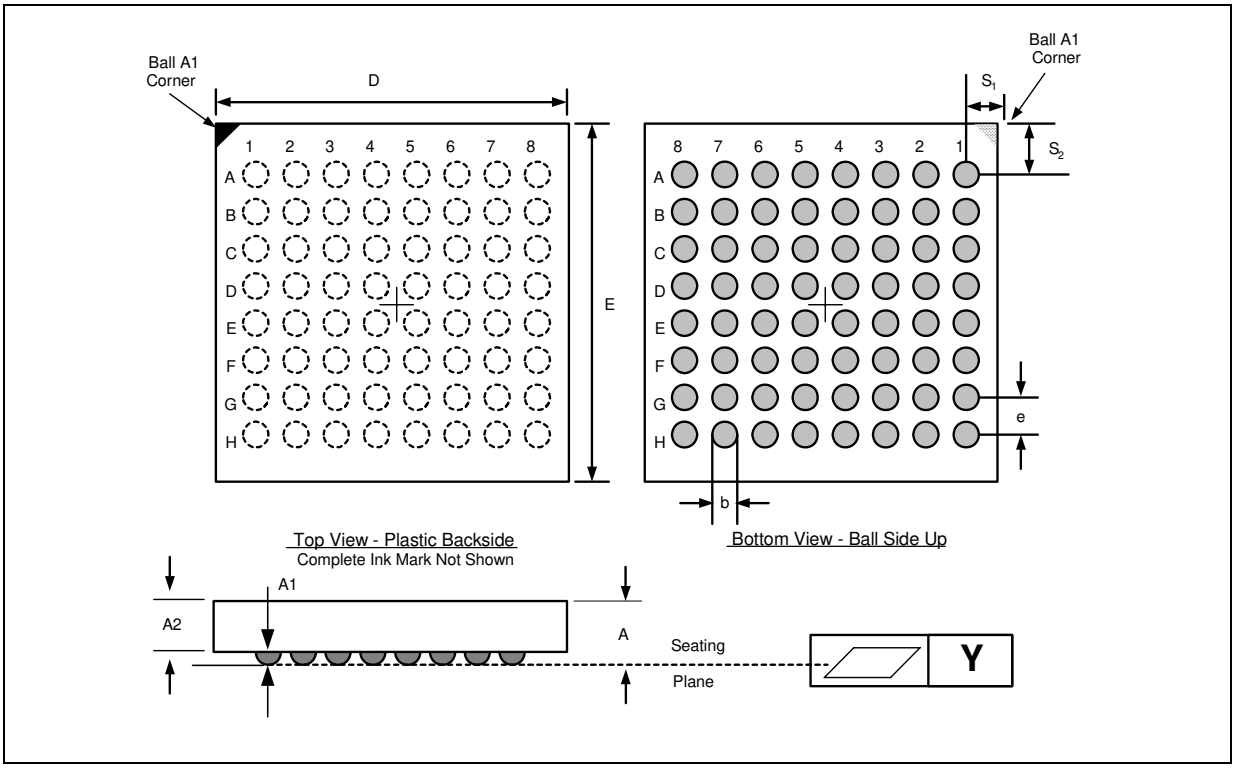


Table 2: Easy BGA Package Dimensions Table (Sheet 1 of 2)

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	—	—	1.200	—	—	0.0472
Ball Height	A1	0.250	—	—	0.0098	—	—
Package Body Thickness	A2	—	0.780	—	—	0.0307	—
Ball (Lead) Width	b	0.310	0.410	0.510	0.012	0.016	0.020

Table 2: Easy BGA Package Dimensions Table (Sheet 2 of 2)

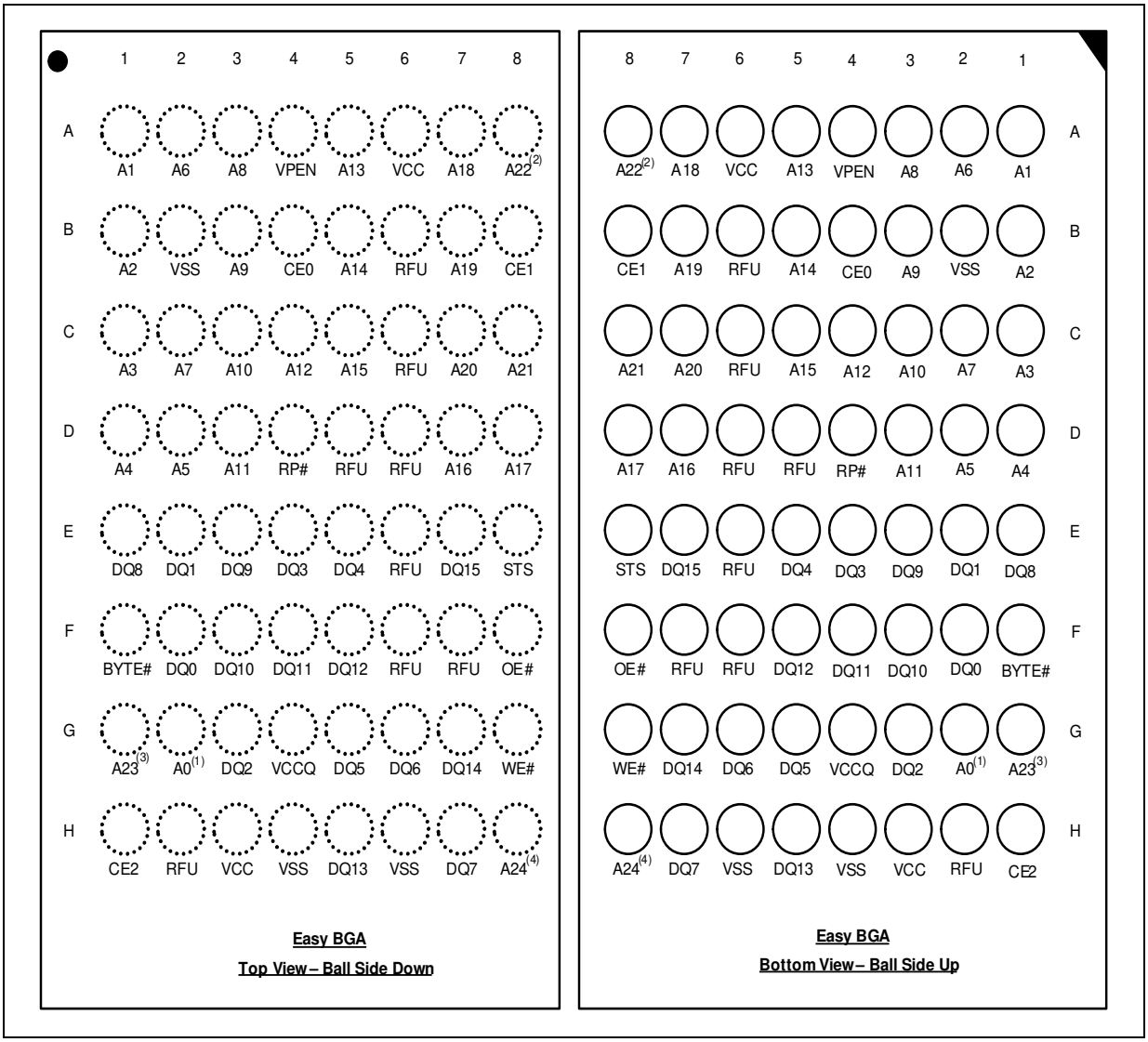
Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Body Width	D	9.900	10.000	10.100	0.3898	0.3937	0.3976
Package Body Length	E	12.900	13.000	13.100	0.5079	0.5118	0.5157
Pitch	e	—	1.000	—	—	0.0394	—
Ball (Lead) Count	N	—	64	—	—	64	—
Seating Plane Coplanarity	Y	—	—	0.100	—	—	0.0039
Corner to Ball A1 Distance Along D	S1	1.400	1.500	1.600	0.0551	0.0591	0.0630
Corner to Ball A1 Distance Along E	S2	2.900	3.000	3.100	0.1142	0.1181	0.1220

4.0 Ballouts/ Pinouts and Signal Descriptions

J3 65 nm SBC is available in two package types. All densities of the J3 65 nm SBC devices are supported on both 64-ball Easy BGA and 56-lead Thin Small Outline Package (TSOP) packages. The figures below show the ballouts/Pinouts.

4.1 Easy BGA Ballout for 32-, 64-, 128-Mbit

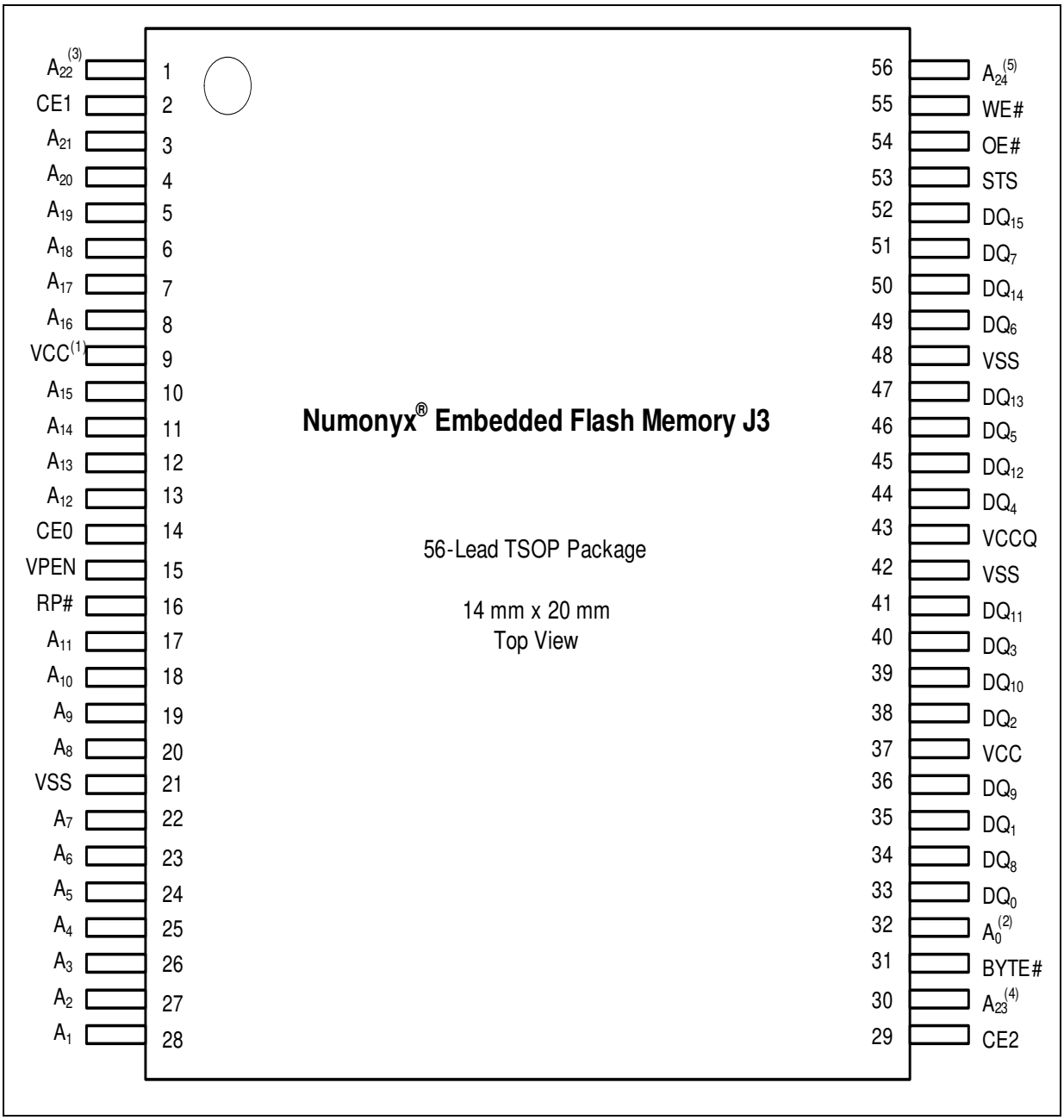
Figure 5: Easy BGA Ballout (32/ 64/ 128 Mbit)



Notes:
1. A0 is the least significant address bit.
2. A22 is valid for 64-Mbit density and above. On 32-Mbit, it is a no-connect (NC).
3. A23 is valid for 128-Mbit density. On 32- and 64-Mbit, it is a no-connect (NC).
4. A24 is a no connect (NC) on 128-, 64-, 32- Mbit, reserved for 256-Mbit.

4.2 56-Lead TSOP Package Pinout for 32-, 64-,128-Mbit

Figure 6: 56-Lead TSOP Package Pinout (32/ 64/ 128 Mbit)



Notes:
1. No internal connection for pin 9; it may be driven or floated. For legacy designs, the pin can be tied to V_{CC}.
2. A0 is the least significant address bit.
3. A22 is valid for 64-Mbit density and above. On 32-Mbit, it is a no-connect (NC).
4. A23 is valid for 128-Mbit density. On 32- and 64-Mbit, it is a no-connect (NC).
5. A24 is a no connect (NC) on 128-, 64-, 32- Mbit, reserved for 256-Mbit.

4.3 Signal Descriptions

Table 3 lists the active signals used on J3 65 nm SBC and provides a description of each.

Table 3: Signal Descriptions for J3 65 nm SBC

Symbol	Type	Name and Function
A0	Input	**BYTE-SELECT ADDRESS:** Selects between high and low byte when the device is in x8 mode. This address is latched during a x8 program cycle. Not used in x16 mode (i.e., the A0 input buffer is turned off when BYTE# is high).
A[MAX:1]	Input	**ADDRESS INPUTS:** Inputs for addresses during read and program operations. Addresses are internally latched during a program cycle: 32-Mbit — A[21:1] 64-Mbit— A[22:1] 128-Mbit — A[23:1]
DQ[7:0]	Input/ Output	**LOW-BYTE DATA BUS:** Inputs data during buffer writes and programming, and inputs commands during CUI writes. Outputs array, CFI, identifier, or status data in the appropriate read mode. Data is internally latched during write operations.
DQ[15:8]	Input/ Output	**HIGH-BYTE DATA BUS:** Inputs data during x16 buffer writes and programming operations. Outputs array, CFI, or identifier data in the appropriate read mode; not used for Status Register reads. Data is internally latched during write operations in x16 mode. D[15:8] float in x8 mode.
CE[2:0]	Input	**CHIP ENABLE:** Activates the 32-, 64-, 128-Mbit devices' control logic, input buffers, decoders, and sense amplifiers. When the device is de-selected (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30), power reduces to standby levels. All timing specifications are the same for these three signals. Device selection occurs with the first edge of CE0, CE1, or CE2 that enables the device. Device deselection occurs with the first edge of CE0, CE1, or CE2 that disables the device (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30).
RP#	Input	**RESET:** RP#-low resets internal automation and puts the device in power-down mode. RP#-high enables normal operation. Exit from reset sets the device to read array mode. When driven low, RP# inhibits write operations which provides data protection during power transitions.
OE#	Input	**OUTPUT ENABLE:** Activates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	Input	**WRITE ENABLE:** Controls writes to the CUI, the Write Buffer, and array blocks. WE# is active low. Addresses and data are latched on the rising edge of WE#.
STS	Open Drain Output	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default), it acts as a RY/BY# signal. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. For alternate configurations of the Status signal, see the Configurations command and Section 9.7, "Status Signal" on page 41. STS is to be tied to VCCQ with a pull-up resistor.
BYTE#	Input	**BYTE ENABLE:** BYTE#-low places the device in x8 mode; data is input or output on D[7:0], while D[15:8] is placed in High-Z. Address A0 selects between the high and low byte. BYTE#-high places the device in x16 mode, and turns off the A0 input buffer, the address A1 becomes the lowest-order address bit.
VPEN	Input	**ERASE / PROGRAM / BLOCK LOCK ENABLE:** For erasing array blocks, programming data, or configuring lock-bits. With $V_{PEN} \le V_{PENLK}$, memory contents cannot be altered.
VCC	Power	**CORE Power Supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \le V_{Lko}$. Caution: Device operation at invalid Vcc voltages should not be attempted.
VCCQ	Power	**I/O Power Supply:** Power supply for Input/Output buffers.This ball can be tied directly to V_{CC}.
VSS	Supply	**GROUND:** Ground reference for device logic voltages. Connect to system ground.
NC	—	**No Connect:** Lead is not internally connected; it may be driven or floated.
RFU	—	**Reserved for Future Use:** Balls designated as RFU are reserved by Numonyx for future device functionality and enhancement.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Numonyx sales office that you have the latest datasheet before finalizing a design.

Table 4: Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Temperature under Bias Expanded (T_A, Ambient)	–40	+85	°C	—
Storage Temperature	–65	+125	°C	—
VCC Voltage	–2.0	+5.6	V	2
VCCQ Voltage	–2.0	+5.6	V	2
Voltage on any input/output signal (except VCC, VCCQ)	–2.0	V_{CCQ} (max) + 2.0	V	1
I_{SH} Output Short Circuit Current	—	100	mA	3

Notes:
1. Voltage is referenced to V_{SS}. During infrequent non-periodic transitions, the voltage potential between V_{SS} and input/output pins may undershoot to –2.0 V for periods < 20 ns or overshoot to V_{CCQ} (max) + 2.0 V for periods < 20 ns.
2. During infrequent non-periodic transitions, the voltage potential between V_{CC} and the supplies may undershoot to –2.0 V for periods < 20 ns or V_{SUPPLY} (max) + 2.0 V for periods < 20 ns.
3. Output shorted for less than one second. No more than one output pin/ball can be shorted at a time.

5.2 Operating Conditions

Warning: Operations beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 5: Temperature and V_{CC} Operating Condition

Symbol	Parameter	Min	Max	Unit	Test Condition
T_A	Operating Temperature	-40.0	+85	°C	Ambient Temperature
V_{CC}	VCC Supply Voltage	2.70	3.6	V	—
V_{CCQ}	VCCQ Supply Voltage	2.70	3.6	V	—

5.3 Power-Up/ Down

This section provides an overview of system level considerations with regards to the flash device. It includes a brief description of power-up/down sequence and decoupling design considerations.

5.3.1 Power-Up/ Down Sequence

To prevent conditions that could result in spurious program or erase operations, the power-up/power-down sequence shown in Table 6 is recommended. For DC voltage characteristics refer to Table 8. Note that each power supply must reach its minimum voltage range before applying/removing the next supply voltage.

Table 6: Power-Up/Down Sequence

Power Supply Voltage	Power-Up Sequence				Power-Down Sequence			
$V_{CC(min)}$	1st	1st	1st(1)	Sequencing not required(1)	3rd	2nd	2nd(1)	Sequencing not required(1)
$V_{CCQ(min)}$	2nd	2nd(1)			2nd	1st(1)		
$V_{PEN(min)}$	3rd		2nd		1st		1st	

Note:
1. Power supplies connected or sequenced together.

Device inputs must not be driven until all supply voltages reach their minimum range. RP# should be low during power transitions.

5.3.2 Power Supply Decoupling

When the device is enabled, many internal conditions change. Circuits are energized, charge pumps are switched on, and internal voltage nodes are ramped. All of this internal activities produce transient signals. The magnitude of the transient signals depends on the device and system loading. To minimize the effect of these transient signals, a 0.1 µF ceramic capacitor is required across each VCC/VSS and VCCQ signal. Capacitors should be placed as close as possible to device connections.

Additionally, for every eight flash devices, a 4.7 µF electrolytic capacitor should be placed between VCC and VSS at the power supply connection. This 4.7 µF capacitor should help overcome voltage slumps caused by PCB trace inductance.

5.4 Reset

By holding the flash device in reset during power-up and power-down transitions, invalid bus conditions may be masked. The flash device enters reset mode when RP# is driven low. In reset, internal flash circuitry is disabled and outputs are placed in a high-impedance state. After return from reset, a certain amount of time is required before the flash device is able to perform normal operations. After return from reset, the flash device defaults to asynchronous page mode. If RP# is driven low during a program or erase operation, the program or erase operation will be aborted and the memory contents at the aborted block or address are no longer valid. See Figure 12, “AC Waveform for Reset Operation” on page 28 for detailed information regarding reset timings.

6.0 Electrical Characteristics

6.1 DC Current Specifications

Table 7: DC Current Characteristics

V_{CCQ}		2.7 - 3.6V			Test Conditions	Notes
V_{CC}		2.7 - 3.6V				
Symbol	**Parameter**	**Typ**	**Max**	**Unit**		
I_{LI}	Input and V_{PEN} Load Current	—	±1	µA	V_{CC} = V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{LO}	Output Leakage Current	—	±10	µA	V_{CC}= V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{CCS}	V_{CC} Standby Current	50	120	µA	CMOS Inputs, V_{CC} = V_{CC} Max; Vccq = VccqMax Device is disabled (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30), RP# = V_{CCQ} ± 0.2 V	1,2,3
		0.71	2	mA	TTL Inputs, V_{CC} = V_{CC} Max, Vccq = VccqMax Device is disabled (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30), RP# = V_{IH}	
I_{CCD}	V_{CC} Power-Down Current	50	120	µA	RP# = V_{SS} ± 0.2 V, I_{OUT} (STS) = 0 mA	—
I_{CCR}	8-Word Page	15	20	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. Device is enabled (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30) f = 5 MHz, I_{OUT} = 0 mA	1,3
		30	54	mA	CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. Device is enabled (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30) f = 33 MHz, I_{OUT} = 0 mA	
I_{CCW}	V_{CC} Program or Set Lock-Bit Current	35	60	mA	CMOS Inputs, V_{PEN} = V_{CC}	1,4
		40	70	mA	TTL Inputs, V_{PEN} = V_{CC}	
I_{CCE} I_{CCBC}	V_{CC} Block Erase or V_{CC} Blank Check or Clear Block Lock-Bits Current	35	70	mA	CMOS Inputs, V_{PEN} = V_{CC}	1,4
		40	80	mA	TTL Inputs, V_{PEN} = V_{CC}	
I_{CCWS} I_{CCES}	V_{CC} Program Suspend or Block Erase Suspend Current	—	10	mA	Device is enabled (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30)	1,5

Notes:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Numonyx or your local sales office for information about typical specifications.
2. Includes STS.
3. CMOS inputs are either V_{CC} ± 0.2 V or V_{SS} ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
4. Sampled, not 100% tested.
5. I_{CCWS} and I_{CCES} are specified with the device selected. If the device is read or written while in erase suspend mode, the device's current draw is I_{CCR} and I_{CCWS}.

6.2 DC Voltage specifications

Table 8: DC Voltage Characteristics

V_{CCQ}		2.7 - 3.6 V			Test Conditions	Notes
V_{CC}		2.7 - 3.6 V				
Symbol	**Parameter**	**Min**	**Max**	**Unit**		
V_{IL}	Input Low Voltage	–0.5	0.8	V	—	2, 5, 6
V_{IH}	Input High Voltage	2.0	V_{CCQ} + 0.5	V	—	2, 5, 6
V_{OL}	Output Low Voltage	—	0.4	V	V_{CC} = V_{CC}Min V_{CCQ} = V_{CCQ} Min I_{OL} = 2 mA	1, 2
		—	0.2	V	V_{CC} = V_{CC}Min V_{CCQ} = V_{CCQ} Min I_{OL} = 100 µA	
V_{OH}	Output High Voltage	0.85 × V_{CCQ}	—	V	V_{CC} = V_{CCMIN} V_{CCQ} = V_{CCQ} Min I_{OH} = –2.5 mA	1, 2
		V_{CCQ} – 0.2	—	V	V_{CC} = V_{CCMIN} V_{CCQ} = V_{CCQ} Min I_{OH} = –100 µA	
V_{PENLK}	V_{PEN} Lockout during Program, Erase and Lock-Bit Operations	—	2.2	V	—	2, 3
V_{PENH}	V_{PEN} during Block Erase, Program, or Lock-Bit Operations	2.7	3.6	V	—	3
V_{LKO}	V_{CC} Lockout Voltage	—	2.0	V	—	4

Notes:
1. Includes STS.
2. Sampled, not 100% tested.
3. Block erases, programming, and lock-bit configurations are inhibited when $V_{PEN} \le V_{PENLK}$, and not guaranteed in the range between V_{PENLK} (max) and V_{PENH} (min), and above V_{PENH} (max).
4. Block erases, programming, and lock-bit configurations are inhibited when $V_{CC} \le V_{LKO}$, and not guaranteed in the range between V_{LKO} and V_{CC} (min), and above V_{CC} (max).
5. Includes all operational modes of the device.
6. Input/Output signals can undershoot to -1.0V referenced to V_{SS} and can overshoot to V_{CCQ} + 1.0V for duration of 2ns or less, the V_{CCQ} valid range is referenced to V_{SS}.

6.3 Capacitance

Table 9: Capacitance

Symbol	Parameter[1]	Type	Max	Unit	Condition[2]
C_{IN}	Input Capacitance	6	7	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	4	5	pF	V_{OUT} = 0.0 V

Notes:
1. Sampled, not 100% tested.
2. T_A = -40 °C to +85 °C, V_{CC}= V_{CCQ}= 0 to 3.6 V.

7.0 AC Characteristics

Timing symbols used in the timing diagrams within this document conform to the following convention.

Figure 7: Timing Signal Naming Convention

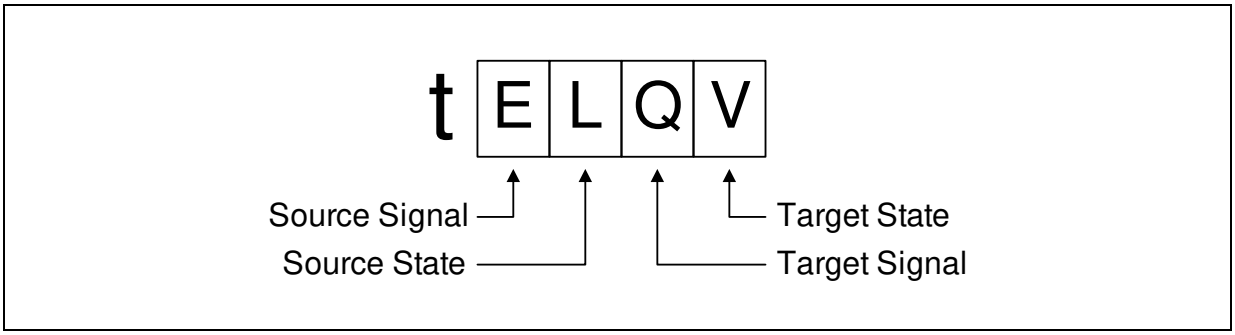


Table 10: Timing Signal Name Decoder

Signal	Code	State	Code
Address	A	High	H
Data - Read	Q	Low	L
Data - Write	D	High-Z	Z
Chip Enable (CE)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Status (STS)	R		
Reset (RP#)	P		
Byte Enable (BYTE#)	F		
Erase/Program/Block Lock Enable (V_{PEN})	V		

Note: Exceptions to this convention include t_{ACC} and t_{APA}. t_{ACC} is a generic timing symbol that refers to the aggregate initial-access delay as determined by t_{AVQV}, t_{ELQV}, and t_{GLQV} (whichever is satisfied last) of the flash device. t_{APA} is specified in the flash device's data sheet, and is the address-to-data delay for subsequent page-mode reads.

7.1 Read Specifications

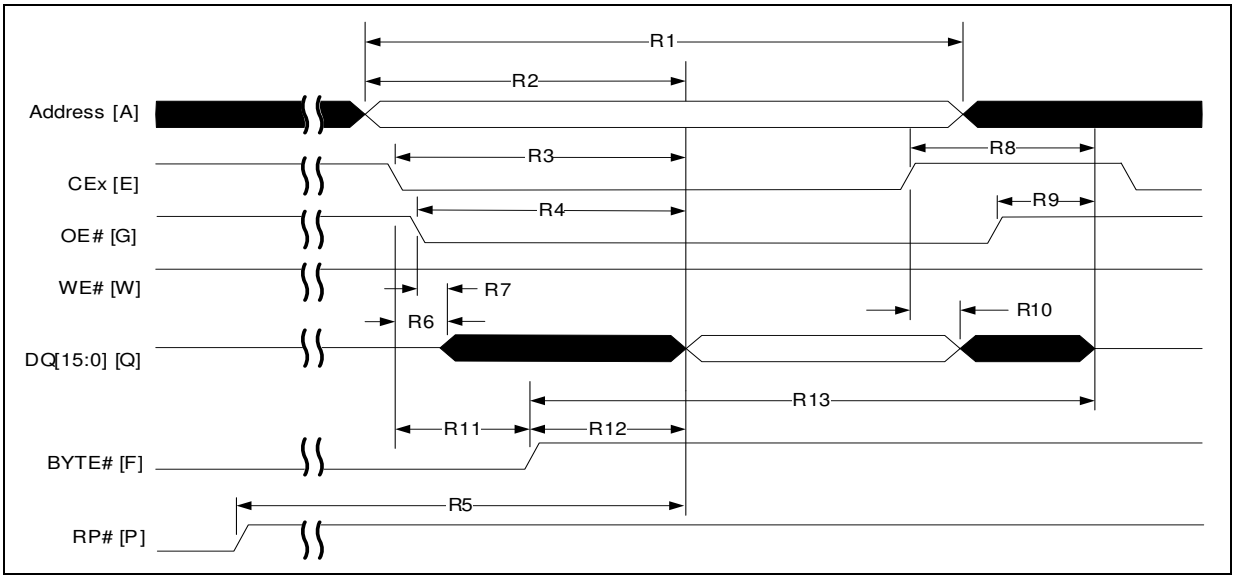
Table 11: Read Operations

Asynchronous Specifications V_{CC} = 2.7 V–3.6 V (3) and V_{CCQ} = 2.7 V–3.6 V (3)							
#	**Sym**	**Parameter**	**Density**	**Min**	**Max**	**Unit**	**Notes**
R1	t_{AVAV}	Read/Write Cycle Time	All	75	—	ns	1,2
R2	t_{AVQV}	Address to Output Delay		—	75	ns	1,2
R3	t_{ELQV}	CEx to Output Delay		—	75	ns	1,2
R4	t_{GLQV}	OE# to Non-Array Output Delay		—	25	ns	1,2,4
R5	t_{PHQV}	RP# High to Output Delay	32 Mbit	—	150	ns	1,2
			64 Mbit	—	180		1,2
			128 Mbit	—	210		1,2
R6	t_{ELQX}	CEx to Output in Low Z	All	0	—	ns	1,2,5
R7	t_{GLQX}	OE# to Output in Low Z		0	—	ns	1,2,5
R8	t_{EHQZ}	CEx High to Output in High Z		—	25	ns	1,2,5
R9	t_{GHQZ}	OE# High to Output in High Z		—	15	ns	1,2,5
R10	t_{OH}	Output Hold from Address, CEx, or OE# Change, Whichever Occurs First		0	—	ns	1,2,5
R11	t_{ELFL}/t_{ELFH}	CEx Low to BYTE# High or Low		—	10	ns	1,2,5
R12	t_{FLQV}/t_{FHQV}	BYTE# to Output Delay		—	1	µs	1,2
R13	t_{FLQZ}	BYTE# to Output in High Z		—	1	µs	1,2,5
R14	t_{EHEL}	CEx High to CEx Low		0	—	ns	1,2,5
R15	t_{APA}	Page Address Access Time		—	25	ns	5, 6
R16	t_{GLQV}	OE# to Array Output Delay		—	25	ns	1,2,4

Notes:

1. CE_X low is defined as the combination of pins CE0, CE1 and CE2 that enable the device. CE_X high is defined as the combination of pins CE0, CE1, and CE2 that disable the device (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30).
2. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.
3. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE_X (see note 1 and Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30) without impact on t_{ELQV}.
4. See Figure 13, "AC Input/Output Reference Waveform" on page 29 and Figure 14, "Transient Equivalent Testing Load Circuit" on page 29 for testing characteristics.
5. Sampled, not 100% tested.
6. For devices configured to standard word/byte read mode, R15 (t_{APA}) will equal R2 (t_{AVQV}).

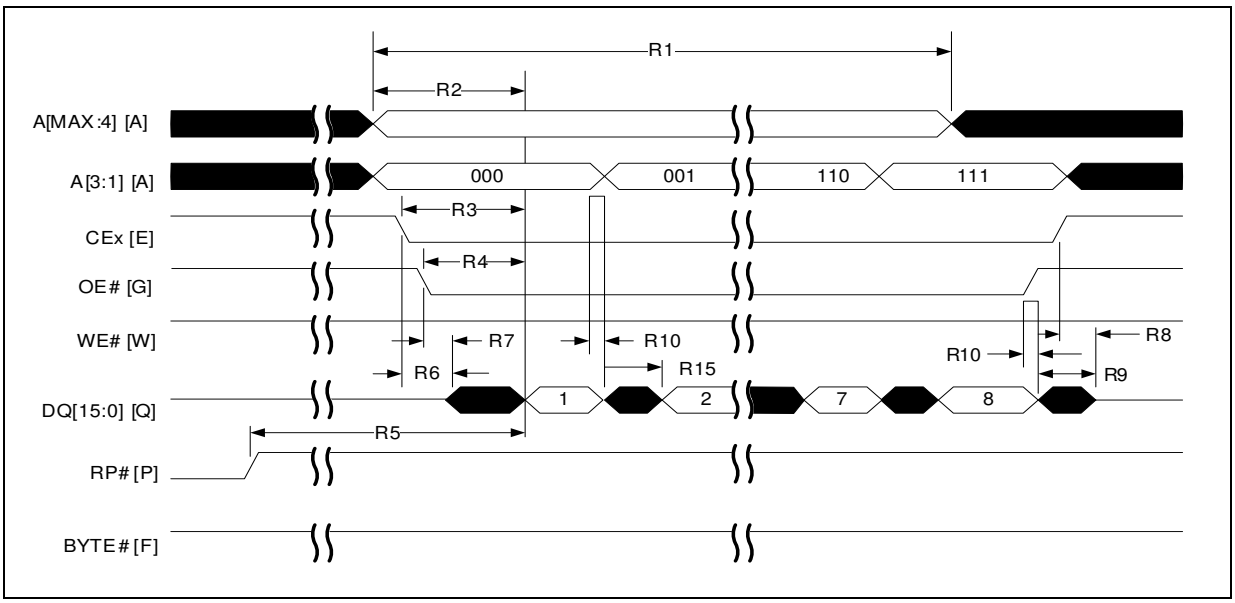
Figure 8: Single-Word Asynchronous Read Waveform



Notes:

1. CE_X low is defined as the combination of pins CE0, CE1, and CE2 that enable the device. CE_X high is defined as the combination of pins CE0, CE1, and CE2 that disable the device (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30).
2. When reading the flash array a faster t_{GLQV} (R16) applies. For non-array reads, R4 applies (i.e., Status Register reads, query reads, or device identifier reads).

Figure 9: 8-Word Asynchronous Page Mode Read



Notes:

1. CE_X low is defined as the combination of pins CE0, CE1, and CE2 that enable the device. CE_X high is defined as the combination of pins CE0, CE1, and CE2 that disable the device (see Table 17, "Chip Enable Truth Table for 32-, 64-, 128-Mb" on page 30).
2. In this diagram, BYTE# is asserted high.