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Cyclone III 3C120 Development Board

Reference Manual

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Contents

Additional Information

1. Overview

Introduction

This document describes the hardware features of the Cyclone® III development board, including detailed pin-out information to enable you to create custom FPGA designs that interface with all components of the board.

For information about setting up and powering up the Cyclone III development board and using the kit's demo software, refer to the *Cyclone III Development Kit User Guide*.

General Description

The Cyclone® III development board provides a hardware platform for developing and prototyping low-power, high-volume, and feature-rich designs as well as to demonstrate the Cyclone III device's on-chip memory, embedded multipliers, and the Nios® II embedded processor.

With up to 4 Mbits of embedded memory and 288 embedded 18-bit × 18-bit multipliers, the Cyclone III device supplies internal memory while also providing external support for high-speed, low-latency memory access via dual-channel DDR SDRAM and low-power SRAM.

Built on TSMC's 65-nm low-power process technology, Cyclone III devices are designed to provide low static and dynamic power consumption. Additionally, with the support of the Quartus® II software's PowerPlay technology, designs are automatically optimized for power consumption. Therefore, the Cyclone III development board provides a power-optimized, integrated solution for memory-intensive, high-volume applications.

Accordingly, the Cyclone III development board is especially suitable for wireless, video and image processing, and other high-bandwidth, parallel processing applications. Through the use of Altera®-provided video and image intellectual property (or other MegaCore® functions) and board expansion connectors, you can enable the inter-operability of the Cyclone III device, allowing application-specific customization of the development board.

For more information about the Altera Video and Image Processing Suite MegaCore functions, refer to the *Video and Image Processing Suite User Guide*.

To get you started, Altera provides application-specific design examples. The pre-built and tested design examples allow you to:

- Create a Cyclone III FPGA design in an hour
- View Cyclone III FPGA power measurement examples
- Design a 32-bit soft processor system inside the Cyclone III FPGA in an hour

The Cyclone III development board has the following main features:

- High logic density to implement more functions and features
- Embedded memory for high-bandwidth applications
- Expandable through two Altera High-Speed Mezzanine Connectors (HSMCs)
- 256-MB of dual channel DDR2 SDRAM with a 72-bit data width
- Supports high-speed external memory interfaces including dual-channel DDR SDRAM and low-power SRAM
- Four user push-button switches
- Eight user LEDs
- Power consumption display

The Cyclone III development board provides the following advantages:

- Unique combination of low-cost, low-power Cyclone III FPGA that supports high-volume, memory-intensive designs
- Highest multiplier-to-logic ratio FPGA in the industry
- Lowest cost, density- and power-optimized FPGA
- Quartus II development software's power optimization tools

Board Component Blocks

The board features the following major component blocks:

- 780-pin Altera Cyclone III EP3C120 FPGA in a BGA package
  - 119K logic elements (LEs)
  - 3,888 Kbits of memory
  - 288 18 × 18 multiplier blocks
  - Four phase locked loops (PLLs)
  - 20 global clock networks
  - 531 user I/Os
  - 1.2-V core power
- 256-pin Altera MAX® II EPM2210G CPLD in a FineLine Ball Grid Array (FBGA) package
  - 1.8-V core power
- On-board memory
  - 256-MB dual-channel DDR2 SDRAM
  - 8-MB SRAM
  - 64-MB flash memory

- FPGA configuration circuitry
  - MAX II CPLD and flash passive serial configuration
  - On-board USB-Blaster™ circuitry using the Quartus II Programmer
- On-board clocking circuitry
  - Two clock oscillators to support Cyclone III device user logic
    - 50 MHz
    - 125 MHz
  - 80 I/O, 6 clocks, SMBus, and JTAG
  - SMA connector for external clock input and output
- General user and configuration interfaces
  - LEDs/displays:
    - Eight user LEDs
    - One transmit/receive LED (TX/RX) per HSMC interface
    - One configuration done LED
    - Ethernet LEDs
    - User 7-segment display
    - Power consumption display
  - Memory activity LEDs:
    - SRAM
    - FLASH
    - DDR2 Top
    - DDR2 Bottom
  - Push-buttons:
    - One user reset push-button (CPU reset)
    - Four general user push-buttons
    - One system reset push-button (user configuration)
    - One factory push-button switch (factory configuration)
  - DIP switches:
    - One MAX control DIP switch
    - One JTAG control switch
    - Eight user DIP switches
    - Speaker header
- Displays
  - 128 × 64 graphics LCD
  - 16 × 2 line character LCD

- Power supply
  - 14 V – 20 V DC input
  - On-board power measurement circuitry
  - Up to 19.8 W per HSMC interface
- Mechanical
  - 6″ × 8″ board
  - Bench-top design

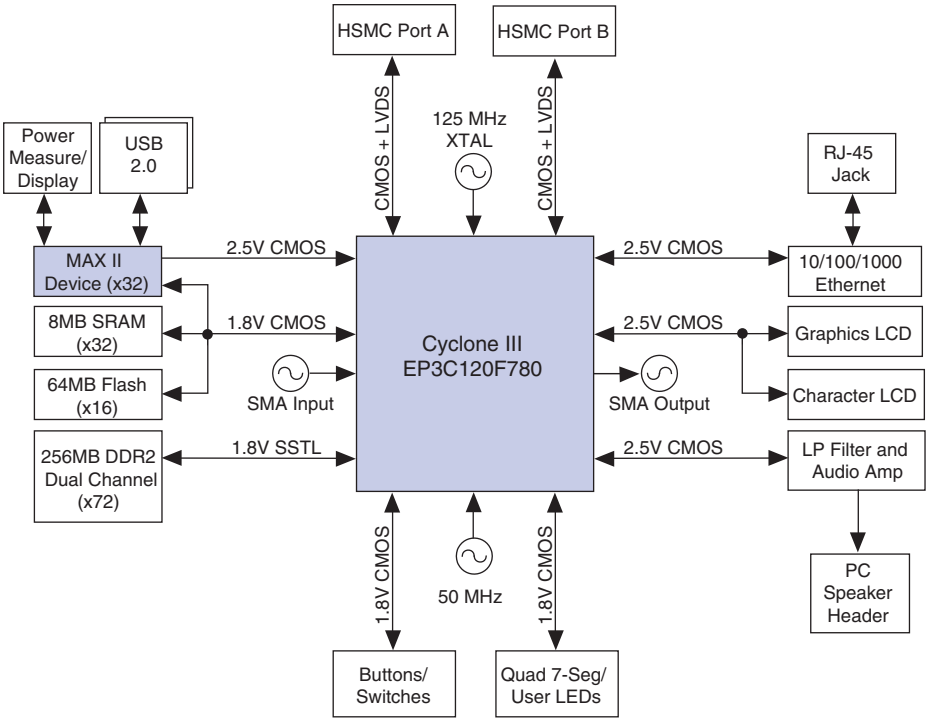
The Cyclone III FPGA Development Kit ships with additional HSMC daughter card loopback and break-out headers for convenient testing of some of the HSMC signals. For more details regarding these test daughter cards, refer to their respective schematics at these locations in the installed kit directory:

- *<path>***board_design_files\schematic\breakout_hsmc debug_header_breakout.pdf**
- *<path>***board_design_files\schematic\loopback_hsmc loopback_test_lowcost.pdf**

Block Diagram

Figure 1–1 shows the functional block diagram of the Cyclone III development board.

Figure 1–1. Cyclone III Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following precaution:

CAUTION

Static Discharge Precaution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces all the important components on the Cyclone III development board. Figure 2–1 illustrates all component locations and Table 2–1 describes component features.

The chapter is divided into the following sections:

A complete set of board schematics, a physical layout database, and GERBER files for the Cyclone III development board are installed in the Cyclone III Development Kit documents directory.

For information about powering up the development board and installing the demo software, refer to the *Cyclone III Development Kit User Guide*.

Board Overview

This section provides an overview of the Cyclone III development board, including an annotated board image and component descriptions.

Figure 2–1 shows the top view of the Cyclone III development board.

Figure 2–1. Top View of the Cyclone III Development Board

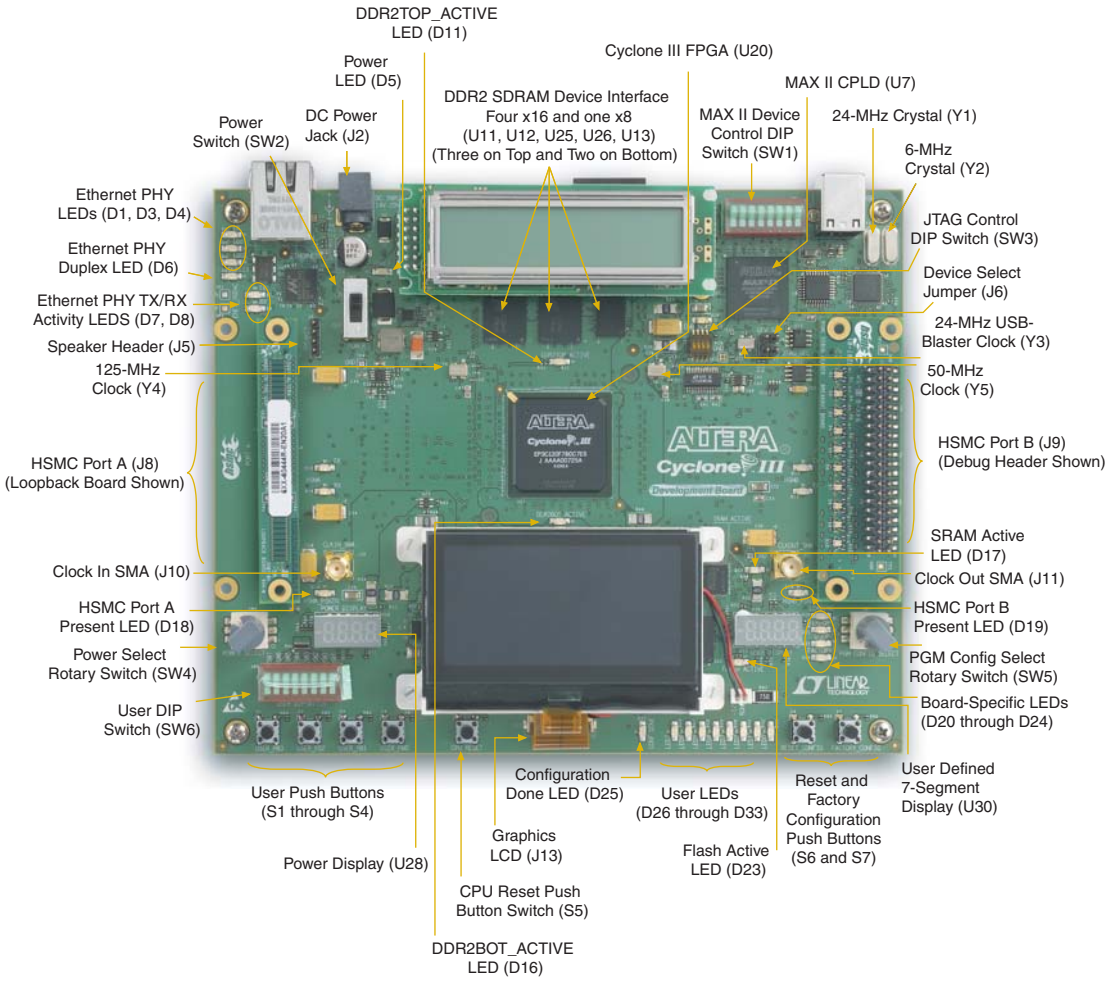


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Cyclone III Development Board (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U20	FPGA	EP3C120, 780-pin FineLine BGA package.
U7	CPLD	EPM2210G, 256-pin device in a FineLine BGA package.
Configuration Status and Setup Elements		
J6	Device select (`DEV_SEL`) jumper	Sets target device for JTAG signals when using an external USB-Blaster or equivalent.
J3	Input	Type B USB connector that allows for connecting a Type A-B USB cable between a PC and the board.
D20 through D24	User LEDs	Board-specific configuration green LEDs.
D25	Configuration done LED	Green LED that illuminates when the FPGA is successfully configured.
D12 through D15	Channel activity LEDs	Green LEDs that indicate the RX and TX activity on the HSMC Ports A or B.

Table 2–1. Cyclone III Development Board (Part 2 of 3)

Board Reference	Type	Description
J5	Header	Speaker header.
D1, D3, D4	Ethernet PHY LEDs	Green Ethernet PHY LEDs. Illuminate when Ethernet PHY is using the 10/100/1000 Mbps (D1, D3, D4) connection speeds.
D6	Duplex Ethernet PHY LED	Green Ethernet PHY LED. Illuminates when Ethernet PHY is both sending and receiving data.
D5	Power LED	Blue LED indicates when power is applied to the board.
D7, D8	Ethernet PHY transmit/receive activity LEDs	Green LED. Illuminates when transmit/receive data is active from the Ethernet PHY.
SW1	MAX II device control DIP switch	Controls various features specific to the Cyclone III development board.
SW3	JTAG control switch	JTAG control DIP switch used to remove or include devices in the active JTAG chain.
D17	SRAM active	SRAM active LED. Illuminates when the SRAM device is accessed.
D23	Flash active	Flash active LED. Illuminates when the flash device is accessed.
U28	Power display	Displays power measured by the MAX II CPLD.
D16	DDR2 LED	Indicates that the DDR2 top devices are active.
D11	DDR2 LED	Indicates that the DDR2 bottom devices are active.
Clock Circuitry		
Y4	125 MHz	125-MHz clock oscillator used for the system clock.
Y5	50 MHz	50-MHz clock oscillator used for data processing.
Y1	24-MHz crystal	Cypress USB PHY.
Y2	6-MHz crystal	USB PHY FTDI reference clock.
Y3	24 MHz	MAX II device clock.
J10	SMA clock input	SMA connector that allows the provision of an external clock input.
J11	SMA clock output	SMA connector that allows the provision of an external clock output.
General User Input and Output		
S1 through S4	User push buttons	Four 1.8-V push-button switches for user-defined, logic inputs.
S5	CPU reset push button	One 1.8-V push-button switch for FPGA logic and CPU reset.
S6 and S7	Reset and factory configuration push buttons	Two 1.8-V push-button switches that control FPGA configuration from flash memory.
D26 through D33	User LEDs	Eight user-defined LEDs.
SW5	PGM CONFIG SELECT	Rotary switch to select which FPGA configuration file to use in flash memory.
SW4	Power select rotary switch	Power rail select for on-board power monitor.
U30	User display	User-defined, green 7-segment display.
J4	Character LCD	14-pin LCD display.
J13	Graphics LCD	30-position dot matrix graphics LCD display.
Memory		
U31	Flash	64 MB of flash memory with a 16-bit data bus.

Table 2–1. Cyclone III Development Board (Part 3 of 3)

Board Reference	Type	Description
U23 and U24	SRAM	The SRAM devices connect to the MAX II device as well as the flash memory device.
U11, U12, U13, U25, U26	DDR2 SDRAM	Four ×16 devices and a single ×8 device.
Components and Interfaces		
U6	USB device	USB device that provides JTAG programming of on-board devices, including the Cyclone III device and flash memory device.
U3	Ethernet cable jack	The RF-45 jack is for Ethernet cable connection. The connector is fed by a 10/100/1000 base T PHY device with an RGMII interface to the Cyclone III device.
J8, J9	HSMC Port A and Port B	High-speed mezzanine header allows for the connection of HSMC daughter cards.
Power Supply		
J2	DC power jack	14–20 V DC power source.
SW2	Input	Switches the board's power on and off.

Featured FPGA (U20)

The Cyclone III Development Kit features the EP3C120F780 device (U20) in a 780-pin BGA package.

For more information about Cyclone III devices, refer to the *Cyclone III Device Handbook*.

Table 2–2 lists the main Cyclone III device features.

Table 2–2. Cyclone III Device Features

Feature	Quantity
Logic elements	119,088
Memory (Kbits)	3,888
Multipliers	288
PLLs	4
Global clock networks	20

Table 2–3 lists the Cyclone III component reference and manufacturing information.

Table 2–3. Cyclone III Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U20	Memory rich FPGA device	Altera Corporation	EP3C120F780	www.altera.com

Table 2–4 lists the Cyclone III EP3C120F780C7 device pin count.

Table 2–4. Cyclone III Device Pin Count

Function	I/O Type	I/O Count	Special Pins
Oscillators and SMAs	1.8-V CMOS	4	Three clock inputs, one output
DDR2	1.8-V SSTL	148	Nine data strobe signal (DQS), 10 V_{REF}
Flash/SRAM/MAX	1.8-V CMOS	78	—
Horizontal bank OCT calibration	1.8-V CMOS	4	2 Rup, 2 Rdn
Vertical bank OCT calibration	2.5-V CMOS	4	2 Rup, 2 Rdn
Passive serial configuration	2.5-V CMOS	2	DATA0, DCLK
Ethernet	2.5-V CMOS	16	1 clock input
Buttons, Switches, LEDs	1.8-V CMOS	34	DEV_CLR
Character LCD, Graphics LCD	2.5-V CMOS	14	—
Speaker header	2.5-V CMOS	1	—
USB	2.5-V CMOS	14	1 clock input
HSMC Port A	2.5-V CMOS 2.5-V LVDS	86	5 clock inputs (1 single-ended, 2 differential)
HSMC Port B	2.5-V CMOS 2.5-V LVDS	86	5 clock inputs (1 single-ended, 2 differential)
Device I/O total: 491			

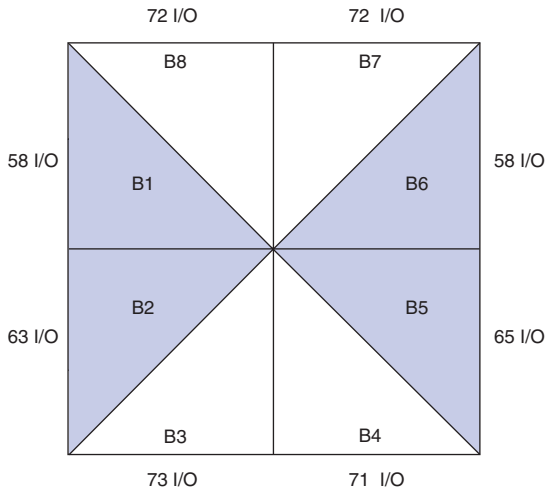
For additional information about Altera devices, go to www.altera.com/products/devices.

I/O and Clocking Resources

This section lists specific I/O and clocking resources available with the EP3C120F780C7 device, which is the largest of the Cyclone III devices.

Figure 2–2 illustrates the available I/O bank resources on the EP3C120F780C7 device.

Figure 2–2. Cyclone III Device I/O Bank Resources



MAX II CPLD

The board utilizes an Altera MAX II CPLD for the following purposes:

- Power-up configuration of the FPGA from flash memory
- Embedded USB-Blaster core for USB-based configuration of the FPGA
- Power consumption monitoring and display

There are two USB MAC/PHY devices— FTDI and Cypress USB PHY devices— on the board. They are muxed through the MAX II CPLD. Only one can operate at any time. The FTDI device is the default device and it supports the embedded blaster functionality. The Cypress USB PHY is held in reset and is reserved for future use. Each device has a shared path between the USB device and the MAX II CPLD. The individual paths then drive to the FPGA separately. Figure 2–3 illustrates the MAX II device's block diagram.

Figure 2–3. MAX II Device's Block Diagram

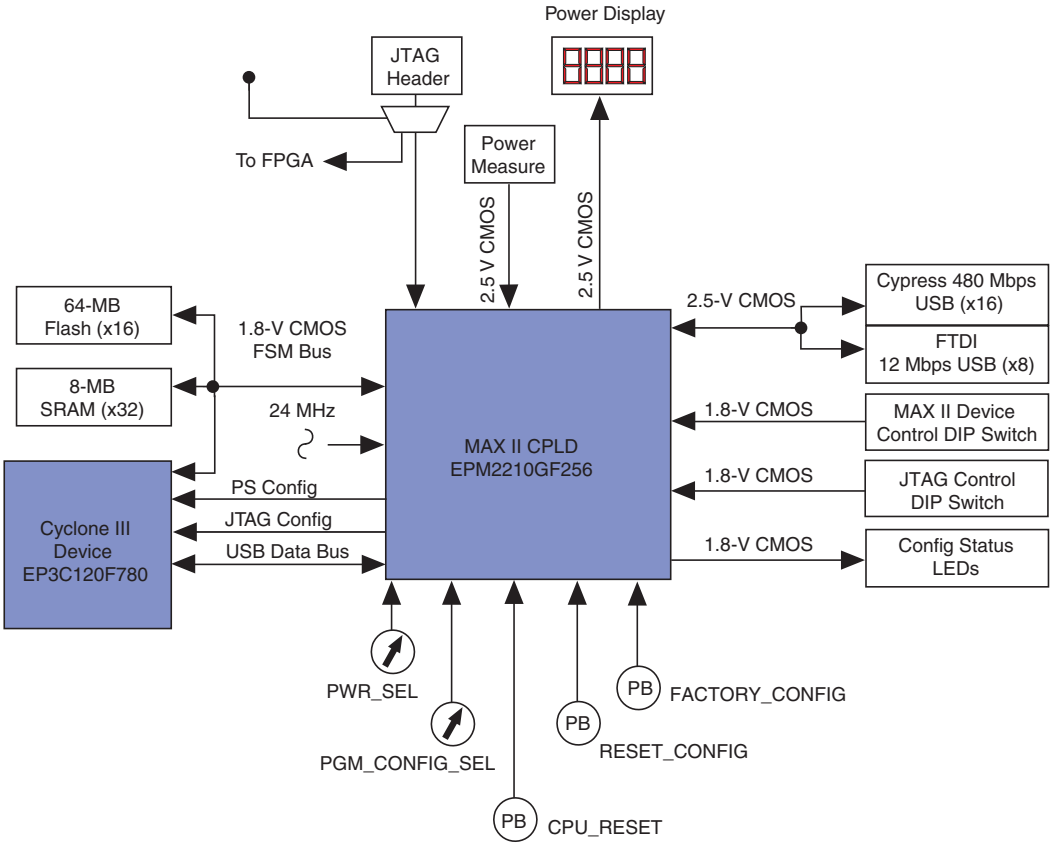


Table 2–5 lists the I/O signals present on the MAX II CPLD. The signal name and function are relative to the MAX II device.

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 1 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
P3	—	Input	TCK
L6	—	Input	TDI
M5	—	Output	TDO
N4	—	Input	TMS
C14	1.8 V	Output	CLKIN_125_EN
J12	1.8 V	Input	CLKIN_24
E13	1.8 V	Output	CLKIN_50_EN
M9	1.8 V	Input	CPU_RESETn
F11	1.8 V	Input	DEV_SEL
A10	2.5 V	Input	FACTORY_CONFIGn
G13	1.8 V	Output	FLASH_ACTIVE
L15	1.8 V	Output	FLASH_BYTEn
K14	1.8 V	Output	FLASH_CEn

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 2 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
M16	1.8 V	Output	FLASH_OEn
L11	1.8 V	Input	FLASH_RDYBSYn
M15	1.8 V	Output	FLASH_RESETn
L12	1.8 V	Output	FLASH_WEn
J16	1.8 V	Input	FPGA_BYPASS
E3	2.5 V	Input	FPGA_CONF_DONE
D3	2.5 V	Output	FPGA_DATA
C2	2.5 V	Output	FPGA_DCLK
N3	2.5 V	Input	FPGA_JTAG_TCK
N1	2.5 V	Output	FPGA_JTAG_TDI
N2	2.5 V	Input	FPGA_JTAG_TDO
P2	2.5 V	Input	FPGA_JTAG_TMS
E4	2.5 V	Output	FPGA_nCONFIG
C3	2.5 V	Input	FPGA_nSTATUS
N9	1.8 V	Output	FSA[0]
T8	1.8 V	Output	FSA[1]
N10	1.8 V	Output	FSA[10]
R11	1.8 V	Output	FSA[11]
P10	1.8 V	Output	FSA[12]
T12	1.8 V	Output	FSA[13]
M11	1.8 V	Output	FSA[14]
R12	1.8 V	Output	FSA[15]
N11	1.8 V	Output	FSA[16]
T13	1.8 V	Output	FSA[17]
P11	1.8 V	Output	FSA[18]
R13	1.8 V	Output	FSA[19]
T9	1.8 V	Output	FSA[2]
M12	1.8 V	Output	FSA[20]
R14	1.8 V	Output	FSA[21]
N12	1.8 V	Output	FSA[22]
T15	1.8 V	Output	FSA[23]
P12	1.8 V	Output	FSA[24]
R9	1.8 V	Output	FSA[3]
P9	1.8 V	Output	FSA[4]
T10	1.8 V	Output	FSA[5]
K16	1.8 V	Output	FSA[6]
R10	1.8 V	Output	FSA[7]
M10	1.8 V	Output	FSA[8]
T11	1.8 V	Output	FSA[9]

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 3 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
P4	1.8 V	Bidirectional	FSD[0]
R1	1.8 V	Bidirectional	FSD[1]
M6	1.8 V	Bidirectional	FSD[10]
R5	1.8 V	Bidirectional	FSD[11]
P7	1.8 V	Bidirectional	FSD[12]
T5	1.8 V	Bidirectional	FSD[13]
N7	1.8 V	Bidirectional	FSD[14]
R6	1.8 V	Bidirectional	FSD[15]
M7	1.8 V	Bidirectional	FSD[16]
T6	1.8 V	Bidirectional	FSD[17]
J15	1.8 V	Bidirectional	FSD[18]
R7	1.8 V	Bidirectional	FSD[19]
P5	1.8 V	Bidirectional	FSD[2]
P8	1.8 V	Bidirectional	FSD[20]
T7	1.8 V	Bidirectional	FSD[21]
N8	1.8 V	Bidirectional	FSD[22]
R8	1.8 V	Bidirectional	FSD[23]
F12	1.8 V	Bidirectional	FSD[24]
D16	1.8 V	Bidirectional	FSD[25]
F13	1.8 V	Bidirectional	FSD[26]
D15	1.8 V	Bidirectional	FSD[27]
F14	1.8 V	Bidirectional	FSD[28]
D14	1.8 V	Bidirectional	FSD[29]
T2	1.8 V	Bidirectional	FSD[3]
E12	1.8 V	Bidirectional	FSD[30]
C15	1.8 V	Bidirectional	FSD[31]
N5	1.8 V	Bidirectional	FSD[4]
R3	1.8 V	Bidirectional	FSD[5]
P6	1.8 V	Bidirectional	FSD[6]
R4	1.8 V	Bidirectional	FSD[7]
N6	1.8 V	Bidirectional	FSD[8]
T4	1.8 V	Bidirectional	FSD[9]
F7	GNDINT	Gnd	—
G6	GNDINT	Gnd	—
H7	GNDINT	Gnd	—
H9	GNDINT	Gnd	—
J8	GNDINT	Gnd	—
J10	GNDINT	Gnd	—
K11	GNDINT	Gnd	—

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 4 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
L10	GNDINT	Gnd	—
A1	GNDIO	Gnd	—
A16	GNDIO	Gnd	—
B2	GNDIO	Gnd	—
B15	GNDIO	Gnd	—
G7	GNDIO	Gnd	—
G8	GNDIO	Gnd	—
G9	GNDIO	Gnd	—
G10	GNDIO	Gnd	—
K7	GNDIO	Gnd	—
K8	GNDIO	Gnd	—
K9	GNDIO	Gnd	—
K10	GNDIO	Gnd	—
R2	GNDIO	Gnd	—
R15	GNDIO	Gnd	—
T1	GNDIO	Gnd	—
T16	GNDIO	Gnd	—
J13	1.8 V	Input	HSMA_BYPASS
M4	2.5 V	Output	HSMA_JTAG_TDI
K4	2.5 V	Input	HSMA_JTAG_TDO
H16	1.8 V	Input	HSMB_BYPASS
H1	2.5 V	Output	HSMAB_JTAG_TDI
B9	2.5 V	Input	HSMB_JTAG_TDO
E16	1.8 V	Input	JTAG_SEL
D9	2.5 V	Output	LCD_BS1
N16	1.8 V	Output	LCD_SERn
L16	1.8 V	Input	MAX_CSn
N14	1.8 V	Input	MAX_DIP[0]
M13	1.8 V	Input	MAX_DIP[1]
N15	1.8 V	Input	MAX_DIP[2]
L14	1.8 V	Input	MAX_DIP[3]
J5	2.5 V	Output	MAX_EMB
M8	1.8 V	Input	MAX_EN
J4	2.5 V	Output	MAX_ERROR
J3	2.5 V	Output	MAX_FACTORY
K1	2.5 V	Output	MAX_LOAD
K13	1.8 V	Input	MAX_OEn
M14	1.8 V	Input	MAX_RESERVE[0]
P14	1.8 V	Input	MAX_RESERVE[1]

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 5 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
K2	2.5 V	Output	MAX_USER
K15	1.8 V	Input	MAX_WEn
H12	1.8 V	Input	MAX2_CLK
M1	2.5 V	Input	MAXGP_JTAG_TCK
L4	2.5 V	Output	MAXGP_JTAG_TDI
L5	2.5 V	Input	MAXGP_JTAG_TDO
M2	2.5 V	Input	MAXGP_JTAG_TMS
N13	1.8 V	Input	MWATTS_MAMPS
H13	1.8 V	Input	PGM[0]
H15	1.8 V	Input	PGM[1]
H14	1.8 V	Input	PGM[2]
G16	1.8 V	Input	PGM[3]
J1	2.5 V	Output	PMON_CLK
J2	2.5 V	Output	PMON_CSN
H3	2.5 V	Bidir	PMON_DATA
H4	2.5 V	Output	PMON_SDI
H5	2.5 V	Output	PMON_SYNC
F6	2.5 V	Output	PWR_DIG_SEL[1]
F1	2.5 V	Output	PWR_DIG_SEL[2]
G3	2.5 V	Output	PWR_DIG_SEL[3]
G2	2.5 V	Output	PWR_DIG_SEL[4]
D2	2.5 V	Output	PWR_SEG_A
E5	2.5 V	Output	PWR_SEG_B
D1	2.5 V	Output	PWR_SEG_C
F3	2.5 V	Output	PWR_SEG_D
F5	2.5 V	Output	PWR_SEG_DP
E2	2.5 V	Output	PWR_SEG_E
F4	2.5 V	Output	PWR_SEG_F
E1	2.5 V	Output	PWR_SEG_G
F2	2.5 V	Output	PWR_SEG_MINUS
G4	2.5 V	Input	PWR_SEL[0]
G1	2.5 V	Input	PWR_SEL[1]
G5	2.5 V	Input	PWR_SEL[2]
H2	2.5 V	Input	PWR_SEL[3]
D13	—	—	RESERVED_INPUT
E14	—	—	RESERVED_INPUT
E15	—	—	RESERVED_INPUT
G12	—	—	RESERVED_INPUT
G14	—	—	RESERVED_INPUT

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 6 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
G15	—	—	RESERVED_INPUT
K12	—	—	RESERVED_INPUT
L13	—	—	RESERVED_INPUT
P13	—	—	RESERVED_INPUT
R16	—	Input	RESET_CONFIGn
F16	—	Output	SRAM_ACTIVE
F15	—	Input	SRAM_CSn
B3	2.5 V	Input	USB_CLKOUT
E10	2.5 V	Input	USB_CMD_DATA
B10	2.5 V	Output	USB_EMPTY
E9	2.5 V	Bidirectional	USB_FD[0]
A9	2.5 V	Bidirectional	USB_FD[1]
A8	2.5 V	Bidirectional	USB_FD[2]
B8	2.5 V	Bidirectional	USB_FD[3]
E8	2.5 V	Bidirectional	USB_FD[4]
A7	2.5 V	Bidirectional	USB_FD[5]
D8	2.5 V	Bidirectional	USB_FD[6]
B7	2.5 V	Bidirectional	USB_FD[7]
C9	2.5 V	Output	USB_FULL
J14	1.8 V	Input	USB_IFCLK
A2	2.5 V	Bidirectional	USB_PA0_INT0n
D5	2.5 V	Bidirectional	USB_PA1_INT1n
B1	2.5 V	Bidirectional	USB_PA2_SLOE
D4	2.5 V	Bidirectional	USB_PA3_WU2
L3	2.5 V	Bidirectional	USB_PA4_IF0ADR0
L1	2.5 V	Bidirectional	USB_PA5_IF0ADR1
K5	2.5 V	Bidirectional	USB_PA6_PKTEND
L2	2.5 V	Bidirectional	USB_PA7_SLCSn
A4	2.5 V	Input	USB_PHY_CMD_DATA
D6	2.5 V	Output	USB_PHY_EMPTY
C13	2.5 V	Bidirectional	USB_PHY_FD[0]
B16	2.5 V	Bidirectional	USB_PHY_FD[1]
E11	2.5 V	Bidirectional	USB_PHY_FD[10]
B12	2.5 V	Bidirectional	USB_PHY_FD[11]
C10	2.5 V	Bidirectional	USB_PHY_FD[12]
A12	2.5 V	Bidirectional	USB_PHY_FD[13]
D10	2.5 V	Bidirectional	USB_PHY_FD[14]
B11	2.5 V	Bidirectional	USB_PHY_FD[15]
C12	2.5 V	Bidirectional	USB_PHY_FD[2]

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 7 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
A15	2.5 V	Bidirectional	USB_PHY_FD[3]
D12	2.5 V	Bidirectional	USB_PHY_FD[4]
B14	2.5 V	Bidirectional	USB_PHY_FD[5]
C11	2.5 V	Bidirectional	USB_PHY_FD[6]
B13	2.5 V	Bidirectional	USB_PHY_FD[7]
D11	2.5 V	Bidirectional	USB_PHY_FD[8]
A13	2.5 V	Bidirectional	USB_PHY_FD[9]
C4	2.5 V	Output	USB_PHY_FULL
C7	2.5 V	Input	USB_PHY_IFCLK
E6	2.5 V	Input	USB_PHY_REn
B4	2.5 V	Input	USB_PHY_WEn
E7	2.5 V	Input	USB_PWR_ENn
C8	2.5 V	Output	USB_RDn
A11	2.5 V	Input	USB_REn
C6	2.5 V	Output	USB_RESETn
A5	2.5 V	Output	USB_RSTn
D7	2.5 V	Input	USB_RSTOUTn
B6	2.5 V	Input	USB_RXFn
B5	2.5 V	Output	USB_SI_WU
K3	2.5 V	Input	USB_TXEn
C5	2.5 V	Output	USB_WAKEUP
M3	2.5 V	Input	USB_WEn
A6	2.5 V	Output	USB_WR
F10	—	Power	VCCINT
G11	—	Power	VCCINT
H8	—	Power	VCCINT
H10	—	Power	VCCINT
J7	—	Power	VCCINT
J9	—	Power	VCCINT
K6	—	Power	VCCINT
L7	—	Power	VCCINT
C1	—	Power	VCCIO1
H6	—	Power	VCCIO1
J6	—	Power	VCCIO1
P1	—	Power	VCCIO1
A3	—	Power	VCCIO2
A14	—	Power	VCCIO2
F8	—	Power	VCCIO2
F9	—	Power	VCCIO2

Table 2–5. MAX II Device Pin-Out *(Note 1)* (Part 8 of 8)

MAX II Pin Number	I/O Standard	Signal Direction	Schematic Signal Name
C16	—	Power	VCCIO3
H11	—	Power	VCCIO3
J11	—	Power	VCCIO3
P16	—	Power	VCCIO3
L8	—	Power	VCCIO4
L9	—	Power	VCCIO4
T3	—	Power	VCCIO4
T14	—	Power	VCCIO4
P15	1.8 V	Input	VOLTS_WATTS

Note to Table 2–5:

(1) For more information about the MAX II pin-out, refer to the Altera website at www.altera.com/literature/lit-dp.jsp.

Table 2–6 lists the MAX II component reference and manufacturing information.

Table 2–6. MAX II Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U7	256-pin device in a FineLine Ball Grid Array (FBGA) package	Altera Corporation	EPM2210GF256C3N	www.altera.com

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements, and is divided into the following groups:

- "Configuration" on page 2–15
  - FPGA programming over USB
  - FPGA programming from flash memory
  - Flash programming over USB
- "Status Elements" on page 2–17
  - Board-specific LEDs
  - Power display
- "Setup Elements" on page 2–18
  - JTAG control DIP switch
  - MAX II device control DIP switch
  - System reset and configuration push buttons
  - POWER SELECT rotary switch
  - PGM CONFIG SELECT rotary switch
  - Speaker header

Configuration

This section discusses FPGA, flash memory, and MAX II device programming methods supported by the Cyclone III development board.

FPGA Programming Over USB

The FPGA can be configured at any time the board is powered on by using the USB 2.0 interface and the Quartus II Programmer in JTAG mode.

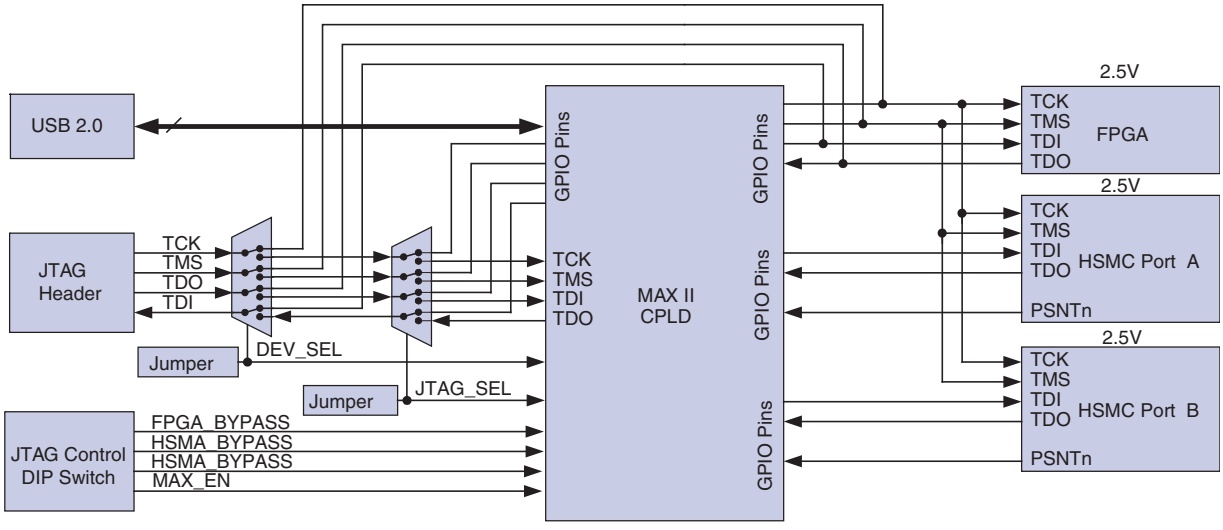
The JTAG chain is mastered by the embedded USB Blaster function found in the MAX II device. Only a USB cable is needed to program the Cyclone III FPGA. Any device can be bypassed by using the appropriate switch on the JTAG control DIP switch.

☞ Board reference SW1 position 5 (SW1.5), labeled `MAX0`, must be in the closed position (on) for this feature to properly work. If the SW1 switch is in the closed position, the parallel flash loader (PFL) megafunction in the MAX II CPLD may try to overwrite the FPGA image just downloaded over the USB immediately after completion.

For more information about:

- Advanced JTAG settings, refer to Table 2–7.
- The JTAG control switch, refer to "JTAG Control DIP Switch" on page 2–19.

Figure 2–4. JTAG Chain with the MAX II Device and the Cyclone III Device



The JTAG header can be used with an external USB-Blaster cable, or equivalent, to program either the MAX II CPLD or configure the Cyclone III FPGA. Most users of the Cyclone III development board do not use the JTAG header at all and instead use a USB cable along with the embedded USB-Blaster. Using an external USB-Blaster with the JTAG header requires disabling the embedded USB-Blaster function. See Table 2–7.