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VEEK-MT2-C5SOC

VEEK with Multi-touch Capacitive Panel

User Manual

CONTENTS

Chapter 1

Introduction of the VEEK-MT2-C5SOC

The Video and Embedded Evaluation Kit - Multi-touch Second Edition on Cyclone® V SOC Development Board (VEEK-MT2-C5SOC) is a comprehensive design environment with everything embedded developers need to create processing-based systems. VEEK-MT2-C5SOC delivers an integrated platform that includes hardware, design tools, intellectual property (IP) and reference designs for developing embedded software and hardware platform in a wide range of applications. The fully integrated kit allows developers to rapidly customize their processor and IP to best suit their specific application. The VEEK-MT2-C5SOC features the Altera Cyclone® V SoC development board targeting the Altera Cyclone® V SX SoC FPGA, as well as a capacitive LCD multimedia color touch panel which natively supports multi-touch gestures. An 8-megapixel digital image sensor, ambient light sensor, accelerometer, gyroscope, and magnetometer make up the rich feature-set.

The all-in-one embedded solution offered on the VEEK-MT2-C5SOC, in combination of the LCD touch panel and digital image module, provides embedded developers the ideal platform for multimedia applications with unparallel processing performance. Developers can benefit from the use of FPGA-based embedded processing system such as mitigating design risk and obsolescence, design reuse, reducing bill of material (BOM) costs by integrating powerful graphics engines within the FPGA, and lower cost.

Figure 1-1 shows a photograph of VEEK-MT2-C5SOC.

Figure 1-1 The VEEK-MT2-C5SOC board overview

The key features of the board are listed below:

1.1 Cyclone V SX SoC Development Board

- Cyclone V SX SoC—5CSXFC6D6F31C6N
  - 110K LEs, 41509 ALMs
  - 5140 M10K memory blocks
  - 224 18x18 Multiplier
  - 6 FPGA PLLs and 3 HPS PLLs.
- Configuration Sources
  - Active Serial (AS) x1 or x4 configuration (EPCQ256SI16N)
  - MAX® V CPLD (5M2210ZF256I5N) in a 256-pin FBGA package as the System Controller
  - Flash fast passive parallel (FPP) configuration
  - MAX II CPLD (EPM570GM100) as part of the embedded USB-BlasterTM II for use with the Quartus® II Programmer

- Memory Devices
  - One 1,024-Mbyte (MB) HPS DDR3 SDRAM with error correction code (ECC) support
  - One 1,024-MB FPGA DDR3 SDRAM
  - One 256-Megabit (Mb) quad serial peripheral interface (QSPI) flash

  - One 512-Mb CFI flash
  - One 32-Kb I2
  - C serial electrically erasable PROM (EEPROM)
  - One Micro SD flash memory card
- Switches and Indicators
  - LEDs and displays
  - Eight user LEDs
  - One configuration load LED
  - One configuration done LED
  - One error LED
  - Three configuration select LEDs
  - Four on-board USB-Blaster II status LEDs
  - One HSMC interface LED
  - Two UART data transmit and receive LEDs
  - One power on LED
  - One two-line character LCD display
  - Push buttons
  - One CPU reset push button
  - One MAX V reset push button
  - One program select push button
  - One program configuration push button
  - Six general user push buttons
  - DIP switches
  - One MAX V CPLD System Controller control switch
  - One JTAG chain control DIP switch
  - One mode select DIP switch
  - One general user DIP switch

- On-board Clocking Circuitry
  - Si570, Si571, and Si5338 programmable oscillators
  - 25-MHz, 50-MHz,100-MHz, 125-MHz, 148.50-MHz, and 156.25-MHz

- Oscillators
  - SMA input (LVCMOS)

- Communication Ports
  - One PCI Express x4 Gen1 socket
  - One universal HSMC port
  - One USB 2.0 on-the-go (OTG) port
  - One Gigabit Ethernet port
  - Dual 10/100 Ethernet ports
  - One SDI port (option for SMA connection)
  - One controller area network (CAN) port
  - One RS-232 UART (through the mini-USB port)
  - One real-time clock

- Power
  - 14–20-V (laptop) DC input

- Mechanical
  - 5.2" × 8.2" rectangular form factor

■ Capacitive LCD Touch Screen

- Equipped with an 7-inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module
- Module composed of LED backlight
- Support 24-bit parallel RGB interface
- Converting the X/Y coordination of touch point to its corresponding digital data via the Touch controller.

Table 1-1 shows the general physical specifications of the touch screen (Note*).

Table 1-1 General physical specifications of the LCD

Item	*Specification*	*Unit*
LCD size	7-inch (Diagonal)	-
Resolution	800 x3(RGB) x 480	dot
Dot pitch	0.1926(H) x0.1790 (V)	mm
Active area	154.08 (H) x 85.92 (V)	mm
Module size	164.9(H) x 100.0(V) x 5.7(D)	mm
Surface treatment	Glare	-
Color arrangement	RGB-stripe	-
Interface	Digital	-

■ 8-Megapixel Digital Image Sensor

- 8-Mega Pixels(3264x2448)
- Support Focus Control
- Automatic black level calibration (ABLC)
- Programmable controls for frame rate, mirror and flip, cropping, and windowing
- MIPI to Parallel Port Converter

Table 1-2 shows the key parameters of the CMOS sensor (Note*).

Table 1-2 Key performance parameters of the CMOS sensor

Parameter	*Value*
Active Pixels	3264Hx2448V

Pixel size	**1.4umx1.4um**
Color filter array	**RGB Bayer pattern**
Shutter type	**Global reset release(GRR)**
ADC resolution	**10-bit**
Pixel dynamic range	**68.8dB**
SNRMAX	**36.7dB**

■ Ambient Light Sensor

- Approximates human-eye response
- Precise luminance measurement under diverse lighting conditions
- Programmable interrupt function with user-defined upper and lower threshold settings
- 16-bit digital output with I2C fast-mode at 400 kHz
- Programmable analog gain and integration time
- 50/60-Hz lighting ripple rejection

■ Accelerometer Features

- Digital-output triple-axis accelerometer
- Programmable full scale range of ±2g, ±4g, ±8g and ±16g and integrated 16-bit
- Self-test

■ Gyrosope Features

- Digital-output X-, Y-, and Z-Axis angular rate sensors
- User-programmable full-scale range of ±250, ±500, ±1000, and ±2000°/sec
- Integrated 16-bit ADCs
- Self-test

■ Magnetometer

- 3-axis silicon monolithic Hall-effect magnetic sensor with magnetic concentrator
- Wide dynamic measurement range and high resolution with lower current consumption
- Output data resolution of 14 bit (0.6μT/LSB) or 16 bit (15μT/LSB)
- Full scale measurement range is ±4800μT
- Magnetometer normal operating current: 280μA at 8Hz repetition rate
- Self-test


Note: for more detailed information of the LCD touch panel and CMOS sensor module, please refer to their datasheets respectively.

1.2 Getting Help

Here is the contact information should you encounter any problem:

- Terasic Technologies
- 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan
- Tel: +886-3-575-0880
- Email: support@terasic.com

Chapter 2

Architecture

This chapter describes the architecture of the VEEK-MT2-C5SOC including block diagram and components.

2.1 Layout and Components

The picture of the VEEK-MT2-C5SOC is shown in Figure 2-1 and Figure 2-2. It depicts the layout of the board and indicates the locations of the connectors and key components.

Figure 2-1 VEEK-MT2-C5SOC PCB and Component Diagram (top view)

Figure 2-2 VEEK-MT-C5SOC PCB and Component Diagram (bottom view)

2.2 Block Diagram of the VEEK-MT2-C5SOC

Figure 2-3 gives the block diagram of the VEEK-MT2-C5SOC board. VEEK-MT2-C5SOC is a Cyclone V SoC development board and a Multi-touch LCD Camera Card (MTLC2) combination connected via the HSMC connector. MTLC2 module is not only equipped with a 5-point touch 7"LCD screen, it also equips an 8-Megapixel digital image sensor module, light sensor, accelerometer, gyroscope, and magnetometer. All these sensors connect to the FPGA device via the HSMC connector, so they can be controlled and directly used by the FPGA device.

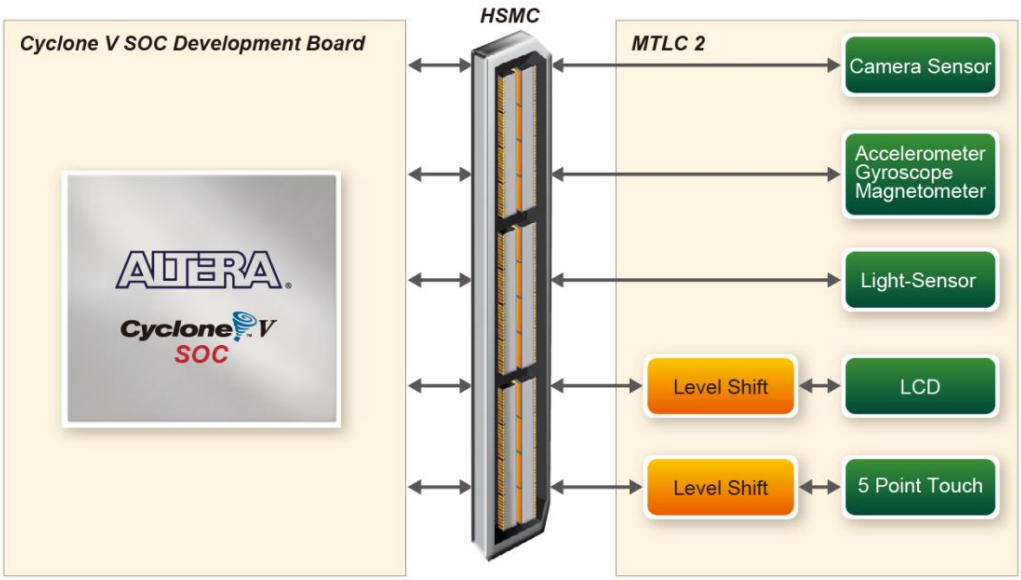

Figure 2-3 Block Diagram of VEEK-MT2-C5SOC

Chapter 3

Using VEEK-MT2-C5SOC

This section describes the detailed information of the components, connectors, and pin assignments of the VEEK-MT2-C5SOC.

3.1 Using the Cyclone® V SX SoC FPGA

The VEEK-MT-C5SOC is composed of Cyclone V SoC development board and 7" touch panel daughter card. In this combination, the Cyclone V SoC development board which equips the FPGA device is considered as the main part. Therefore, it can refer to the User Guide (http://www.altera.com/literature/ug/ug_cv_soc_dev_kit.pdf) of Cyclone V SoC development board on the FPGA device configuration and board setup.

3.2 Using the 7” LCD Capacitive Touch Screen

The VEEK-MT2-C5SOC features a 7-inch capacitive amorphous TFT-LCD panel. The LCD touch screen offers resolution of (800x480) to provide users the best display quality for developing applications. The LCD panel supports 24-bit parallel RGB data interface.

The VEEK-MT2-C5SOC is also equipped with a Touch controller, which can read the coordinates of the touch points through the I2C of the Touch controller.

To display images on the LCD panel correctly, the RGB color data along with the data enable and clock signals must act according to the timing specification of the LCD touch panel as shown in Table 3-1 and Table 3-2. Table 3- gives the pin assignment information of the LCD touch panel.

Table 3-1 LCD Horizontal timing specifications

Item	*Symbol*	*Typical Value*			*Unit*
		Min.	*Typ.*	*Max.*	
Horizontal Display Area	thd	-	800	-	DCLK
DCLK Frequency	fclk	26.4	33.3	46.8	MHz
One Horizontal Line	th	862	1056	1200	DCLK
HS pulse width	thpw	1		40	DCLK
HS Blanking	thb	46	46	46	DCLK
HS Front Porch	thfp	16	210	354	DCLK

Table 3-2 LCD Vertical timing specifications

Item	Symbol	Typical Value			Unit
		Min.	Typ.	Max.	
Horizontal Display Area	thd	-	800	-	DCLK
DCLK Frequency	fclk	26.4	33.3	46.8	MHz
One Horizontal Line	th	862	1056	1200	DCLK
HS pulse width	thpw	1		40	DCLK
HS Blanking	thb	46	46	46	DCLK
HS Front Porch	thfp	16	210	354	DCLK

Table 3-3 Pin assignment of the LCD touch panel

Signal Name	FPGA Pin No.	Description	I/O Standard
LCD_B0	C4	LCD blue data bus bit 0	2.5V
LCD_B1	D5	LCD blue data bus bit 1	2.5V
LCD_B2	A3	LCD blue data bus bit 2	2.5V
LCD_B3	A4	LCD blue data bus bit 3	2.5V
LCD_B4	E11	LCD blue data bus bit 4	2.5V
LCD_B5	F11	LCD blue data bus bit 5	2.5V
LCD_B6	F8	LCD blue data bus bit 6	2.5V
LCD_B7	F9	LCD blue data bus bit 7	2.5V
LCD_DCLK	E6	LCD Clock	2.5V
LCD_DE	C3	Data Enable signal	2.5V
LCD_DIM	F13	LCD backlight enable	2.5V
LCD_DITH	H8	Dithering setting	2.5V
LCD_G0	D12	LCD green data bus bit 0	2.5V
LCD_G1	E12	LCD green data bus bit 1	2.5V
LCD_G2	D10	LCD green data bus bit 2	2.5V
LCD_G3	D11	LCD green data bus bit 3	2.5V
LCD_G4	D9	LCD green data bus bit 4	2.5V
LCD_G5	E9	LCD green data bus bit 5	2.5V
LCD_G6	B5	LCD green data bus bit 6	2.5V
LCD_G7	B6	LCD green data bus bit 7	2.5V
LCD_HSD	C12	Horizontal sync input.	2.5V
LCD_MODE	G8	DE/SYNC mode select	2.5V
LCD_POWER_CTL	C2 (Note.)	LCD power control	2.5V
LCD_R0	A13	LCD red data bus bit 0	2.5V
LCD_R1	B13	LCD red data bus bit 1	2.5V
LCD_R2	C9	LCD red data bus bit 2	2.5V
LCD_R3	C10	LCD red data bus bit 3	2.5V

LCD_R4	B8	LCD red data bus bit 4	2.5V
LCD_R5	C8	LCD red data bus bit 5	2.5V
LCD_R6	A8	LCD red data bus bit 6	2.5V
LCD_R7	A9	LCD red data bus bit 7	2.5V
LCD_RSTB	B1	Global reset pin	2.5V
LCD_SHLR	B3	Left or Right Display Control	2.5V
LCD_UPDN	B2	Up / Down Display Control	2.5V
LCD_VSD	B11	Vertical sync input.	2.5V
TOUCH _I2C_SCL	F14	touch I2C clock	2.5V
TOUCH _I2C_SDA	F15	touch I2C data	2.5V
TOUCH _INT_n	B12	touch interrupt	2.5V
Note. The pin assignment is different from the VEEK-MT-C5SoC. In VEEK-MT-C5SOC, the LCD_POWER_CTL is assigned to PIN_G10.			

3.3 Using 8-megapixel Digital Image Sensor

VEEK-MT2-C5SoC board equips with an 8M pixel MIPI camera module named OV8865 (See Figure 3-1). The OV8865 color image sensor is a high performance, 8 megapixel RAW image sensor that delivers 3264x2448. It provides options for multiple resolutions while maintaining full field of view. Users can program image resolution, frame rate, and image quality parameters. Camera functions are controlled via I2C bus (CAMERA_I2C_SDA and CAMERA_I2C_SCL). The I2C device address is 0x6C. Table 3-5 contains the pin names and descriptions of the MPU-9250. For more hardware description and register information about this camera module, please refer to the datasheet named OV8865 Data Sheet.pdf in the VEEK-MT2-C5SoC System CD.

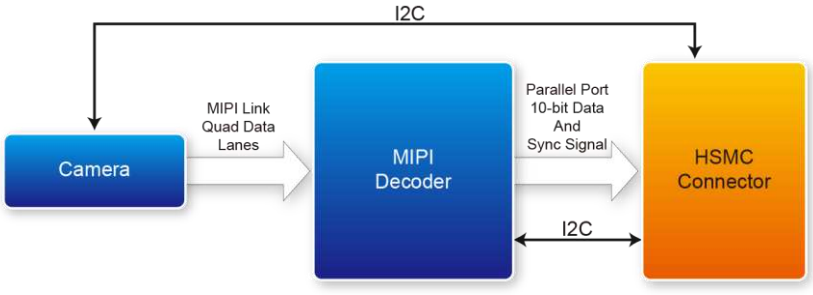

Figure 3-1 Block Diagram of the Bus Controller

■ Voice Coil Motor (VCM)

There is a Voice Coil Motor (VCM) driver chip named VCM149C on the MIPI camera module. Users can use the same I2C bus (I2C device address is 0x18) to modify the DAC value in the VCM driver chip that can allow the VCM to move its lens to the desired position for getting a sharp image and realizing the Auto Focus (AF) feature. Terasic also provides an AF demonstration and IP in the System CD, see section 4.6 for details. The datasheet of this VMC driver IC named VM149C VCM Driver IC.pdf also can be found in the System CD.

■ MIPI Decoder

The MIPI camera module output interface is MIPI interface, which cannot directly connect to the Terasic FPGA board; therefore, a MIPI Decoder (TC358748XBG) is added to convert MIPI interface to a parallel port interface. Decoder users can quickly obtain the image data and process it. MIPI Decoder can convert MIPI Interface up to 24-bit data. The Camera module used on the D8M can only output 10 bit data, MIPI_PIXEL_D[9:0] the HSMC connector is the camera image output data bus.

FPGA also can read/write MIPI Decoder through a I2C bus (MIPI_I2C_SDA / MIPI_I2C_SCL ; I2C device address is 0x1C), which is different from the camera module I2C bus. On the VEEK-MT2 board, MIPI Decoder can output clocks to the MIPI camera and FPGA board. So in the demonstrations, most of them show how to control IC PLL parameters as well as others. Detailed clock functions are described in blow.

■ Clock Tree

Figure 3-2 is the VEEK-MT2 board's camera clock tree block diagram. MIPI Decoder PLL receives FPGA Reference Clock (MIPI_REFCLK) and outputs Clock to Camera sensor (MCLK), at the same time, MIPI Decoder PLL will also output a parallel port clock (MIPI_PIXEL_CLK) and feedback to the FPGA to deal with parallel data.

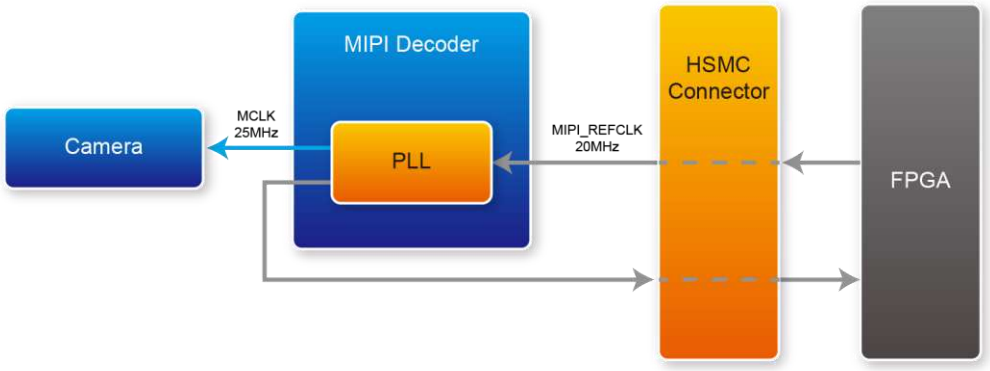

Figure 3-2 Clock Tree of Camera System

In the provided demonstrations, MIPI_REFCLK is set to 20MHz, FPGA transmits this clock to the VEEK-MT2-C5SoC's MIPI Decoder PLL through the HSMC connector. No matter how much the camera resolution is, the MCLK fixed output is 25MHz. According to the output resolution, MIPI_PIXEL_CLK can be set as 25MHz for 640x480@60fps and 50MHz for 1920x1080@15fps.

For more MIPI Decoder PLL setting details, please refer to "Chapter 5: Clock and System" in the datasheet TC358746AXBG_748XBG_rev09.pdf or refer to Terasic demonstrations.

■ Pin Assignment

Table 3- gives the pin assignment information of the Camera System.

Table 3-4 Pin assignment of the Camera System

Signal Name	FPGA Pin No.	Description	I/O Standard
MIPI_PIXEL_D[0]	H14	Parallel Port Data	2.5V
MIPI_PIXEL_D[1]	G13	Parallel Port Data	2.5V
MIPI_PIXEL_D[2]	K12	Parallel Port Data	2.5V
MIPI_PIXEL_D[3]	J12	Parallel Port Data	2.5V
MIPI_PIXEL_D[4]	J10	Parallel Port Data	2.5V
MIPI_PIXEL_D[5]	J9	Parallel Port Data	2.5V
MIPI_PIXEL_D[6]	K7	Parallel Port Data	2.5V
MIPI_PIXEL_D[7]	K8	Parallel Port Data	2.5V
MIPI_PIXEL_D[8]	G12	Parallel Port Data	2.5V
MIPI_PIXEL_D[9]	G11	Parallel Port Data	2.5V
MIPI_PIXEL_D[10]	F10	Reserve	2.5V
MIPI_PIXEL_D[11]	G10	Reserve	2.5V
MIPI_PIXEL_D[12]	AG1	Reserve	2.5V
MIPI_PIXEL_D[13]	AF8	Reserve	2.5V
MIPI_RESET_n	E8	Master Reset signal for MIPI camera and bridge device	2.5V
MIPI_PIXEL_CLK	AG2	Parallel Port Clock signal	2.5V
MIPI_PIXEL_HS	H7	Parallel Port Horizontal Synchronization signal	2.5V
MIPI_PIXEL_VS	J7	Parallel Port Vertical Synchronization signal	2.5V
MIPI_CS_n	D7	Chip Select	2.5V
MIPI_REFCLK	AJ2	Reference Clock Input of bridge device	2.5V
MIPI_I2C_SCL	AF9	I2C Clock for bridge device	2.5V

MIPI_I2C_SDA	AG7	I2C Data for bridge device	2.5V
MIPI_MCLK	AC12	MIPI camera system clock (Reserve)	2.5V
CAMERA_PWDN_n	C13	Power Down signal of MIPI camera	2.5V
CAMERA_I2C_SCL	E13	I2C Clock for MIPI camera	2.5V
CAMERA_I2C_SDA	E4	I2C Data for MIPI camera	2.5V

3.4 Using Gyroscope/Accelerometer/Magnetometer

The VEEK-MT2-C5SoC is equipped with a Motion-Tracking device named MPU-9250. The MPU-9250 is a 9-axis Motion-Tracking device that combines a 3-axis gyroscope, 3-axis accelerometer and 3-axis magnetometer. Detail features of these sensors are listed below:

■ Gyroscope

The MPU-9250 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

■ Accelerometer

The MPU-9250's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The MPU-9250's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0g on the X- and Y-axes and +1g on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2g, ±4g, ±8g, or ±16g.

■ Magnetometer

The 3-axis magnetometer uses highly sensitive Hall sensor technology. The magnetometer portion of the IC incorporates magnetic sensors for detecting terrestrial magnetism in the X-, Y-, and Z-Axes, a sensor driving circuit, a signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Each ADC has a 16-bit resolution and a full scale range of ±4800 μT.

Communication with all registers of the device is performed using either I2C at 400kHz or SPI at 1MHz. For applications requiring faster communications, the sensor and interrupt registers may be read using SPI at 20MHz. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD. 錯誤！找不到參照來源。**Table 3-5** contains the pin names and descriptions of the MPU-9250.gives the pin assignment information of the LCD touch panel. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

Table 3-5 contains the pin names and descriptions of the MPU-9250.

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
MPU_AD0_SDO	E1	I2C Slave Address LSB (AD0); SPI serial data output (SDO)	2.5V
MPU_CS_n	D4	Chip select (SPI mode only)	2.5V
MPU_FSYNC	E2	Frame synchronization digital input	2.5V
MPU_INT	E3	Interrupt digital output	2.5V
MPU_SCL_SCLK	D2	I2C serial clock (SCL); SPI serial clock (SCLK)	2.5V
MPU_SDA_SDI	D1	I2C serial data (SDA); SPI serial data input (SDI)	2.5V

3.5 Using the Ambient Light Sensor

The APDS-9300 is a low-voltage digital ambient light sensor that converts light intensity to digital signal output capable of direct I2C communication. Each device consists of one broadband photodiode (visible plus infrared) and one infrared photodiode. Two integrating ADCs convert the photodiode currents to a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where luminance (ambient light level) in lux is derived using an empirical formula to approximate the human-eye response. Table 3-6 contains the pin names and descriptions of the ambient light sensor module.gives the pin assignment information of the Ambient Light Sensor. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

Table 3-6 contains the pin names and descriptions of the ambient light sensor module.

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LSENSOR_ADDR_SEL	A6	Chip select	2.5V
LSENSOR_INT	B7	Interrupt output	2.5V
LSENSOR_SCL	A5	Serial Communications Clock	2.5V
LSENSOR_SDA	C7	Serial Data	2.5V

Chapter 4

VEEK-MT2-C5SOC Demonstrations

This chapter gives detailed description of the provided bundles of exclusive demonstrations implemented on VEEK-MT2-C5SOC. These demonstrations are particularly designed (or ported) for VEEK-MT2-C5SOC, with the goal of showing the potential capabilities of the kit and showcase the unique benefits of FPGA-based SOPC systems such as reducing BOM costs by integrating powerful graphics and video processing circuits within the FPGA.

4.1 System Requirements

To run and recompile the demonstrations, you should:

- Install Altera Quartus II 15.1 or a later edition on the host computer
- Install the USB-Blaster II driver software.
- Copy the entire demonstrations folder from the VEEK-MT2-C5SOC system CD to your host computer

4.2 Painter Demonstration

This chapter shows how to control LCD and touch controller to establish a paint demo based on Qsys and Altera VIP Suite. The demonstration shows how multi-touch gestures and single-touch coordinates operate.

Figure 4-1 shows the hardware system block diagram of this demonstration. For LCD display processing, the reference design is developed based on the Altera Video and Image Processing Suite (VIP). The Frame Reader VIP is used for reading display content from the associated video memory, and VIP Video Out is used to display the display content. The display content is filled by NIOS II processor according to users' input.

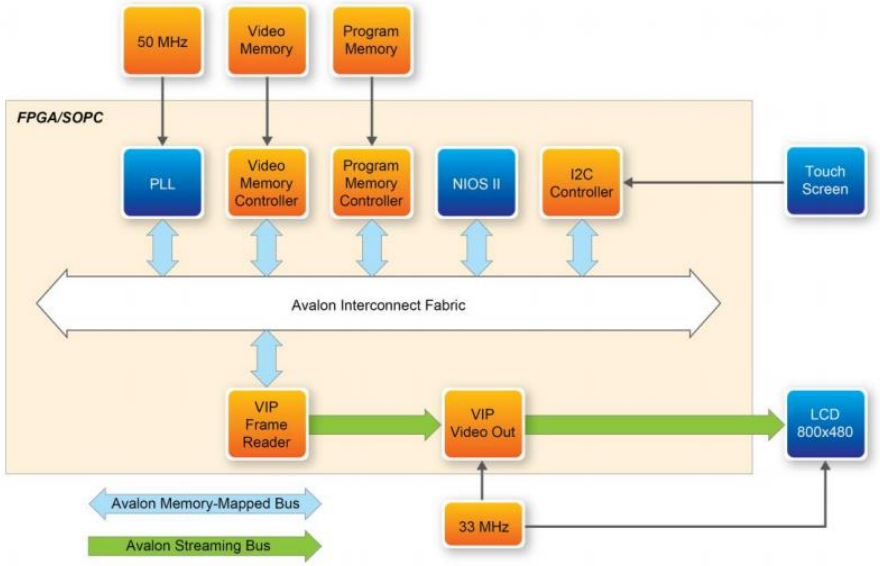

Figure 4-1 Block diagram of the Painter demonstration

■ Demonstration Source Code

- Project directory: Painter
- Bit stream used: Painter.sof
- Nios II Workspace: Painter \Software

■ Demonstration Batch File

Demo Batch File Folder: Painter \demo_batch

The demo batch file includes the following files:

- Batch File: test.bat, test_bashrc
- FPGA Configure File: Painter.sof
- Nios II Program: Painter.elf

■ Demonstration Setup

- Make sure Quartus II and Nios II are installed on your PC
- Power on the Cyclone V SoC development board
- Connect USB-Blaster to the Cyclone V SoC development board and install USB-Blaster driver if necessary
- Execute the demo batch file "test.bat" under the batch file folder, Painter\demo_batch
- After Nios II program is downloaded and executed successfully, you will see a painter GUI in the LCD. Figure 4-2 shows the GUI of the Painter Demo.

- The GUI is classified into three areas: Palette, Canvas, and Gesture. Users can select pen color from the color palette and start painting in the Canvas area. If gesture is detected, the associated gesture symbol is shown in the gesture area. To clear canvas content, click the "Clear" button.
- Figure 4-3 shows the photo when users paint in the canvas area. Figure 4-4 shows the photo when zoom-in gesture is detected.

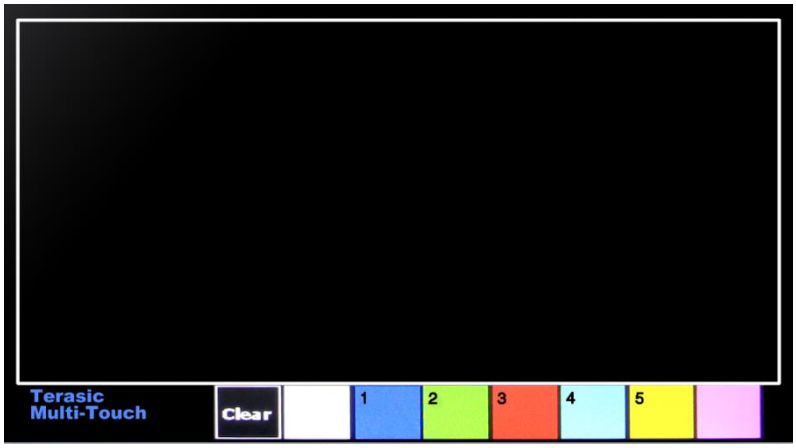

Figure 4-2 GUI of Painter Demo

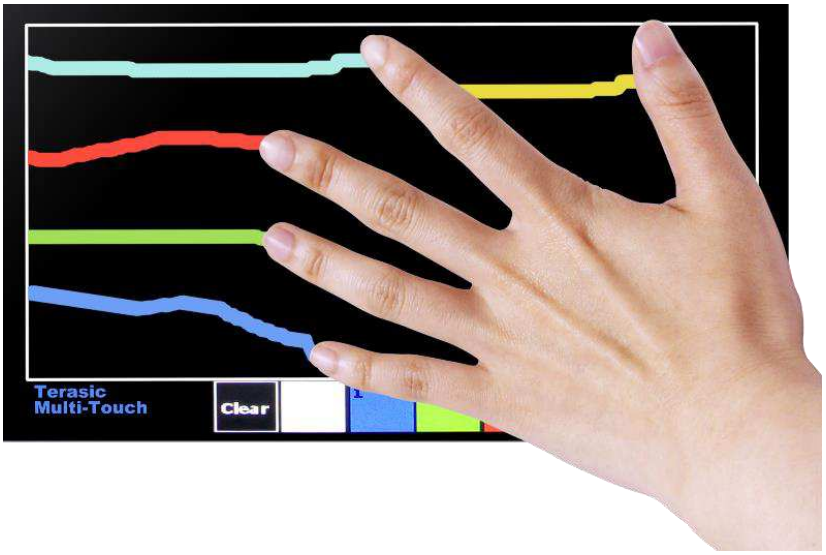

Figure 4-3 Five Point Touch Painting

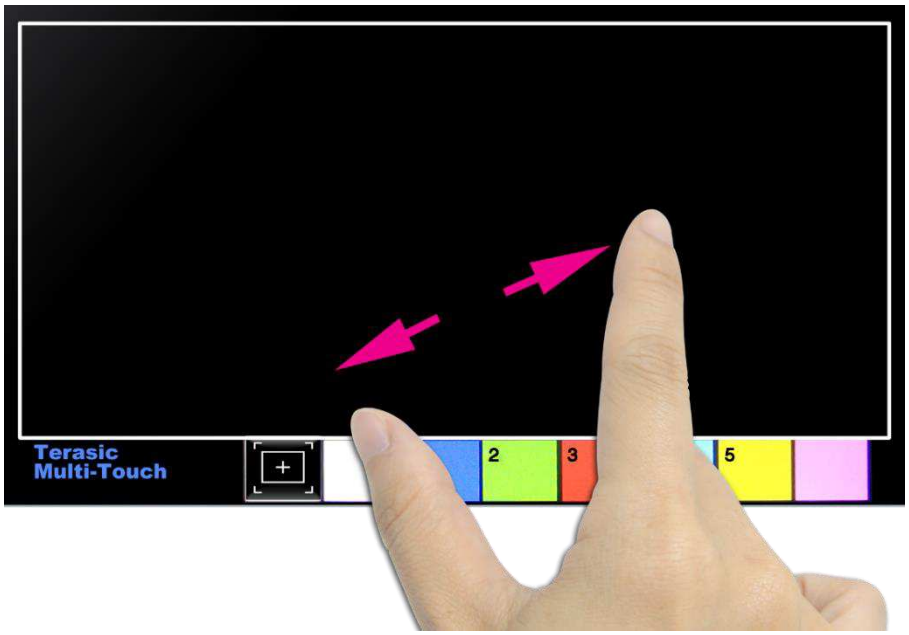

Figure 4-4 Zoom-In Gesture

Note: execute the test.bat under Paintger\demo_batch will automatically download the .sof and .elf file.

4.3 Camera Application

This demonstration shows a digital camera reference design using the 8-Megapixel CMOS sensor and LCD modules on the VEEK-MT2-C5SoC. The CMOS sensor module sends the raw image data to FPGA on the C5SoC board, the FPGA on the board handles image processing part and converts the data to RGB format to display on the LCD module. Figure 4-5 shows the block diagram of the demonstration.

After the configuration, The CMOS sensor starts to capture and output image data streams, the CCD_Capture block extracts the valid pixel data streams based on the synchronous signals from the CMOS sensor. The data streams are generated in Bayer Color Pattern format. So it's then converted to RGB data streams by the RAW2RGB block. After that, the DDR3_Qsys acquires and writes the RGB data streams to the DDR3 SDRAM which performs as a frame buffer. The writing clock is the same as CMOS sensor pixel clock, and the reading clock is provided by the LCD Controller, which is 33MHz. Then the LCD controller fetches the RGB data from the buffer and sent it to the Focus ADJ module to achieve the autofocus function. And finally displays the image streaming to the LCD panel.

All module functions are described below:

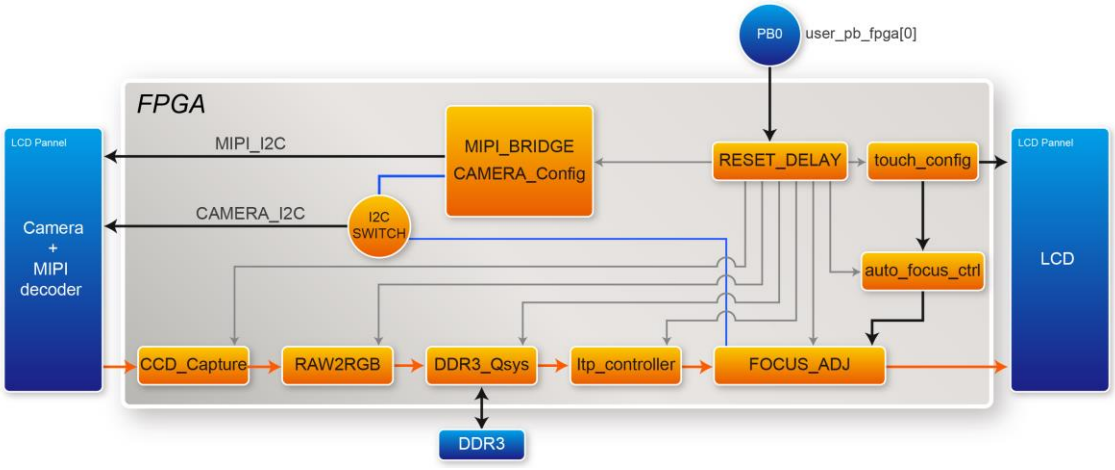

Figure 4-5 Block Diagram of the digital camera design

- MIPI_BRIDGE_CAMERA_Config: the MIPI BRIDGE I2C and Camera I2C setting controller, such as set to output 800X480@60Hz timing. It mainly writes I2C corresponding parameters to MIPI-BRIDGE IC register and Camera Sensor IC register respectively through their own I2C buses. MIPI_I2C bus is used to write MIPI BRIDGE I2C (I2C Slave Address = 0x1c.), CAMERA_I2C bus is used to write Camera Sensor (IC Slave Address = 0x6c).
- CCD_Capture: This module extracts the valid pix data streams based on the synchronous signals from the CMOS sensor.
- RAW2RGB: This module is to convert RAW data to RGB data.
- DDR3_Qsys: This module is a DDR3 Controller can control external DDR3 SDRAM Memory and read/write image data.
- ltp_Controller: the LCD signal timing generator, can generate signal timing which the resolution is 800x480.
- FOCUS_ADJ: This module provides two main focus functions.
- touch_config: This module controls the touch functions of the LCD panel.
- auto_focus_ctrl: This module trigger the autofocus according to the touch status.

■ The Default Camera Settings

In this demonstration, the default camera settings are:

- Resolution: 800x480
- Pixel Data: RAW10
- Frame Rate: 60 fps
- Bin Mode: 1

■ Demonstration Source Code

- Project directory: Camera
- Bit stream used: Camera.sof

■ Demonstration Batch File

Demo Batch File Folder: Camera\demo_batch

The demo batch file includes the following files:

- Batch File: test.bat
- FPGA Configure File: Camera.sof

■ Demonstration Setup

- Load the bit stream into FPGA by executing the batch file 'test.bat' under Camera\demo_batch\ folder
- The system enters the FREE RUN mode automatically. Press S6 on the Altera Cyclone® V SoC board to reset the circuit
- Camera capturing image displays on LCD, if the LCD image is fuzzy, please touch the LCD screen once that will perform the focus operation. Users can also use "ZOOM IN" gesture on the LCD screen (there will be a yellow box on image, see **Figure 4-7** , then, touching the LCD screen once, the middle area focus operation will be performed. Using "ZOOM OUI" gesture on the LCD screen will clear the yellow box.

Note: execute the test.bat under Camera\demo_batch will automatically download the .sof file.

錯誤! 找不到參照來源。 summarizes the functional keys of the digital camera. **Figure 4-6** gives a run-time photograph of the demonstration.

Table 4-1 The functional keys of the digital camera demonstration

Component	*Function Description*
S6	Reset circuit (user_pb_fpga[0])
ZOOM IN Gesture	Area Focus Mode
ZOOM Out Gesture	Whole Area Focus Mode

Figure 4-6 Screen shot of the camera demonstration

Figure 4-7 Area Focus Mode of the camera demonstration

4.4 Digital Accelerometer Demonstration

This demonstration shows a bubble level implementation based on a digital accelerometer. There are two I2C controllers used in this demonstration. One is used to communicate with MPU9250 to retrieve the gravity information, and another is used to communicate with the APDS-9300 Miniature Ambient Light Photo Sensor. The demonstration using the gravity information retrieved from the MPU9250 to implement a bubble level on the LCD panel. When tilting the VEEK-MT2-C5SoC, the NIOS II program reads the acceleration of gravity from the MPU9250.