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EVBUM2259/D

KAF-8300 Imager Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Description

The KAF-8300 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be part of a two−board set, used in conjunction with a Timing Generator Board. ON Semiconductor offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAF-8300 Image Sensor.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (P1). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KAF-8300 Imager Board has been designed to operate the KAF-8300 with the specified performance at nominal operating conditions. (See the KAF-8300 performance specifications for details).

For testing and characterization purposes, the KAF-8300 Imager Board provides the ability to adjust many of the CCD bias voltages and CCD clock level voltages by adjusting potentiometers on the board. The Imager Board provides the means to modify other device operating parameters (eg., CCD Reset clock pulse width, VSS bias voltage) by populating components differently on the board.

Certain features of the Imager Board circuitry are provided for ON Semiconductor use only, and are not supported for customer use. These circuits may not be populated on the Imager Board.

IMAGER BOARD INPUT REQUIREMENTS

Table 1. POWER REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5	5.1	V
		900		mA
−5 V_MTR Supply	−5.1	−5	−4.9	V
		100		mA
VPLUS Supply	18	20	21	V
		200		mA
VMINUS Supply	−21	−20	−18	V
		200		mA

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Comments
H1A (±)	0	±0.1	2.4	V	H1 clock
H1B (±)	0	±0.1	2.4	V	H1L clock
H2A (±)	0	±0.1	2.4	V	H2 clock
H2B (±)	0	±0.1	2.4	V	(not used)
AMP ENABLE (±)	0	±0.1	2.4	V	ALT VDD ckt.
R (±)	0	±0.1	2.4	V	Reset clock
V1 (±)	0	±0.1	2.4	V	V1 clock
V2 (±)	0	±0.1	2.4	V	V2 clock
H1A (±)	0	±0.1	2.4	V	H1 clock

ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the KAF−8300 Imager Board (refer to Figure 1).

Power Filtering and Regulation

Power is supplied to the Imager Board via the P1 interface connector. The power supplies are de-coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V and −15 V supplies from the VPLUS and VMINUS supplies.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the P1 interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

CCD Pixel−Rate Clock Drivers (H1, H1L, H2 & Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL−level input clock signals to the voltage levels required by the CCD. The H1 and H2 clock driver circuits have the option of installing an extra set of transistors to improve transient response; as they are unnecessary to achieve specified CCD performance, they are not populated. The high level and low level of the CCD clocks are set by potentiometers.

Reset Clock One−Shot

The pulse width of the RESET_CCD clock can be set by a programmable One−Shot. The One−Shot can be configured to provide a RESET_CCD clock signal with a pulse width from 5 ns to 15 ns, buffered by operational amplifiers.

CCD VCLK Drivers

The vertical clock (VCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL−level clock signals to the voltage levels required by the CCD. The high and low voltage rails of the vertical clocks are set by potentiometers.

CCD Bias Voltages

The bias voltages are set by potentiometers. The bias voltages are de−coupled at the CCD pin.

Emitter−Follower

The VOUT_CCD signal is buffered using a bipolar junction transistor in the emitter-follower configuration. This circuit also provides the necessary 5 mA current sink for the CCD output circuit.

Line Drivers

The buffered VOUT_CCD signal is AC−coupled and driven from the Imager Board by an operational amplifier in a non−inverting configuration. Because of the magnitude of the output voltage of the KAF−8300, the operational amplifier is configured to have a gain of 1.25, to avoid overloading the input to the AFE on the Timing Board.

CCD Image Sensor

This evaluation board supports the KAF−8300 Image Sensor.

OPERATIONAL SETTINGS

The Imager board is configured to operate the KAF−8300 CCDs under the following operating conditions:

Bias Voltages

The following voltages are fixed, or adjusted with a potentiometer as noted. The Min and Max values in Table 3 indicate the adjustment latitude of the potentiometer circuit. The Nominal values listed in Table 3 are for reference only; refer to the KAF−8300 device specification.

Table 3. BIAS VOLTAGES

Description	Symbol	Min	Nom	Max	Units	Potentiometer	Notes
Output Amplifier Supply	VDD		15.0		V	fixed	1
Reset Drain	RD	7.0	11.5	13.5	V	R16	
Output Amplifier Return	VSS	0.7	1.25	2.8	V	–	2
Substrate	SUB		0		V	fixed	3
Output Gate	OG	−5.0	−2.8	5.0	V	R12	
Lateral Drain − Top	LOD T	6.0	10.0	12.0	V	R7	

1. VDD may be switched to an alternate supply during integration; see Table 4.
2. VSS is set from 1 to 4 diode drops above AGND by populating R51, R50, and R67 accordingly. Each resistor populated bypasses a diode. Default is R67, R50 populated, VSS is two diode drops above AGND.
3. VSUB is connected directly to AGND.
4. LOD B is for internal testing only. During normal device operation, both LOD T and LOD B should be set to the same voltage. The LOD B circuit has been disabled on the Imager Board, and both voltages are controlled by R7.

Clock Voltages

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The Min and Max values in Table 4 indicate the adjustment latitude of the potentiometer circuit. The nominal values listed are for reference only; refer to the KAF−8300 device specification.

Table 4. CLOCK VOLTAGES

Description	Symbol	Level	Min	Nom	Max	Units	Potentiometer	Notes
Horizontal CCD Clock – Phase 1	H1_CCD	Low	−10.0	−4.5	−0.7	V	R114	5
		High	0.7	1.5	5.0	V	R121	6
HCCD Last Gate Clock – Phase 1	H1L_CCD	Low	−10.0	−6.5	−0.7	V	R87	5
		High	0.7	1.5	5.0	V	R98	6
Horizontal CCD Clock – Phase 2	H2_CCD	Low	−10.0	−5.0	−0.7	V	R136	
		High	0.7	1.0	5.0	V	R145	
Vertical CCD Clock – Phase 1	V1_CCD	Low	−10.0	−9.25	−0.7	V	R94	7
		High	0.7	2.25	7.5	V	R63	8
Vertical CCD Clock – Phase 2	V2_CCD	Low	−10.0	−9.25	−0.7	V	R94	7
		High	0.7	2.25	7.5	V	R63	8
Reset Clock	RESET_CCD	Low	−5.0	2.0	5.0	V	R58	
		High	0.0	8.0	10.0	V	R73	
VDD	ALT VDD	Low	7.0		14.0	V	R33	9
	+15 V	High		15.0		V	Fixed	

5. The H1 and H1L drivers' low−level voltage can be set to the same level. If it is desired to set the H1 and H1L low level to the same voltage, this can be accomplished by removing R71 and instead installing jumper E2.
6. The H1 and H1L drivers' high−level voltage can be set to the same level. If it is desired to set the H1 and H1L high level to the same voltage, this can be accomplished by removing R97 and instead installing jumper E3.
7. V1_CCD and V2_CCD low levels are controlled by the same potentiometer (R63).
8. V1_CCD and V2_CCD high levels are controlled by the same potentiometer (R94).
9. Controlled by AMP_ENABLE.

Reset Clock Pulse Width

The pulse width of the RESET_CCD is set by configuring P[2..0], the inputs to the programmable one−shot. P[2..0] can be tied high or low to achieve the desired pulse width by populating the resistors R37, R38, R51, and R52 accordingly.

Table 5. RESET CLOCK PULSE WIDTH

Pulse Width	P2	P1	P0	R52	R51	R37	R38	Notes
15 ns	0	0	0	OUT	IN	OUT	IN	
5 ns	0	0	1	IN	OUT	OUT	IN	Default Setting
7.5 ns	0	1	0	OUT	IN	IN	OUT	
10 ns	0	1	1	IN	OUT	IN	OUT	

BLOCK DIAGRAM AND PERFORMANCE DATA

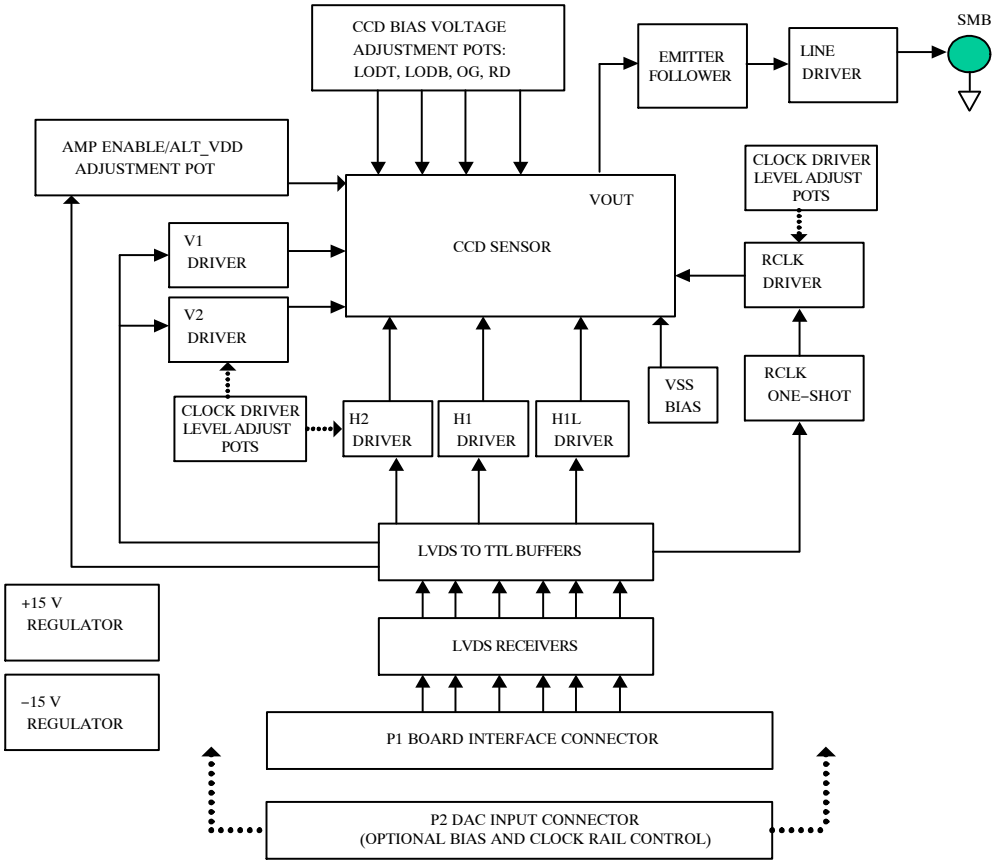

Figure 1. KAF−8300 Imager Board Block Diagram

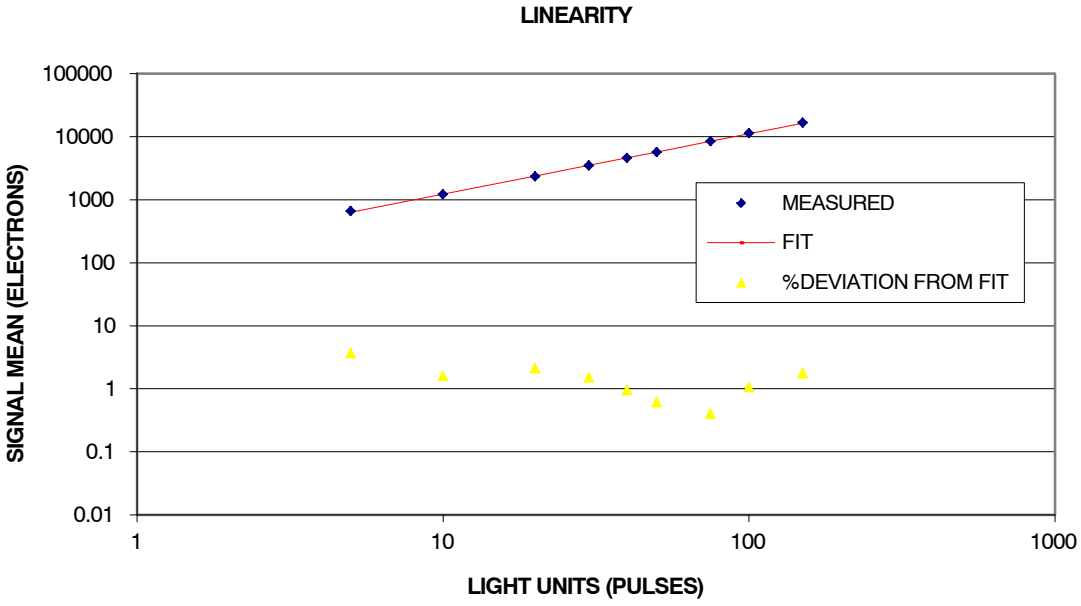

Figure 2. Measured Performance − Linearity

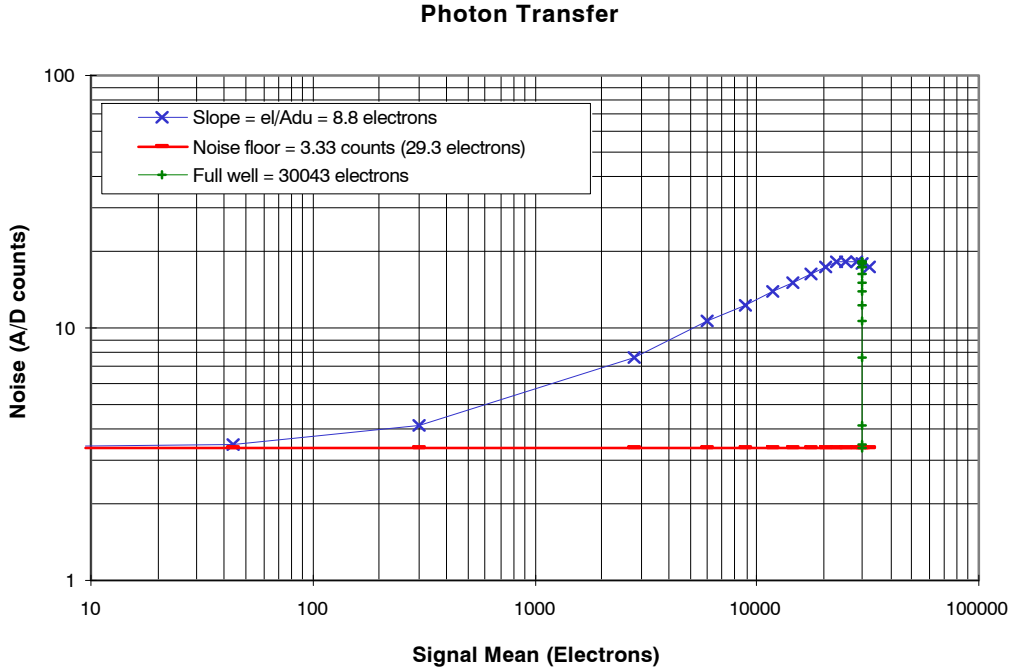

Figure 3. Measured Performance – Dynamic Range and Noise Floor

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J1

The emitter-follower buffered CCD_VOUT signal is driven from the Imager Board via the SMB connector J1. Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Table 6. P1 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	N.C.	6	N.C.
7	AGND	8	AGND
9	AMP_ENABLE+	10	AMP_ENABLE−
11	AGND	12	AGND
13	N.C.	14	N.C.
15	AGND	16	AGND
17	N.C.	18	N.C.
19	AGND	20	AGND
21	V2+	22	V2−
23	AGND	24	AGND
25	V1+	26	V1−
27	AGND	28	AGND
29	R+	30	R−
31	AGND	32	AGND
33	H2B+	34	H2B−
35	AGND	36	AGND
37	H2A+	38	H2A−
39	AGND	40	AGND
41	H1B+	42	H1B−
43	AGND	44	AGND
45	H1A+	46	H1A−
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	N.C.	60	N.C.
61	−5 V_MTR	62	−5 V_MTR
63	N.C.	64	N.C.
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the ON Semiconductor Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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