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KAI-1010

1008 (H) x 1018 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAI–1010 Image Sensor is a high-resolution monochrome charge coupled device (CCD) device whose non-interlaced architecture makes it ideally suited for video, electronic still and motion/still camera applications. The device is built using an advanced true two-phase, double-polysilicon, NMOS CCD technology. The p+npn− photodetector elements eliminate image lag and reduce image smear while providing antiblooming protection and electronic-exposure control. The total chip size is 10.15 (H) mm × 10.00 (V) mm

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD, Non-Interlaced
Total Number of Pixels	1024 (H) × 1024 (V)
Number of Effective Pixels	1008 (H) × 1018 (V)
Number of Active Pixels	1008 (H) × 1018 (V)
Number of Outputs	1 or 2
Pixel Size	9 μm (H) × 9 μm (V)
Active Image Size	9.1 mm (H) × 9.2 mm (V) 12.9 mm (Diagonal) 1″ Optical Format
Optical Fill-Factor	60%
Saturation Signal	> 50,000 e^-
Output Sensitivity	12 μV/e^-
Dark Noise	50 e^- rms
Dark Current	< 0.5 nA/cm^2
Quantum Efficiency (Wavelength = 500 nm)	37%
Blooming Suppression	> 100 X
Maximum Data Rate	20 MHz/Channel (2 Channels)
Image Lag	Negligible
Package	CERDIP
Cover Glass	AR Coated (Both Sides)

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

Figure 1. KAI–1010 Interline CCD Image Sensor

Features

- Front Illuminated Interline Architecture
- Progressive Scan (Non-Interlaced)
- Electronic Shutter
- On-Chip Dark Reference
- Low Dark Current
- High Sensitivity Output Structure
- Anti-Blooming Protection
- Negligible Lag
- Low Smear (0.1% with Microlens)

Application

- Machine Vision

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−1010 Image Sensor

Part Number	Description	Marking Code
KAI−1010−ABA−CD−AE	Monochrome, Telemetric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	KAI−1010M Serial Number
KAI−1010−ABA−CD−BA	Monochrome, Telemetric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Standard Grade	
KAI−1010−ABA−CR−AE	Monochrome, Telemetric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Sample	
KAI−1010−ABA−CR−BA	Monochrome, Telemetric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (2 Sides), Standard Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

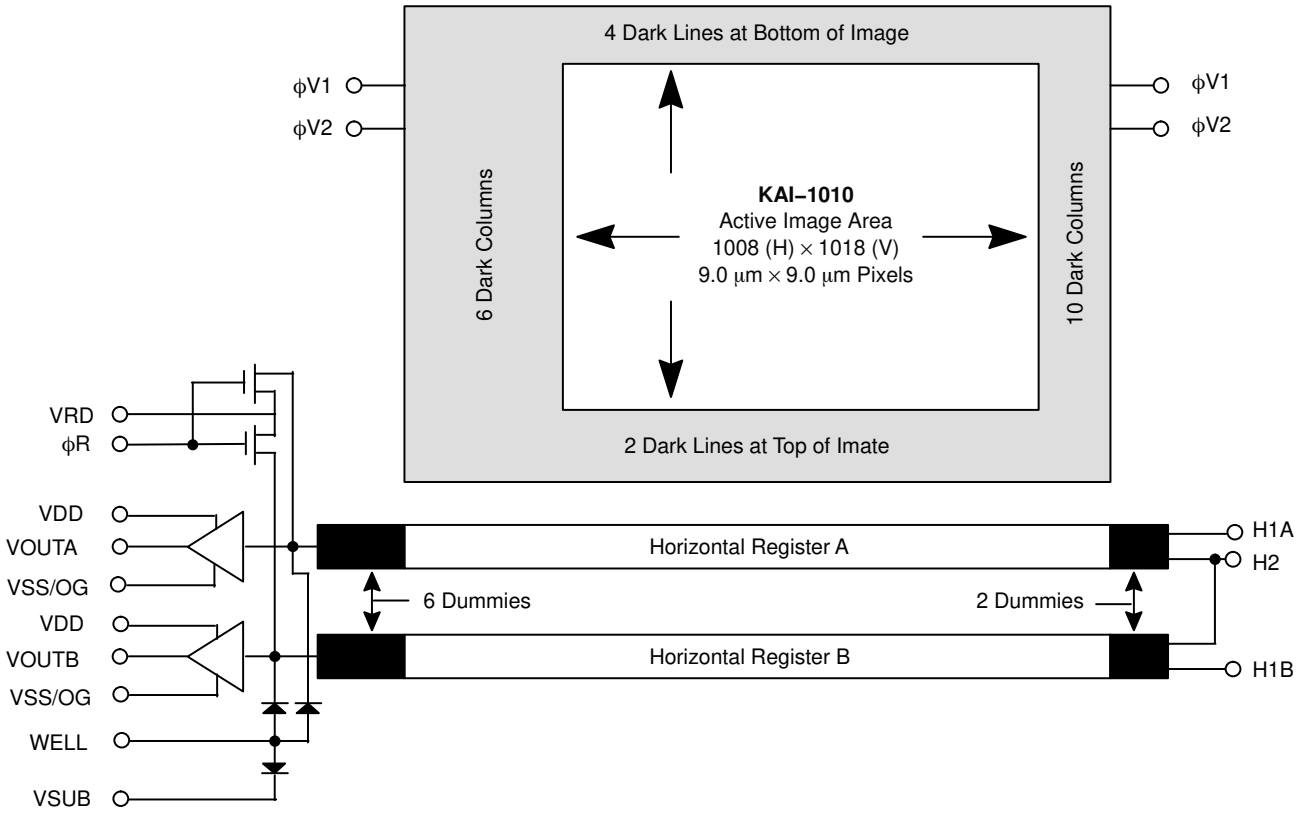


Figure 2. Functional Block Diagram

The KAI−1010 consists of 1024 × 1024 photodiodes, 1024 vertical (parallel) CCD shift registers (VCCDs), and dual 1032 pixel horizontal (serial) CCD shift registers (HCCDs) with independent output structures. The device can be operated in either single or dual line mode. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The active pixels are arranged in a 1008 (H) × 1018 (V) array with an additional 16 columns and 6 rows of light-shielded dark reference pixels.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Charge Transport

The accumulated or integrated charge from each photodiode is transported to the output by a three step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock (ϕV1). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock, ϕH2, these charge packets are dumped over the output gate (OG, Figure 4) onto the floating diffusion (FDA and FDB, Figure 4).

Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the HCCDs begins when ϕV2 is clocked high and then low (while holding ϕH1A high) causing charge to be transferred from ϕV1 to ϕV2 and subsequently into the A HCCD. The A register can now be read out in single line mode. If it is desired to operate the device in a dual line readout mode for higher frame rates, this

line is transferred into the B HCCD by clocking ϕH1A to a low state, and ϕH1B to a high state while holding ϕH2 low. After ϕH1A is returned to a high state, the next line can be transferred into the A HCCD. After this clocking sequence, both HCCDs are read out in parallel.

The charge capacity of the horizontal CCDs is slightly more than twice that of the vertical CCDs. This feature allows the user to perform two-to-one line aggregation in the charge domain during V-to-H transfer. This device is also equipped with a fast dump feature that allows the user to selectively dump complete lines (or rows) of pixels at a time. This dump, or line clear, is also accomplished during the V-to-H transfer time by clocking the fast dump gate.

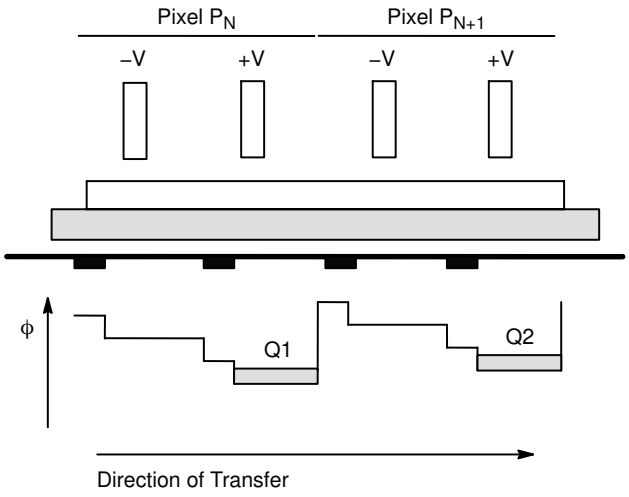


Figure 3. True 2 Phase CCD Cross Section

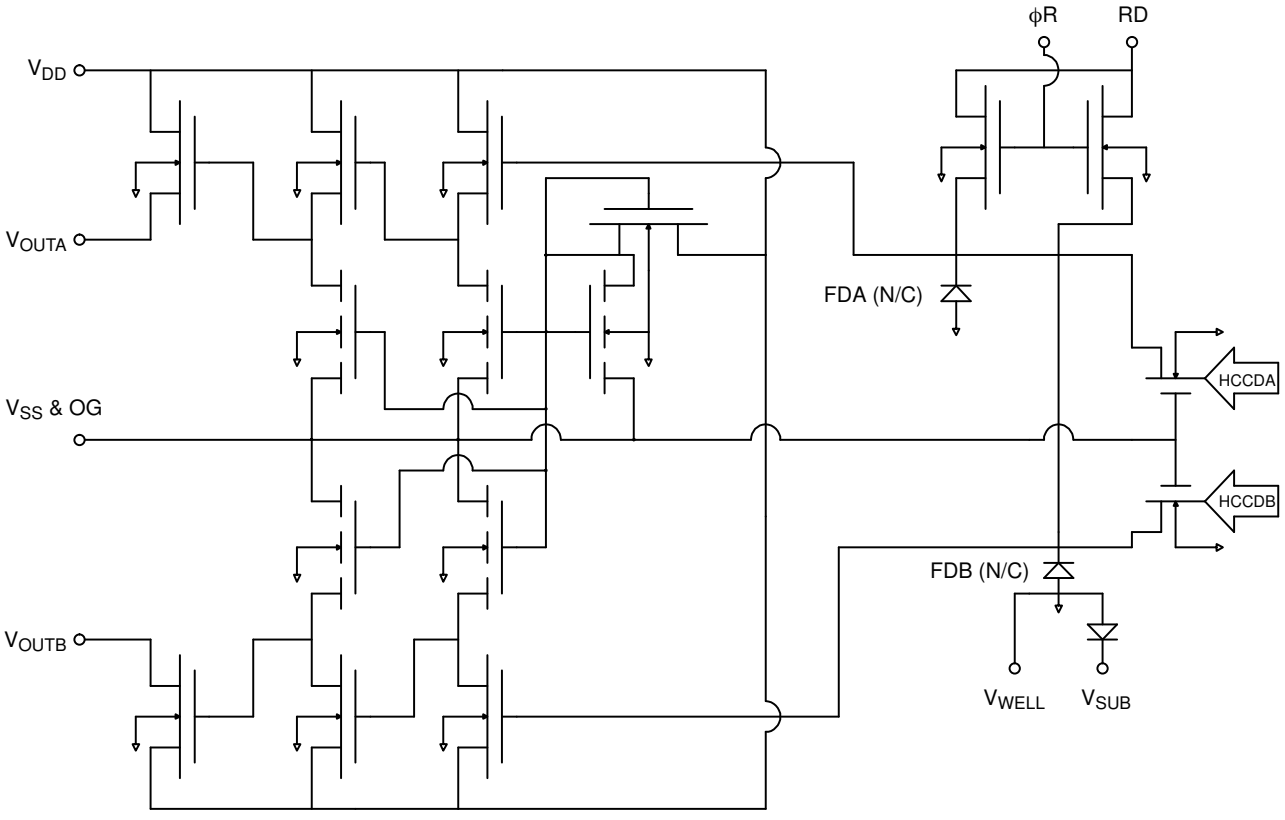


Figure 4. Output Structure

Output Structure

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression $\Delta V_{FD} = \Delta Q / C_{FD}$. A three stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of μV/e⁻. After the signal has been sampled off-chip, the reset clock (ϕR) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage (VRD).

Electronic Shutter

The KAI−1010 provides a structure for the prevention of blooming which may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD). This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse (VES ≈ 40 V) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on ϕV1. The integration time is then the time between the falling edges of the substrate shutter pulse and ϕV1. This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feedϕthrough. The shutter pulse VES must be “hidden” in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Physical Description

Pin Description and Device Orientation

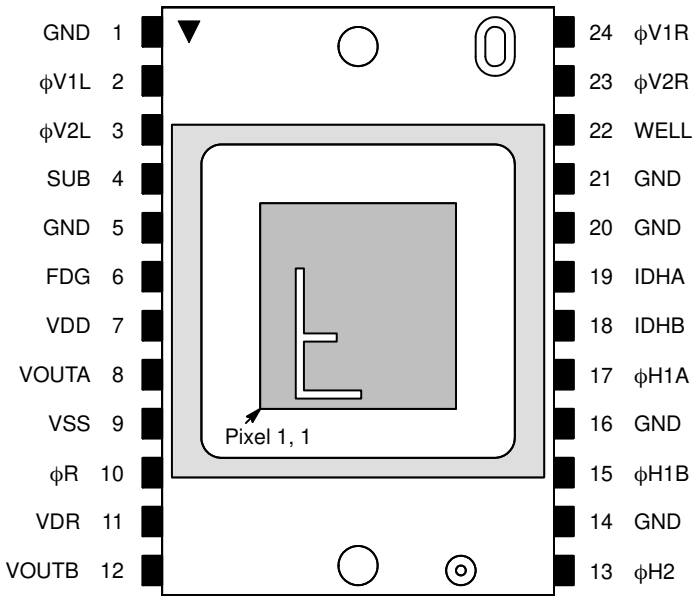


Figure 5. Pinout Diagram

Table 3. PIN DESCRIPTION

Pin	Name	Description
1	GND	Ground
2	ϕV1L	Vertical CCD Clock – Phase 1
3	ϕV2L	Vertical CCD Clock – Phase 2
4	SUB	Substrate
5	GND	Ground
6	FDG	Fast Dump Gate
7	VDD	Output Amplifier Supply
8	VOUTA	Video Output Channel A
9	VSS	Output Amplifier Return & OG
10	ϕR	Reset Clock
11	VDR	Reset Drain
12	VOUTB	Video Output Channel B

Pin	Name	Description
13	ϕH2	A & B Horizontal CCD Clock – Phase 2
14	GND	Ground
15	ϕH1B	B Horizontal CCD Clock – Phase 1
16	GND	Ground
17	ϕH1A	A Horizontal CCD Clock – Phase 1
18	IDHB	Input Diode B Horizontal CCD
19	IDHA	Input Diode B Horizontal CCD
20	GND	Ground
21	GND	Ground
22	WELL	P-Well
23	ϕV2R	Vertical CCD Clock – Phase 2
24	ϕV1R	Vertical CCD Clock – Phase 1

1. All GND pins should be connected to WELL (P-Well).
2. Pins 2 and 24 must be connected together – only 1 Phase 1 clock driver is required.
3. Pins 3 and 23 must be connected together – only 1 Phase 2 clock driver is required.

IMAGING PERFORMANCE

All the following values were derived using nominal operating conditions using the recommended timing. Unless otherwise stated, readout time = 140 ms, integration time = 140 ms and sensor temperature = 40°C. Correlated double sampling of the output is assumed and recommended. Many units are expressed in electrons, to convert to voltage, multiply by the amplifier sensitivity.

Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

Table 4. ELECTRO-OPTICAL IMAGE SPECIFICATIONS KAI−1010−ABA

Parameter	Symbol	Min.	Nom.	Max.	Unit	Notes
Optical Fill Factor	FF	–	55.0	–	%	
Saturation Exposure	E_{SAT}	–	0.037	–	$\mu J/cm^2$	1
Peak Quantum Efficiency	QE	–	37	–	%	2
Photoresponse Non-Uniformity	PRNU	–	10.0	–	% pp	3, 4
Photoresponse Non-Linearity	PRNL	–	5.0	–	%	

1. For λ = 550 nm wavelength, and V_{SAT} = 350 mV.
2. Refer to typical values from Figure 6.
3. Under uniform illumination with output signal equal to 280 mV.
4. Units: % Peak to Peak. A 200 by 200 sub ROI is used.

Monochrome with Microlens Quantum Efficiency

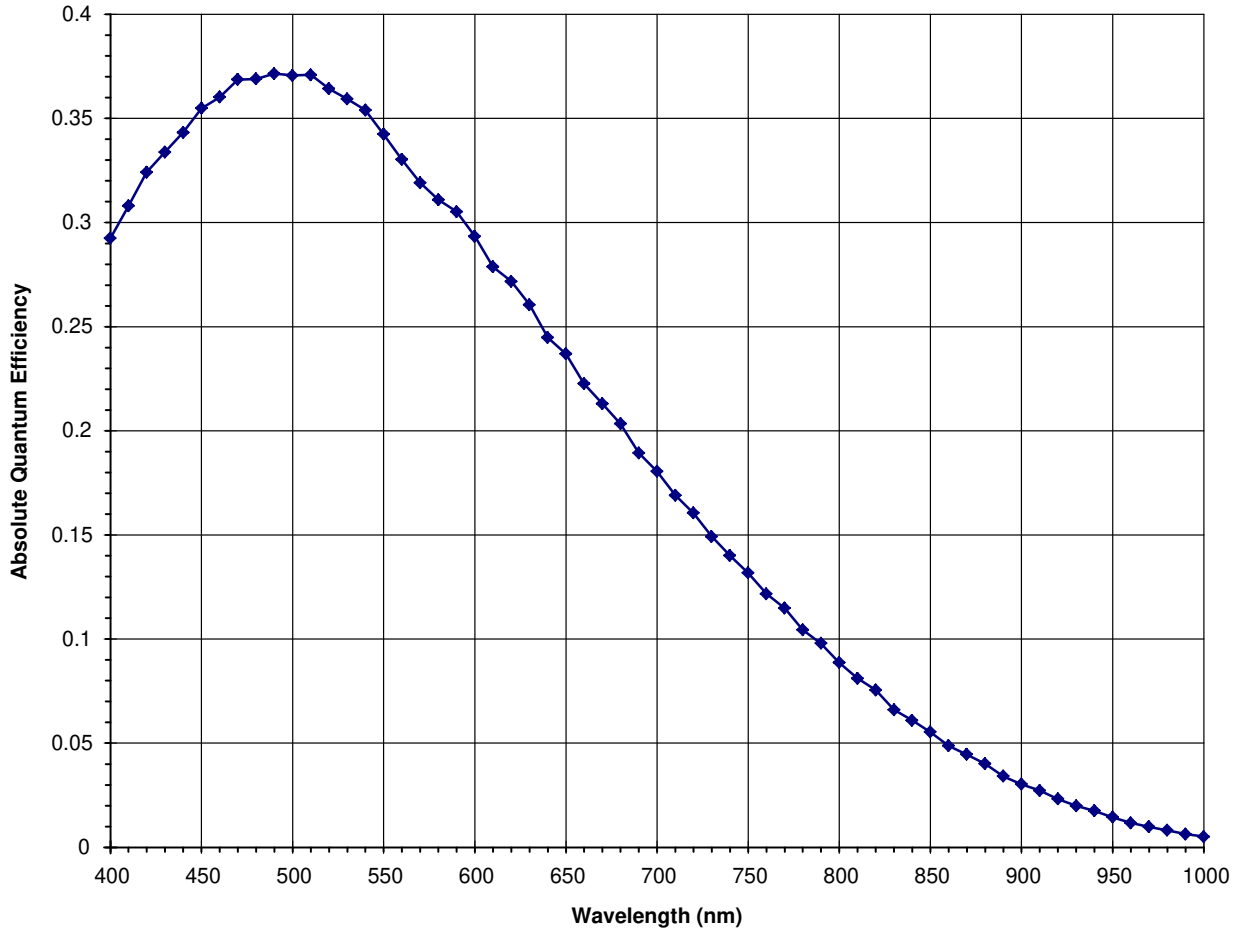
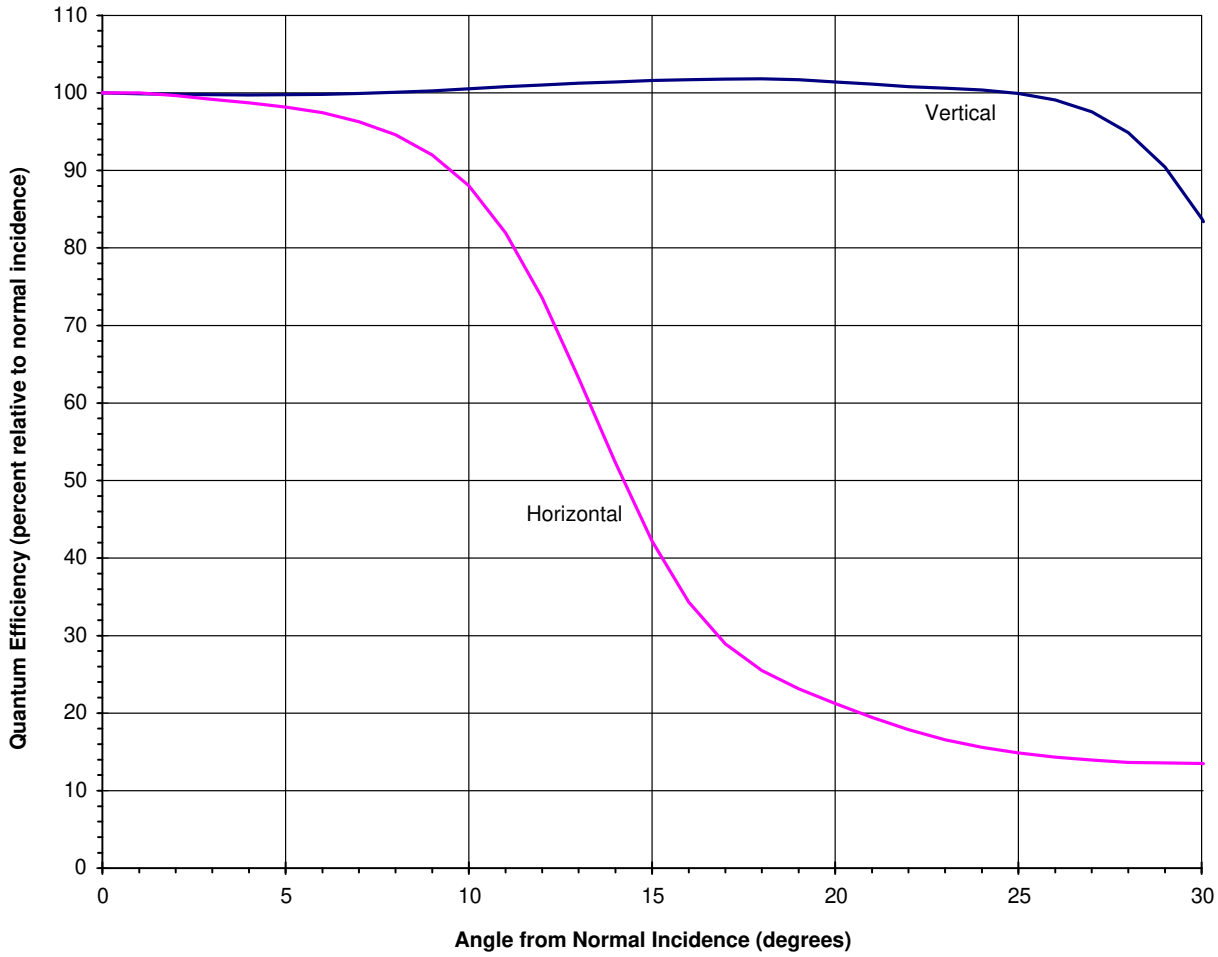


Figure 6. Nominal KAI−1010−ABA Spectral Response

Angular Quantum Efficiency



Notes:
1. For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
2. For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Figure 7. Angular Dependance of Quantum Efficiency

Frame Rates

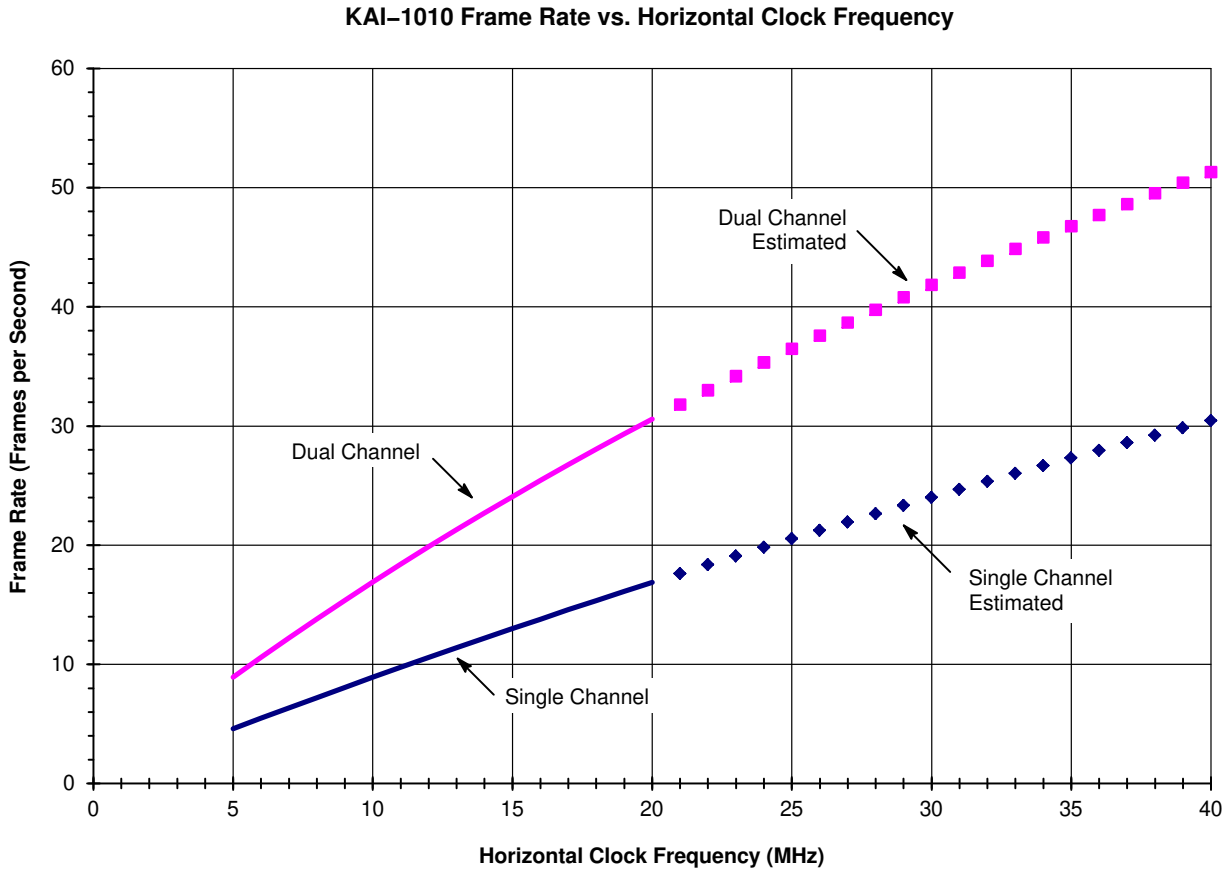


Figure 8. Frame Rate vs. Horizontal Clock Frequency

CCD Image Specifications

Table 5. CCD IMAGE SPECIFICATIONS

Parameter	Symbol	Min.	Nom.	Max.	Unit	Notes
Output Saturation Voltage	V_{SAT}	–	350	–	mV	1, 2, 8
Dark Current	I_D	–	–	0.5	nA	
Dark Current Doubling Temp	DCDT	7	8	10	°C	
Charge Transfer Efficiency	CTE	–	0.99999	–		2, 3
Horizontal CCD Frequency	f_H	–	–	40	MHz	4
Image Lag	I_L	–	–	100	e^-	5
Blooming Margin	X_{AB}	–	–	100		6, 8
Vertical Smear	Smr	–	0.01	–	%	7

1. V_{SAT} is the green pixel mean value at saturation as measured at the output of the device with X_{AB} = 1. V_{SAT} can be varied by adjusting V_{SUB}.
2. Measured at sensor output.
3. With stray output load capacitance of C_L = 10 pF between the output and AC ground.
4. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
5. This is the first field decay lag measured by strobe illuminating the device at (H_{SAT}, V_{SAT}), and by then measuring the subsequent frame's average pixel output in the dark.
6. X_{AB} represents the increase above the saturation-irradiance level (H_{SAT}) that the device can be exposed to before blooming of the vertical shift register will occur. It should also be noted that V_{OUT} rises above V_{SAT} for irradiance levels above H_{SAT}, as shown in Figure 9.
7. Measured under 10% (~ 100 lines) image height illumination with white light source and without electronic shutter operation and below V_{SAT}.
8. It should be noted that there is tradeoff between X_{AB} and V_{SAT}.

Output Amplifier @ V_{DD} = 15 V, V_{SS} = 0.0 V

Table 6. OUTPUT AMPLIFIER IMAGE SPECIFICATIONS

Parameter	Symbol	Min.	Nom.	Max.	Unit	Notes
Output DC Offset	V_{ODC}	–	7	–	V	1, 2
Power Dissipation	P_D	–	225	–	mW	3
Output Amplifier Bandwidth	f_{-3dB}	–	140	–	MHz	1, 4
Off-Chip Load	C_L	–	–	10	pF	

1. Measured at sensor output with constant current load of I_{OUT} = 5 mA per output.
2. Measured with VRD = 9 V during the floating-diffusion reset interval, (ϕR high), at the sensor output terminals.
3. Both channels.
4. With stray output load capacitance of C_L = 10 pF between the output and AC ground.

General

Table 7. GENERAL IMAGE SPECIFICATIONS

Parameter	Symbol	Min.	Nom.	Max.	Unit	Notes
Total Sensor Noise	$V_{N-TOTAL}$	–	0.5	–	mV rms	1
Dynamic Range	DR	–	7	60	dB	2

1. Includes amplifier noise and dark current shot noise at data rates of 10 MHz. The number is based on the full bandwidth of the amplifier. It can be reduced when a low pass filter is used.
2. Uses 20LOG (V_{SAT} / $V_{N-TOTAL}$) where V_{SAT} refers to the output saturation signal.

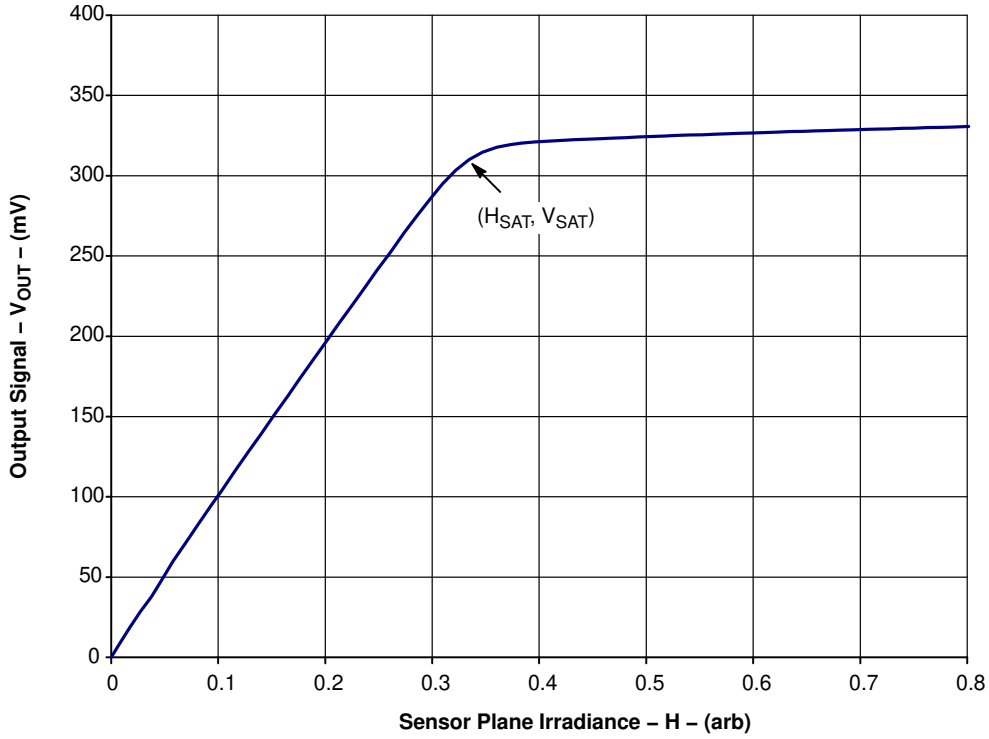
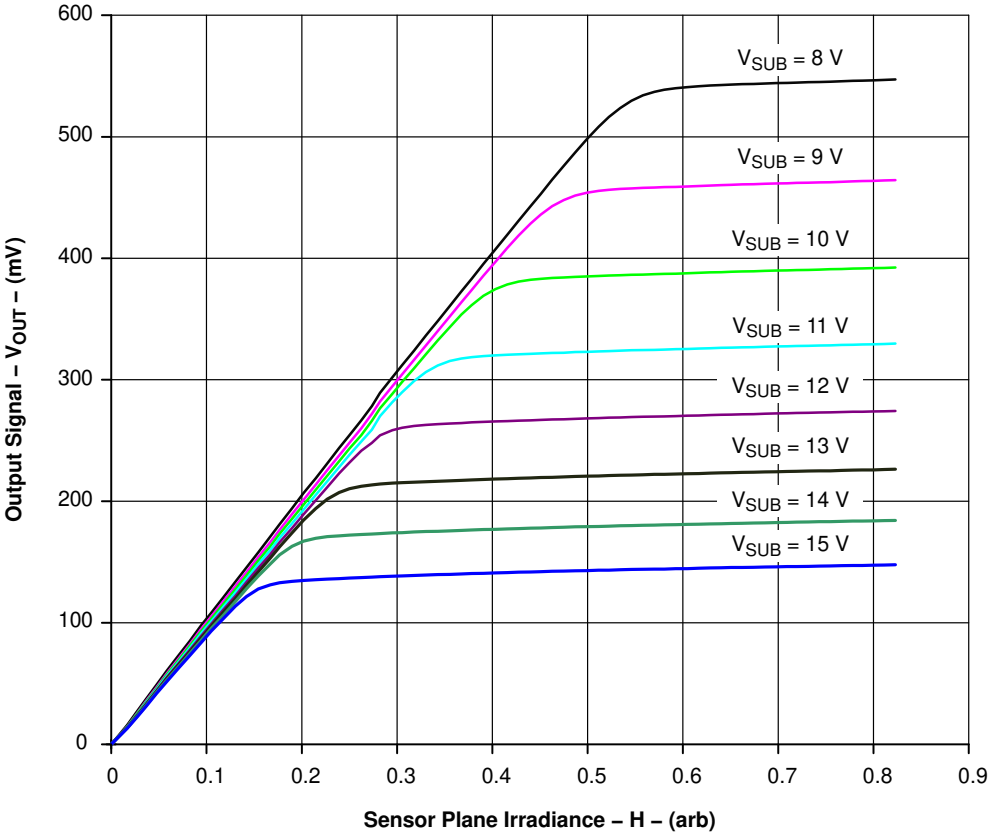


Figure 9. Typical KAI−1010−ABA Photoresponse



Notes:
1. As V_{SUB} is decreased, V_{SAT} increases and anti-blooming protection decreases.
2. As V_{SUB} is increased, V_{SAT} decreases and anti-blooming protection increases.

Figure 10. Example of V_{SAT} vs. V_{SUB}

DEFECT DEFINITIONS

All values are derived under normal operating conditions at 40°C operating temperature.

Table 8. DEFECT DEFINITIONS

Defect Type	Defect Definition	Number Allowed	Notes
Defective Pixel	Under uniform illumination with mean pixel output at 80% of V_{SAT}, a defective pixel deviates by more than 15% from the mean value of all pixels in its section.	12	1
Bright Defect	Under dark field conditions, a bright defect deviates more than 15 mV from the mean value of all pixels in its section.	5	1
Cluster Defect	Two or more vertically or horizontally adjacent defective pixels.	0	

1. Sections are 252 (H) × 255 (V) pixel groups, which divide the imager into sixteen equal areas as shown below.

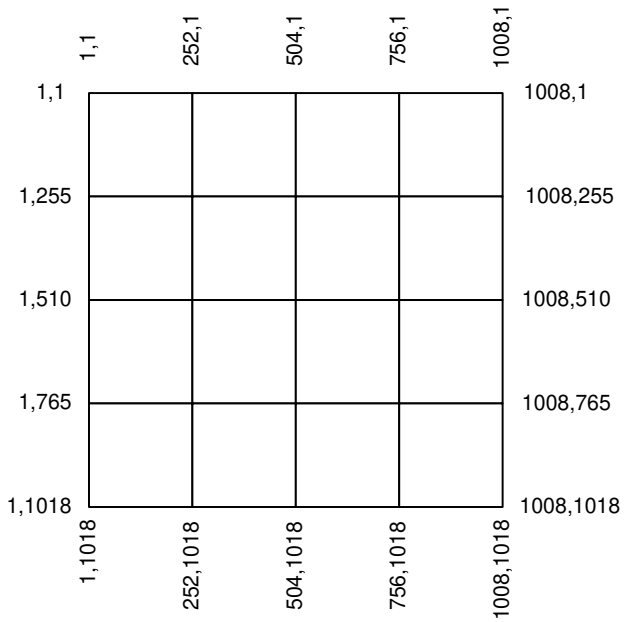


Figure 11.

Table 9.

Test Conditions	Value
Junction Temperature	(T_J) = 40°C
Integration Time	(t_{INT}) = 70 ms
Readout Rate	($t_{READOUT}$) = 70 ms

OPERATION

Table 10. ABSOLUTE MAXIMUM RATINGS

Rating	Description	Min.	Max.	Unit	Notes
Temperature (@ 10% ±5%RH)	Operation Without Damage	−50	+70	°C	5, 6
Voltage (Between Pins)	SUB−WELL	0	+40	V	1, 7
	VRD, VDD, OG & VSS − WELL	0	+15	V	2
	IDHA,B & VOUTA,B − WELL	0	+15	V	2
	ϕV1 − ϕV2	−12	+20	V	2
	ϕH1A, ϕH1B − ϕH2	−12	+15	V	2
	ϕH1A, ϕH1B, ϕH2, FDG − ϕV2	−12	+15	V	2
	ϕH2 − OG & VSS	−12	+15	V	2
	ϕR − SUB	−20	0	V	1, 2, 4
	All Clocks − WELL	−12	+15	V	2
Current	Output Bias Current (I_{OUT})	−	10	mA	3

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Under normal operating conditions the substrate voltage should be above +7 V, but may be pulsed to 40 V for electronic shuttering.
2. Care must be taken in handling so as not to create static discharge which may permanently damage the device.
3. Per Output. I_{OUT} affects the band-width of the outputs.
4. ϕR should never be more positive than V_{SUB}.
5. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
6. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
7. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Table 11. DC OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Unit	**Pin Impedance** (Note 6)	Notes
Reset Drain	V_{RD}	8.5	9	9.5	V	5 pF, > 1.2 MΩ	
Reset Drain Current	I_{RD}	−	0.2	−	mA		
Output Amplifier Return & OG	V_{SS}	−	0	−	V	30 pF, > 1.2 MΩ	
Output Amplifier Return Current	I_{SS}	−	5	−	mA		
Output Amplifier Supply	V_{DD}	12	15.0	15.0	V	30 pF, > 1.2 MΩ	
Output Bias Current	I_{OUT}	−	5	10	mA		5
P-Well	WELL	−	0.0	−	V	Common	1
Ground	GND	−	0.0	−	V		1
Fast Dump Gate	FDG	−7.0	−6.0	−5.5	V	20 pF, > 1.2 MΩ	2
Substrate	SUB	7	V_{SUB}	15	V	1 nF, > 1.2 MΩ	3, 8
Input Diode A, B Horizontal CCD	IDHA, IDHB	12.0	15.0	15.0	V	5 pF, > 1.2 MΩ	4

1. The WELL and GND pins should be connected to P-Well ground.
2. The voltage level specified will disable the fast dump feature.
3. This pin may be pulsed to V_{ES} = 40 V for electronic shuttering
4. Electrical injection test pins. Connect to VDD power supply.
5. Per output. Note also that I_{OUT} affects the bandwidth of the outputs.
6. Pins shown with impedances greater than 1.2 MΩ are expected resistances. These pins are only verified to 1.2 MΩ.
7. The operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

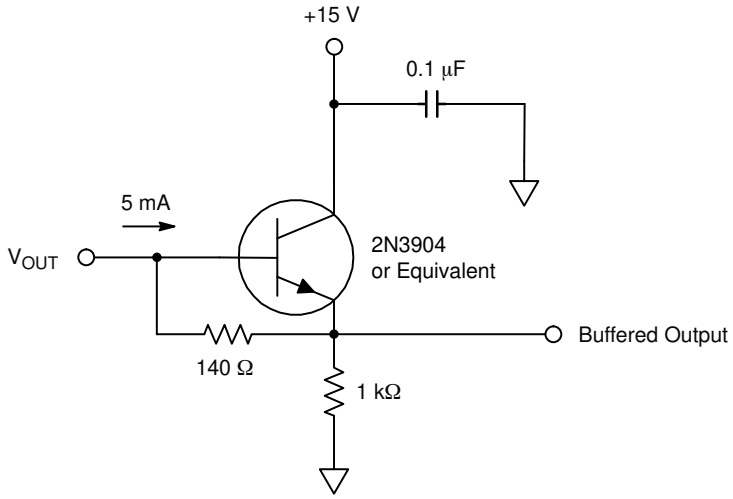


Figure 12. Recommended Output Structure Load Diagram

Table 12. AC CLOCK LEVEL CONDITIONS

Description	Symbol	Level	Min.	Nom.	Max.	Unit	Pin Impedance (Note 2)
Vertical CCD Clock	ϕV1	Low	−10.0	−9.5	−9.0	V	25 nF, > 1.2 MΩ
		Mid	0.0	0.2	0.4		
		High	8.5	9.0	9.5		
Vertical CCD Clock	ϕV2	Low	−10.0	−9.5	−9.0	V	25 nF, > 1.2 MΩ
		High	0.0	0.2	0.4		
ϕ1 Horizontal CCD A Clock	ϕH1A	Low	−7.5	−7.0	−6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5		
ϕ1 Horizontal CCD B Clock (Single Register Mode) (Note 4)	ϕH1B	Low	−7.5	−7.0	−6.5	V	100 pF, > 1.2 MΩ
ϕ1 Horizontal CCD B Clock (Dual Register Mode) (Note 4)	ϕH1B	Low	−7.5	−7.0	−6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5		
ϕ2 Horizontal CCD Clock	ϕH2	Low	−7.5	−7.0	−6.5	V	125 pF, > 1.2 MΩ
		High	2.5	3.0	3.5		
Reset Clock	ϕR	Low	−6.5	−6.0	−5.5	V	5 pF, > 1.2 MΩ
		High	−0.5	0.0	0.5		
Fast Dump Gate Clock (Note 3)	ϕFDG	Low	−7.0	−6.0	−5.5	V	20 pF, > 1.2 MΩ
		High	4.5	5.0	5.5		

1. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
2. Pins shown with impedances greater than 1.2 MΩ are expected resistances. These pins are only verified to 1.2 MΩ.
3. When not used, refer to DC operating condition.
4. For single register mode, set ϕH1B to −7.0 V at all times rather than clocking it.
5. This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult ON Semiconductor in those situations in which operating conditions meet or exceed minimum or maximum levels.

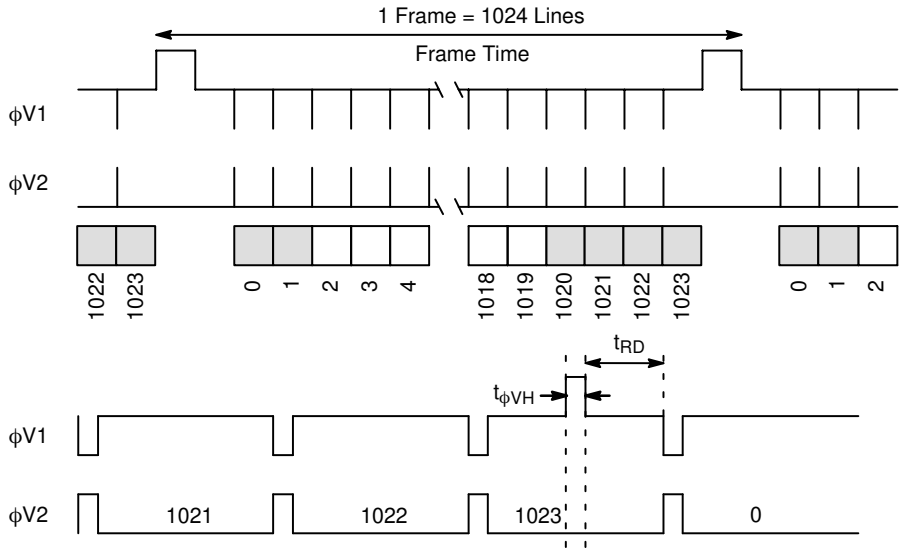
Table 13. AC TIMING REQUIREMENTS FOR 20 MHZ OPERATION

Description	Symbol	Min.	Nom.	Max.	Unit	Figure
Reset Pulse Width	$t_{\phi R}$	–	10	–	ns	Figure 12
Electronic Shutter Pulse Width	t_{ES}	10	25	–	μs	Figure 13
Integration Time (Note 1)	t_{INT}	0.1		–	ms	Figure 13
Photodiode to VCCD Transfer Pulse Width (Note 2)	$t_{\phi VH}$	4	5	–	μs	Figure 9
Clamp Delay	t_{CD}	–	15	–	ns	Figure 12
Clamp Pulse Width	t_{CP}	–	15	–	ns	Figure 12
Sample Delay	t_{SD}	–	35	–	ns	Figure 12
Sample Pulse Width	t_{SP}	–	15	–	ns	Figure 12
Vertical Readout Delay	t_{RD}	10	–	–	μs	Figure 9
ϕV1, ϕV2 Pulse Width	$t_{\phi V}$	3	–	–	μs	Figure 10
Clock Frequency ϕH1A, ϕH1B, ϕH2	$t_{\phi H}$	–	20	–	MHz	Figure 12
Line A to Line B Transfer Pulse Width	$t_{\phi AB}$	–	3	–	μs	Figure 15
Horizontal Delay	$t_{\phi HD}$	3	–	–	μs	Figure 10
Vertical Delay	$t_{\phi VD}$	25	–	–	ns	Figure 10
Horizontal Delay with Electronic Shutter	$t_{\phi HVES}$	1	–	–	μs	Figure 13

1. Integration time varies with shutter speed. It is to be noted that smear increases when integration time decreases below readout time (frame time). Photodiode dark current increases when integration time increases, while CCD dark current increases with readout time (frame time).
2. Anti-blooming function is off during photodiode to VCCD transfer.

TIMING

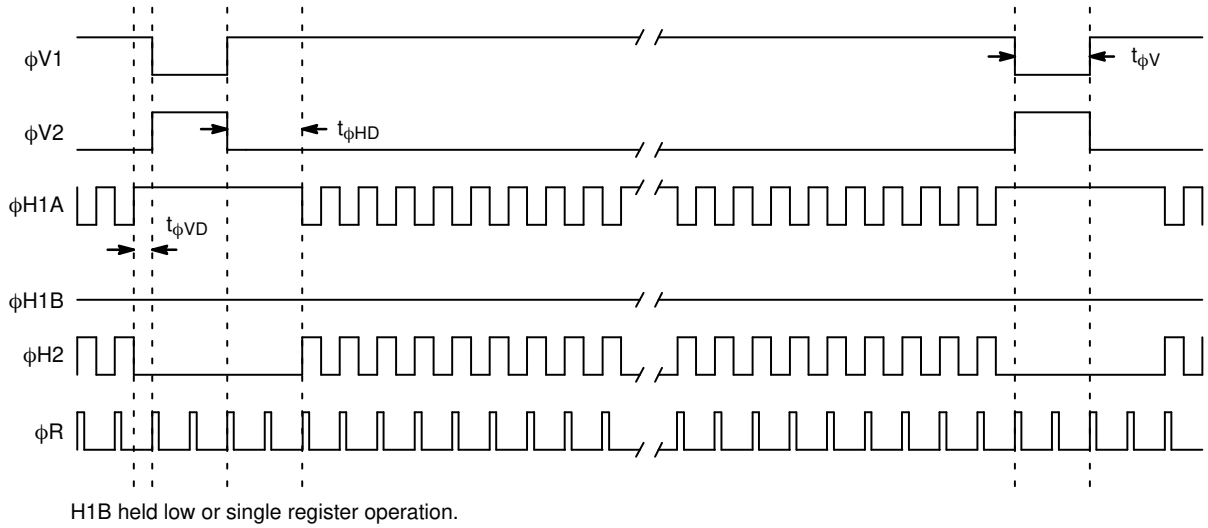
Frame Timing − Single Register Readout



NOTE: When no electronic shutter is used, the integration time is equal to the frame time.

Figure 13. Frame Timing − Single Resistor Readout

Line Timing − Single Register Readout



H1B held low or single register operation.

Line Content

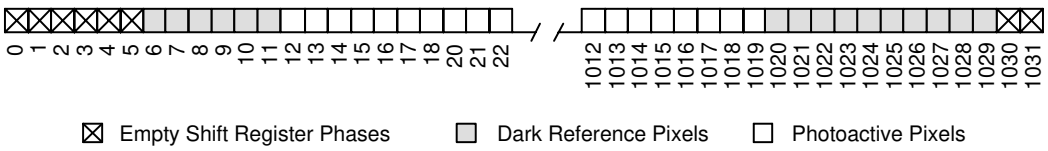


Figure 14. Frame Timing − Single Resistor Readout

Pixel Timing − Single Register Readout

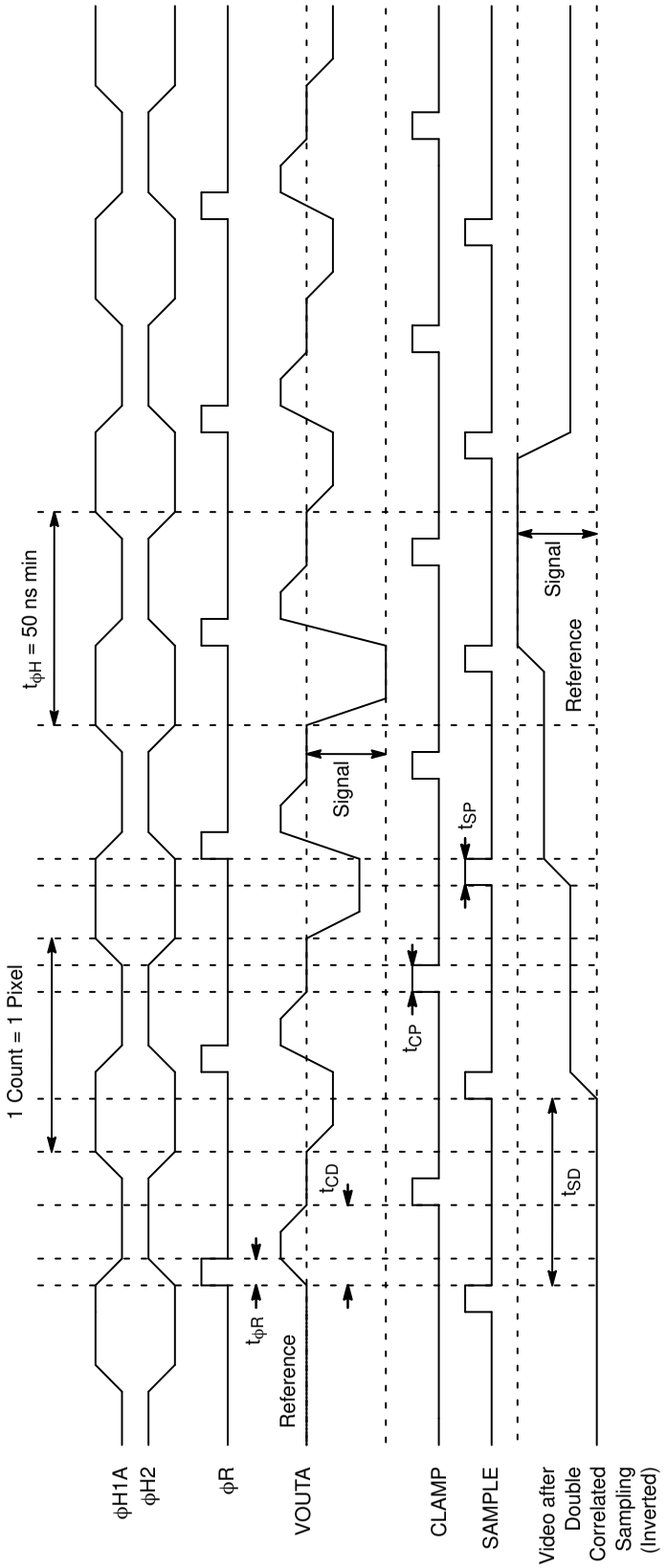
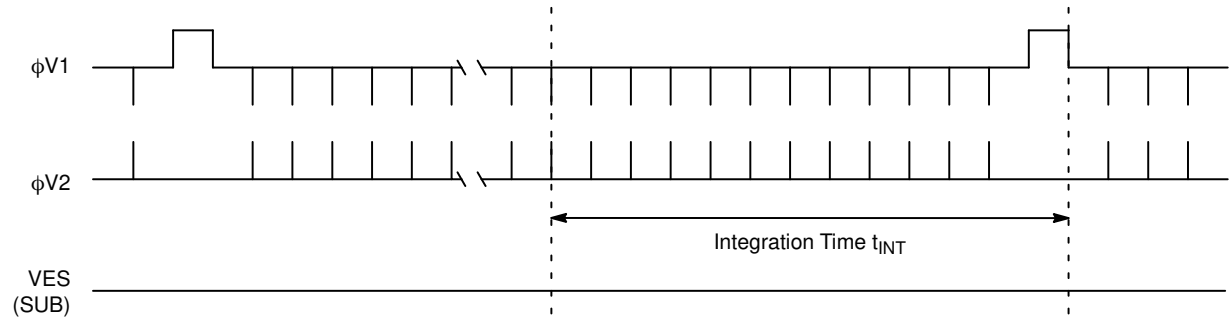


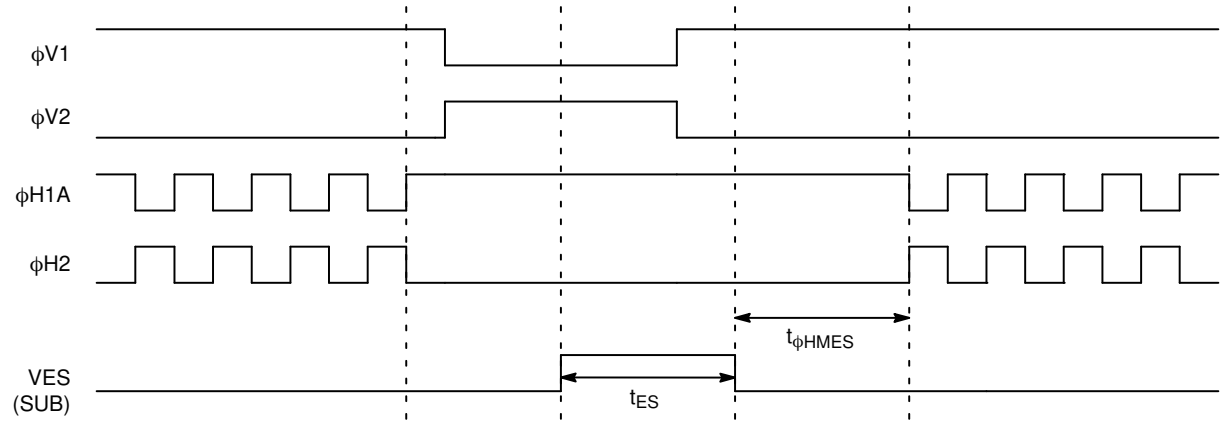
Figure 15. Pixel Timing − Single Resistor Readout

Electronic Shutter Timing − Single Register Readout

Electronic Shutter − Frame Timing



Electronic Shutter − Placement



Electronic Shutter − Operating Voltages

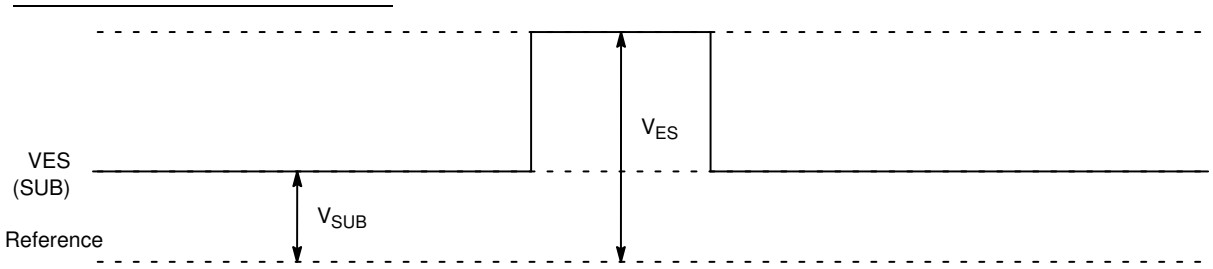
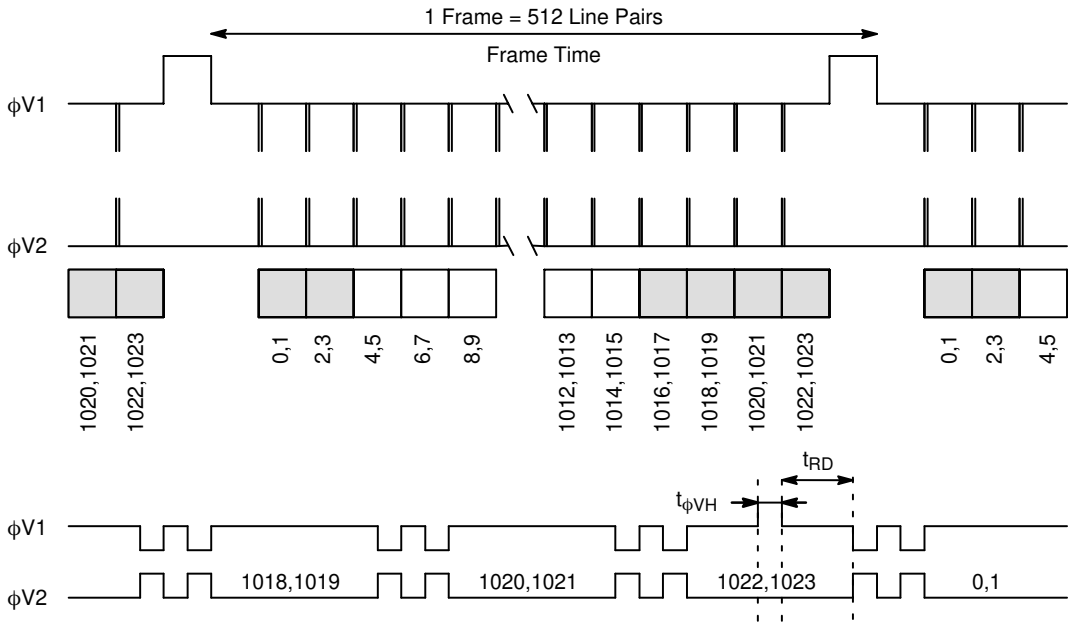


Figure 16. Electronic Shutter Timing − Single Register Readout

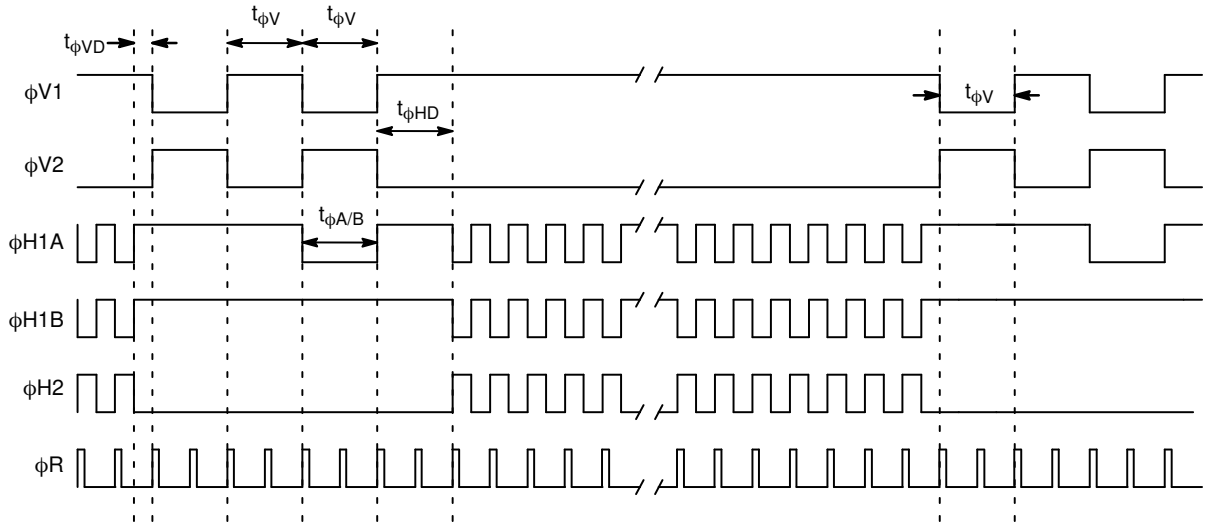
Frame Timing − Dual Register Readout



NOTE: When no electronic shutter is used, the integration time is equal to the frame time.

Figure 17. Frame Timing − Dual Resistor Readout

Line Timing − Dual Register Readout



Line Content

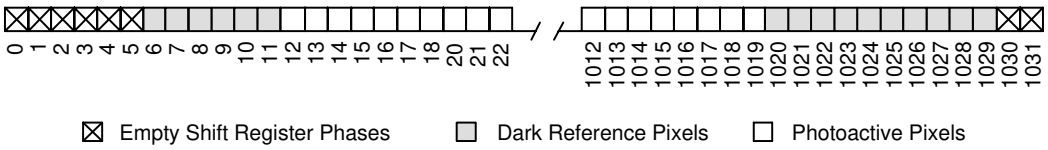


Figure 18. Line Timing − Dual Resistor Readout

Pixel Timing − Dual Register Readout

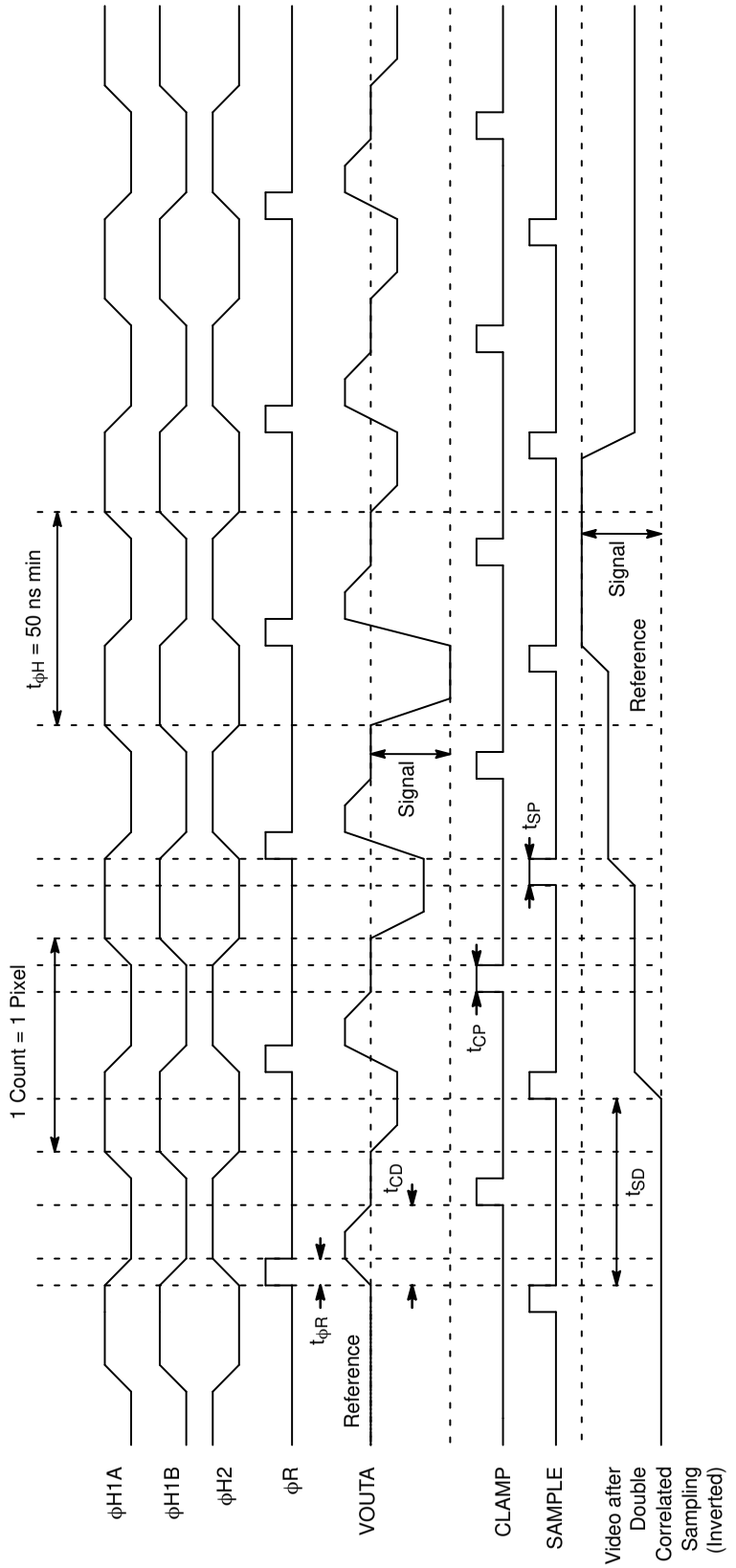


Figure 19. Pixel Timing − Dual Resistor Readout

Fast Dump Timing − Removing Four Lines

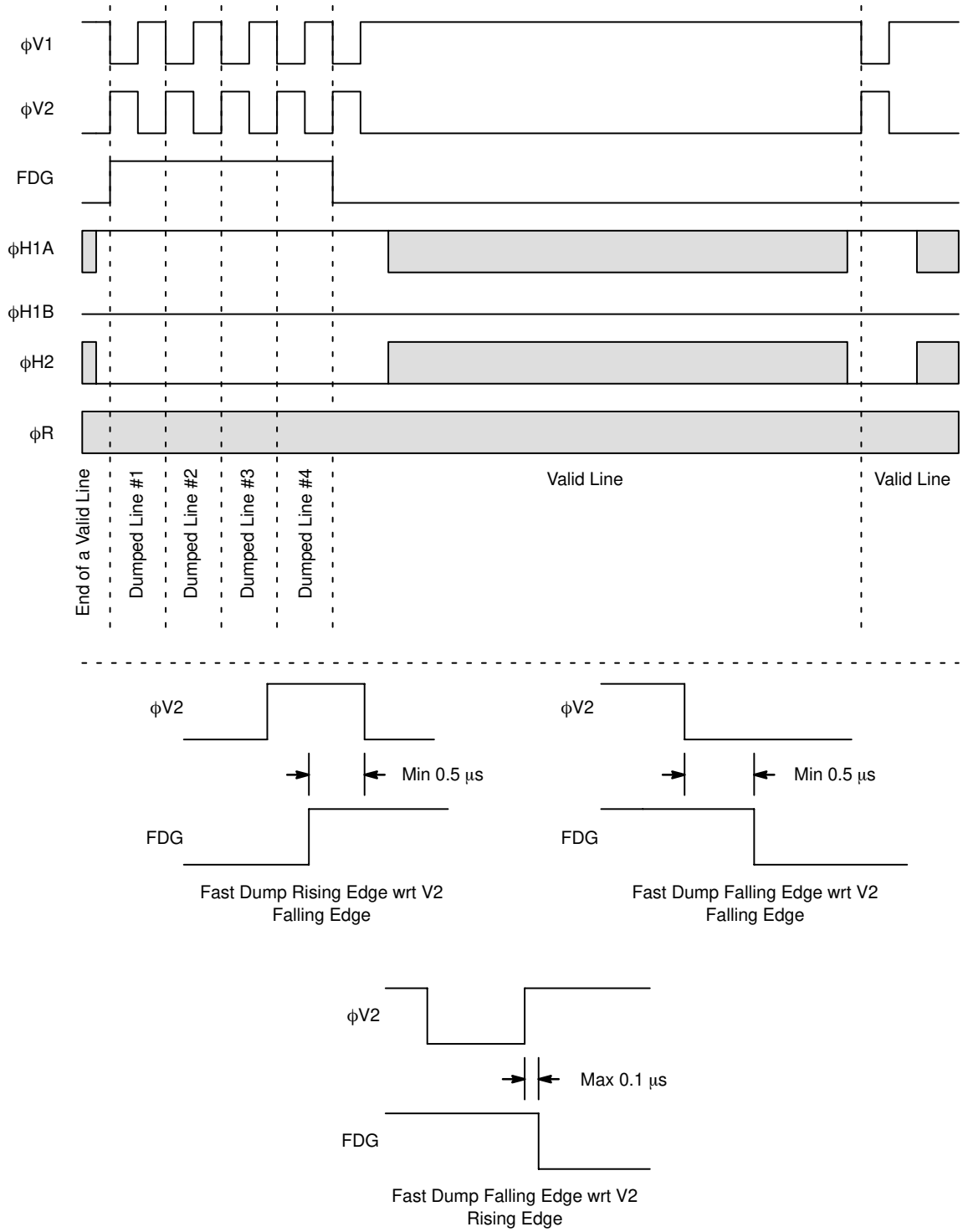


Figure 20. Fast Dump Timing − Removing Four Lines

Binning – Two to One Line Binning

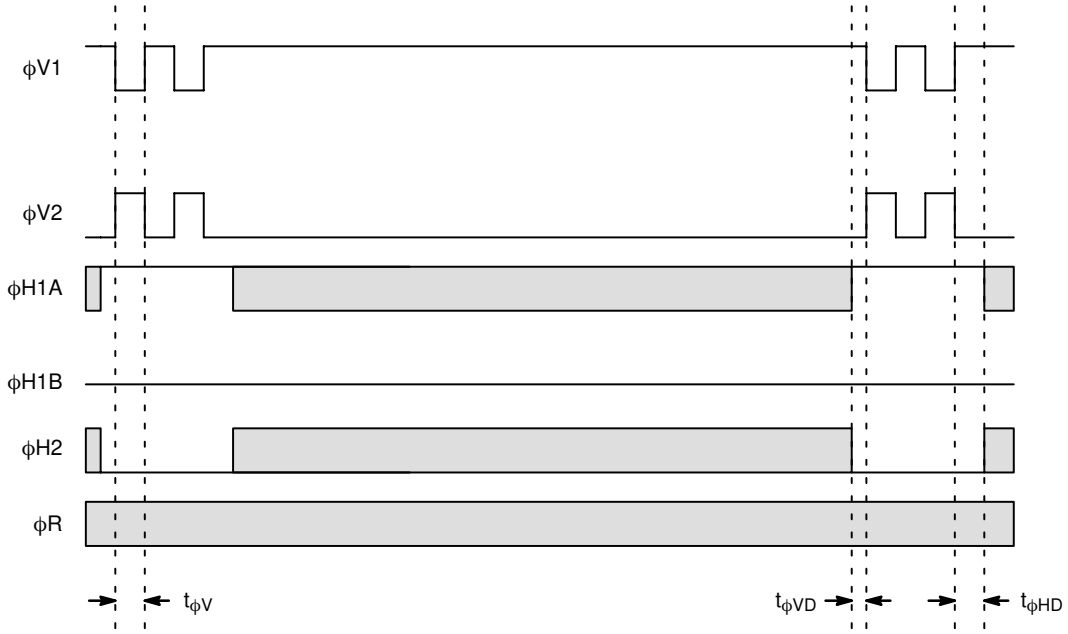


Figure 21. Binning – 2 to 1 Line Binning

Timing – Sample Video Waveform

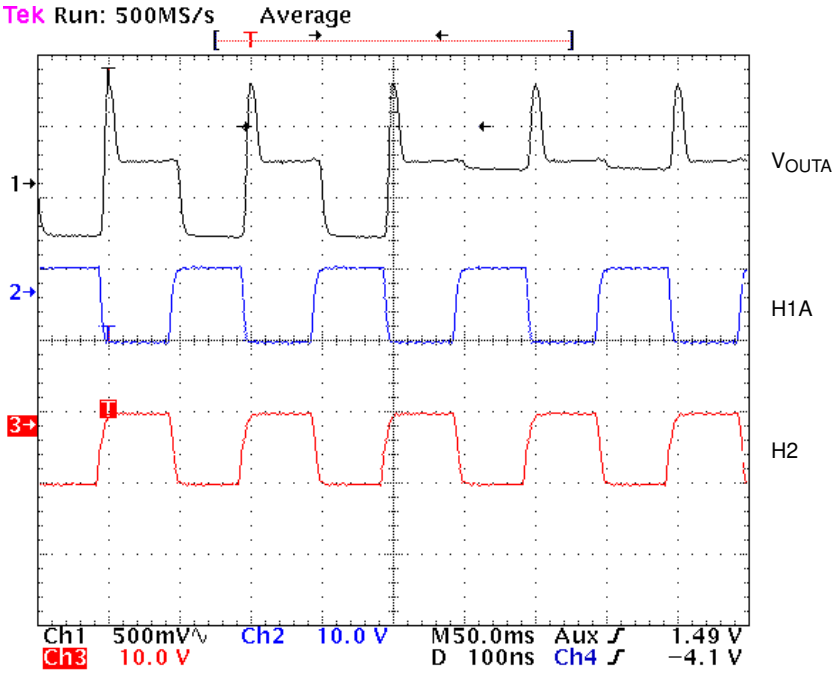


Figure 22. Sample Video Waveform at 5 MHz

STORAGE AND HANDLING

Table 14. CLIMATIC REQUIREMENTS

	Description	Min.	Max.	Unit	Conditions	Notes
Operation to Specification	Temperature	–25	40	°C	@ 10% ±5% RH	1, 2
	Humidity	10	86	% RH	@ 36±2°C Temp.	1, 2
Storage	Temperature	–55	70	°C	@ 10% ±5% RH	2, 3
	Humidity	–	95	% RH	@ 49±2°C Temp.	2, 3

1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
3. The image sensor shall meet the specifications of this document after storage for 15 days at the specified condition.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

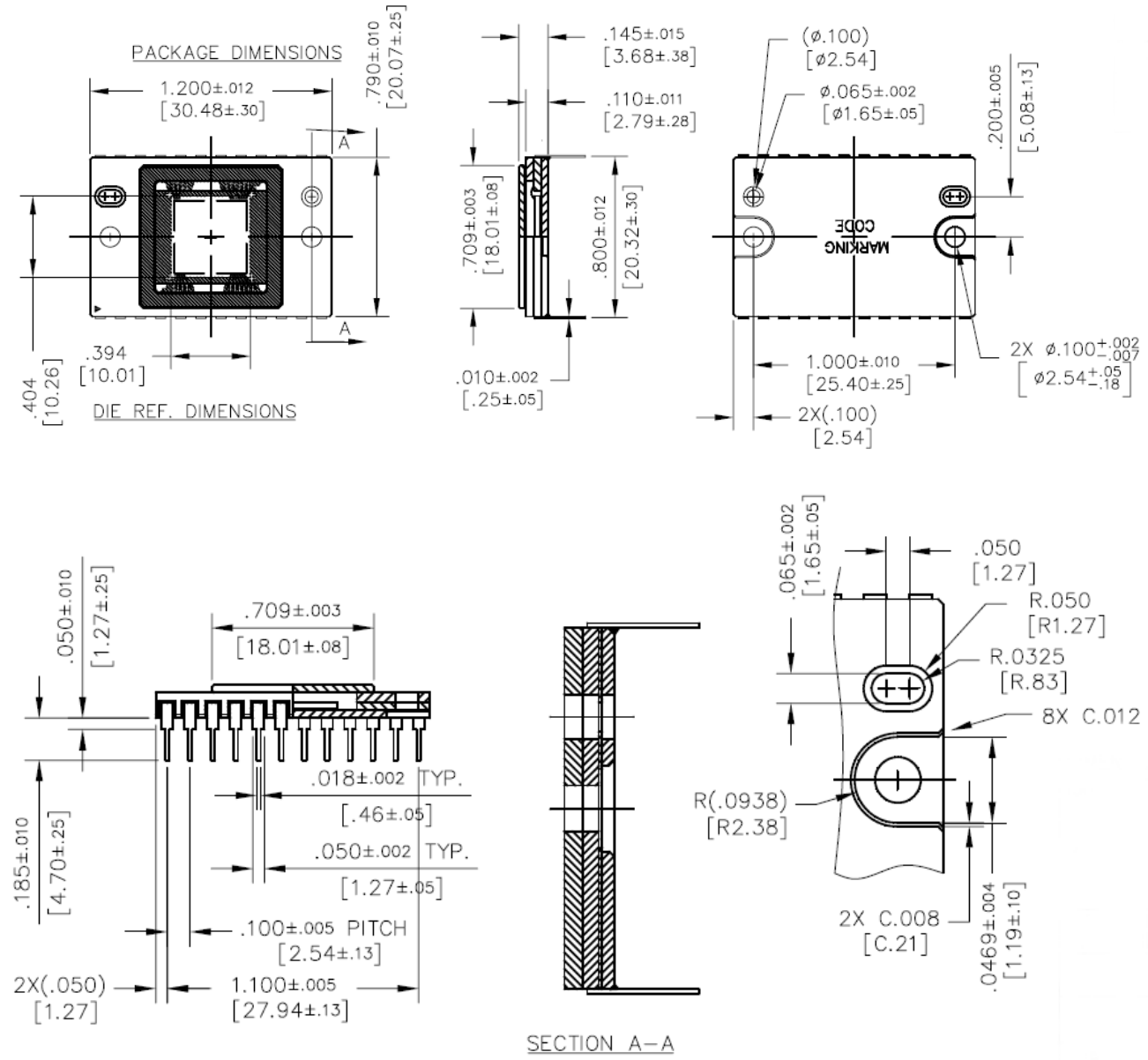
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

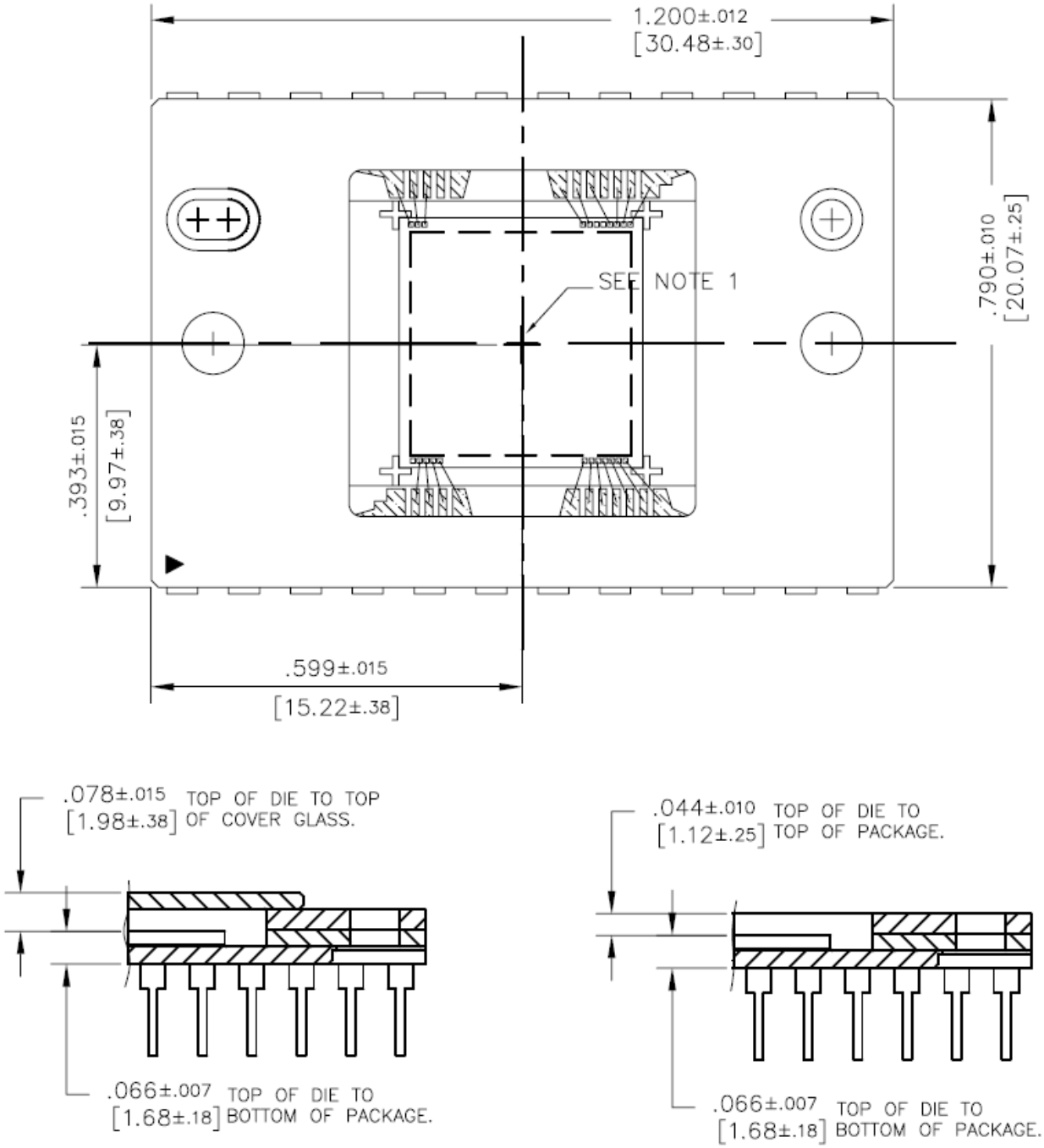
MECHANICAL INFORMATION

Completed Assembly



Note: Cover Glass is manually placed and visually aligned over die – location accuracy is not guaranteed.

Figure 23. Completed Assembly (1 of 2)



Notes:
1. Center of image area is offset from center of package by (−0.02, −0.06) mm nominal.
2. Die is aligned within ±2 degree of any package cavity edge.

Figure 24. Completed Assembly (2 of 2)