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KAI-2093

1920 (H) x 1080 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAI−2093 Image Sensor is a high−performance multi−megapixel image sensor designed for a wide range of medical imaging and machine vision applications.

The 7.4 μm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The split horizontal register offers a choice of single or dual output allowing either 15 or 30 frame per second (fps). The architecture allows for either progressive scan or interlaced readout. The imager features 5 V clocking to facilitate camera design. The vertical overflow drain structure provides antiblooming protection, and enables electronic shuttering for precise exposure control.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD, Progressive Scan or Interlaced Readout
Total Number of Pixels	1984 (H) × 1092 (V)
Number of Effective Pixels	1928 (H) × 1084 (V)
Number of Active Pixels	1920 (H) × 1080 (V)
Pixel Size	7.4 μm (H) × 7.4 μm (V)
Active Image Size	14.208 mm (H) × 7.992 mm (V), 16.3 mm (Diagonal)
Aspect Ratio	16:9
Number of Outputs	1 or 2
Saturation Signal	40,000 e^-
Output Sensitivity	14 μV/e^-
Quantum Efficiency −ABA (490 nm) −CBA (R = 620 nm, G = 540 nm, B = 460 nm)	 40% 37%, 34%, 30%
Total Noise	40 e^- rms
Dark Current (Typical)	< 0.5 nA/cm^2
Dynamic Range	60 dB
Maximum Pixel Clock Speed	40 MHz
Blooming Suppression	100 X
Smear	< 0.03%
Image Lag	< 10 electrons
Frame Rate Single Output, 20 MHz Single Output, 35 MHz Dual Output, 20 MHz Dual Output, 37 MHz	 9 fps 15 fps 17 fps 30 fps
Maximum Data Rate	40 MHz/Channel (2 Channels)
Package	32 pin CerDIP
Cover Glass	Clear Glass or Quartz Glass with AR Coating (2 sides)

NOTE: Parameters above are specified at T = 40°C unless otherwise noted.

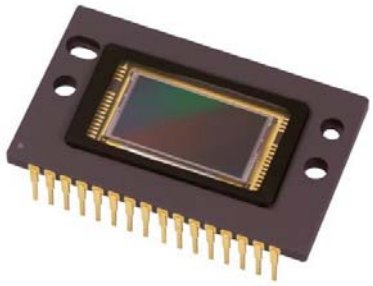


Figure 1. KAI−2093 Interline CCD Image Sensor

Features

- Progressive Scan (Non−interlaced)
- HCCD and Output Amplifier Capable of 40 MHz Operation
- 5 V HCCD Clocking
- Single or Dual Video Output Operation
- 28 Light Shielded Reference Columns per Output
- Only 2 Vertical CCD Clocks and 2 Horizontal CCD Clocks
- Electronic Shutter
- Low Dark Current

Applications

- Intelligent Transportation Systems
- Machine Vision
- Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−2093 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−2093−AAA−CP−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	KAI−2093 Serial Number
KAI−2093−AAA−CP−BA	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade	
KAI−2093−ABA−CB−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Sample	KAI−2093M Serial Number
KAI−2093−ABA−CB−B1	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Grade 1	
KAI−2093−ABA−CB−B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Grade 2	
KAI−2093−ABA−CK−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Quartz Cover Glass with AR Coating (Both Sides), Engineering Sample	
KAI−2093−ABA−CK−BA	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Quartz Cover Glass with AR Coating (Both Sides), Standard Grade	
KAI−2093−ABA−CP−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	
KAI−2093−ABA−CP−BA	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade	
KAI−2093−CBA−CB−AE	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Sample	KAI−2093CM Serial Number
KAI−2093−CBA−CB−BA	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAI−2093−10−40−A−EVK	Evaluation Board, 10 Bit, 40 MHz (Complete Kit)
KAI−2093−12−20−A−EVK	Evaluation Board, 12 Bit, 20 MHz (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

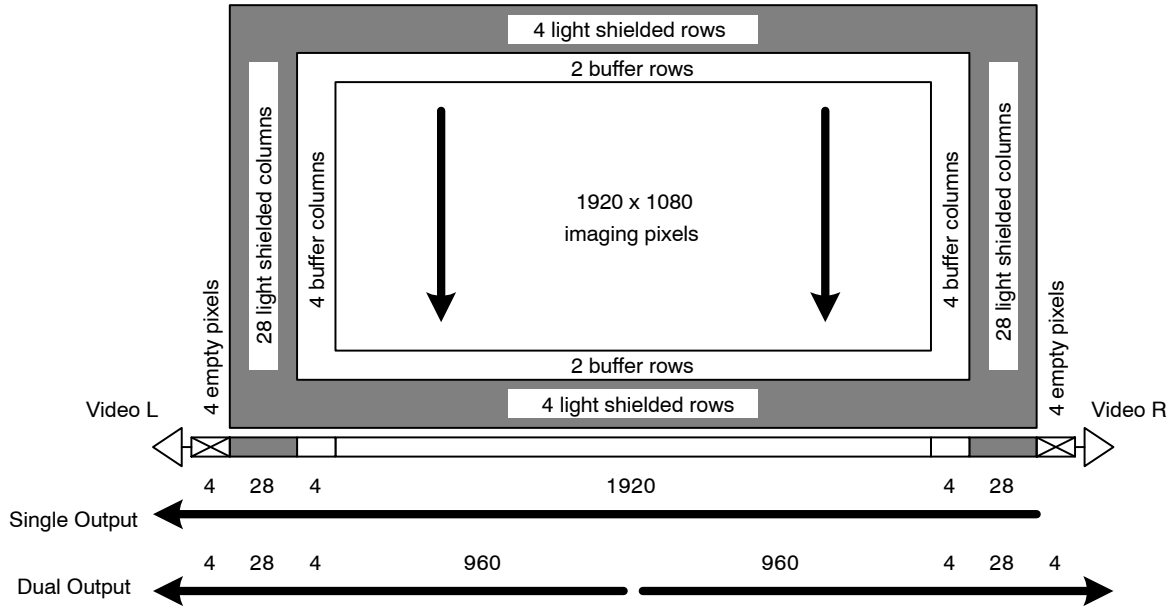


Figure 2. Sensor Architecture

There are 4 light shielded rows followed by 1084 photoactive rows and finally 4 more light shielded rows. The first and last 2 photoactive rows are buffer rows giving a total of 1080 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first four empty pixels of each line do not receive charge from the vertical shift register. The next 28 pixels receive charge from the left light shielded edge followed by 1928 photoactive pixels and finally 28 more light shielded pixels from the right edge of the sensor. The first and last 4 photoactive pixels are buffer pixels giving a total of 1920 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 4 empty pixels followed by 28 light shielded pixels followed by 964 photoactive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

Pin Description and Physical Orientation

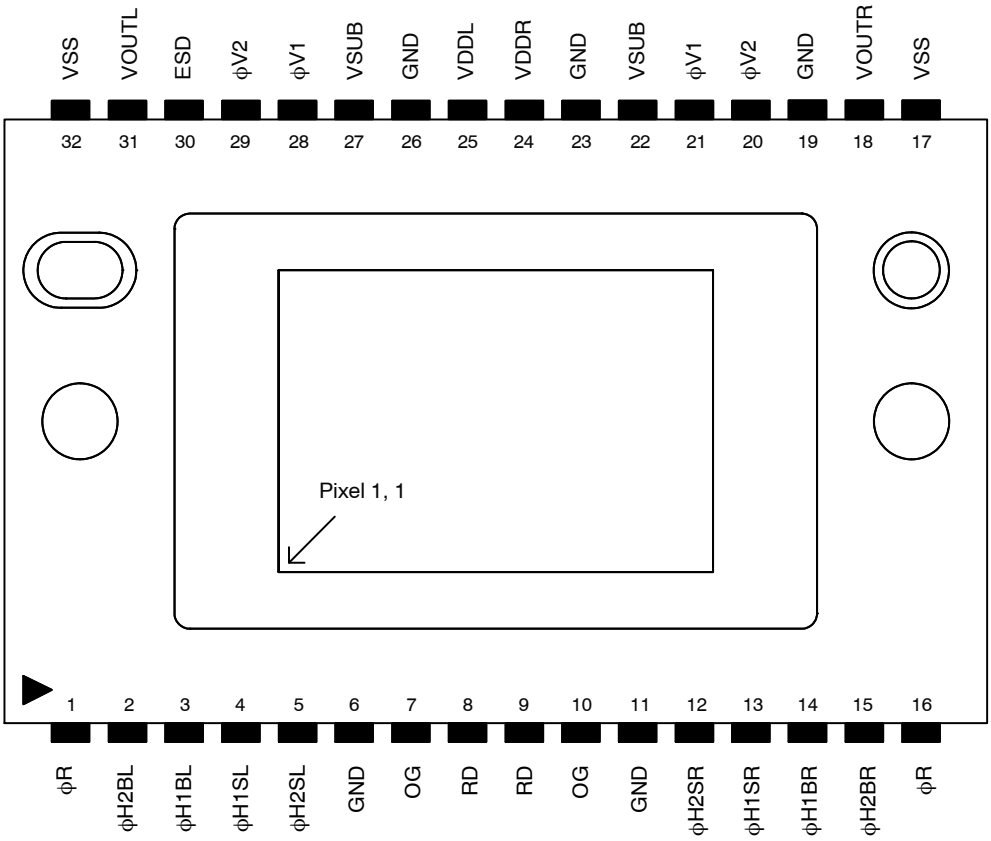


Figure 3. Package Pin Designations − Top View

Table 4. PIN DESCRIPTION

Pin	Label
1	ϕRL
2	ϕH2BL
3	ϕH1BL
4	ϕH1SL
5	ϕH2SL
6	GND
7	OG
8	RD
9	RD
10	OR
11	GND
12	ϕH2SR
13	ϕH1SR
14	ϕH1BR
15	ϕH2BR
16	ϕR

Pin	Label
17	VSS
18	VOUTR
19	GND
20	ϕV2O
21	ϕV1
22	VSUB
23	GND
24	VDDR
25	VDDL
26	GND
27	VSUB
28	ϕV1
29	ϕV2E
30	ESD
31	VOUTL
32	VSS

The horizontal shift register is on the side of the sensor parallel to the row of pins 1 through 16. In single output mode the pixel closest to pin 1 will be read out first through Video L, the pixel closest to pin 17 will be read out last. In dual output mode the pixel closest to pin 16 will be read out first through Video R.

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATIONAL CONDITIONS

Description	Condition
Temperature	40°C
Integration Time	33 ms (40 MHz HCCD Frequency, 30 fps Frame Rate)
Operation	Nominal Voltages and Timing

NOTE: Image defects are excluded from performance tests.

Specifications

Table 6. OPTICAL SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Peak Quantum Efficiency	QE_{MAX}	33	36		%	1
Peak Quantum Efficiency Wavelength	λQE		490		nm	1
Quantum Efficiency at 540 nm	QE(540)	31	33		%	1
Microlens Acceptance Angle (horizontal)	θQE*h*	±12	±13		degrees	2
Microlens Acceptance Angle (vertical)	θQE*v*	±25	±30		degrees	2
Maximum Photoresponse Non-Linearity	NL		2		%	3, 4
Maximum Gain Difference between Outputs	ΔG		10		%	3, 4
Maximum Signal Error caused by Non-Linearity Differences	ΔNL		1		%	3, 4

1. For monochrome sensors.
2. Value is the angular range of incident light for which the quantum efficiency is at least 50% of QE_{max} at a wavelength of λQE. Angles are measured with respect to the sensor surface normal in a plane parallel to the horizontal axis (θQE*h*) or in a plane parallel to the vertical axis (θQE*v*).
3. Value is over the range of 10% to 90% of photodiode saturation.
4. Value is for the sensor operated without binning.

Table 7. CCD SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Vertical CCD Charge Capacity	V_{Ne}	45	50		ke^-	
Horizontal CCD Charge Capacity	H_{Ne}		100		ke^-	
Photodiode Charge Capacity	P_{Ne}	35	40		ke^-	1
Dark Current	I_D		0.3	1.0	nA/cm^2	
Image Lag	Lag		< 10	50	e^-	2
Anti-Blooming Factor	X_{AB}	100	300			3, 4, 5, 6
Vertical Smear	Smr		−75	−72	dB	3, 4

1. This value depends on the substrate voltage setting. Higher photodiode saturation charge capacities will lower the antiblooming specification. Substrate voltage will be specified with each part for nominal photodiode charge capacity.
2. This is the first field decay lag at 70% saturation. Measured by strobe illumination of the device at 70% of photodiode saturation, and then measuring the subsequent frame's average pixel output in the dark.
3. Measured with a spot size of 100 vertical pixels.
4. Measured with F/4 imaging optics and continuous green illumination centered at 550 nm.
5. A blooming condition is defined as when the spot size doubles in size.
6. Antiblooming factor is the light intensity which causes blooming divided by the light intensity which first saturates the photodiodes.

Table 8. OUTPUT AMPLIFIER SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Power Dissipation	P_D		120		mW	1
Bandwidth	f_{-3DB}		140		MHz	1
Max Off−chip Load	C_L		10		pF	2
Gain	A_V		0.75			1
Sensitivity	$\Delta V/\Delta N$		14		$\mu V/e^-$	1

1. For a 5 mA output load on each amplifier. Per amplifier.
2. With total output load capacitance of C_L = 10 pF between the outputs and AC ground.

Table 9. GENERAL SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Total Noise	n_{e-T}		40		e^- rms	1
Dynamic Range	DR		60		dB	2

1. Includes system electronics noise, dark pattern noise and dark current shot noise at 20 MHz.
2. Uses $20LOG(P_{Ne}/n_{e-T})$

TYPICAL PERFORMANCE CURVES

Monochrome Quantum Efficiency

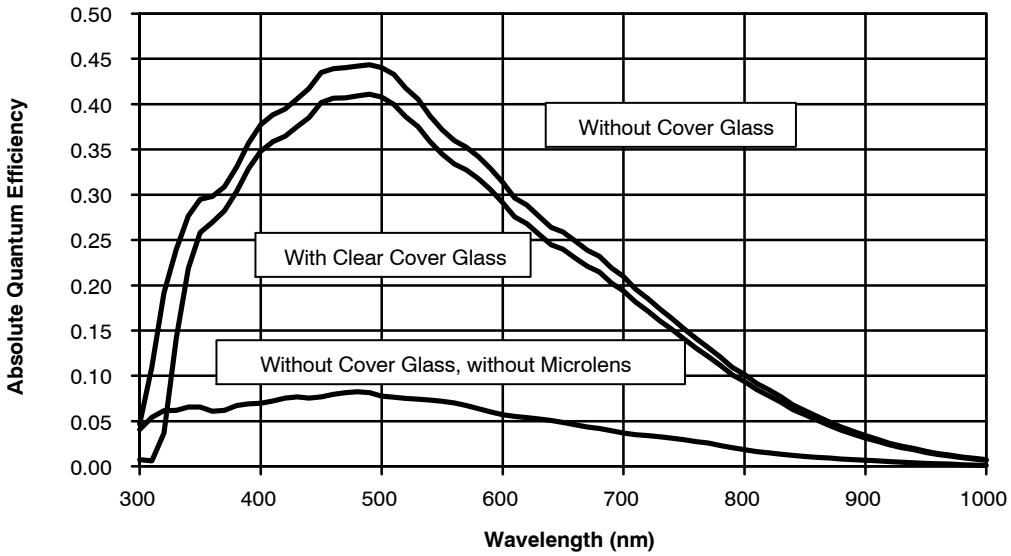


Figure 4. Quantum Efficiency Spectrum for Monochrome Sensors

Monochrome with Microlens Angular Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

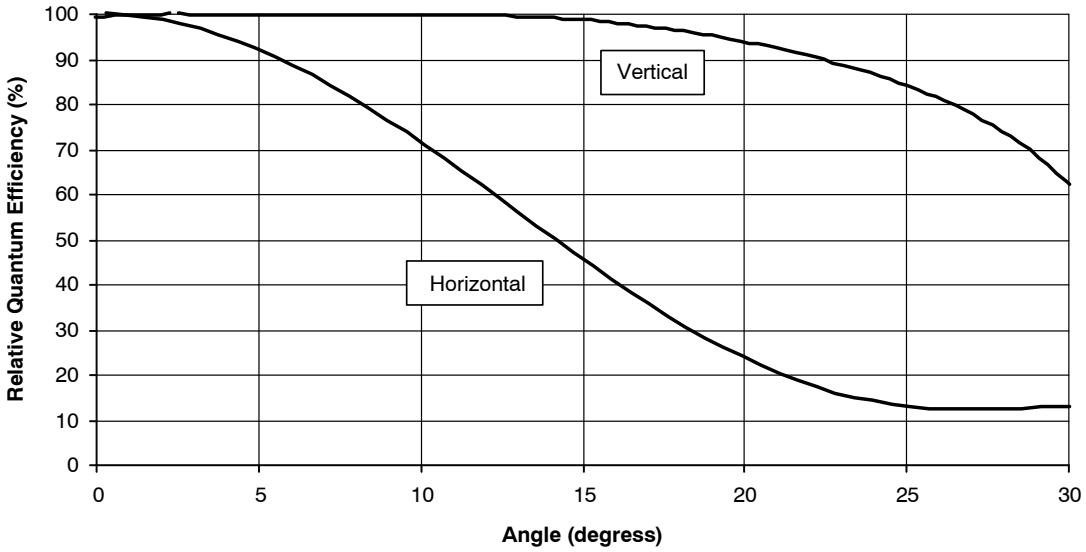


Figure 5. Angular Dependence of Quantum Efficiency

Color with Microlens Quantum Efficiency

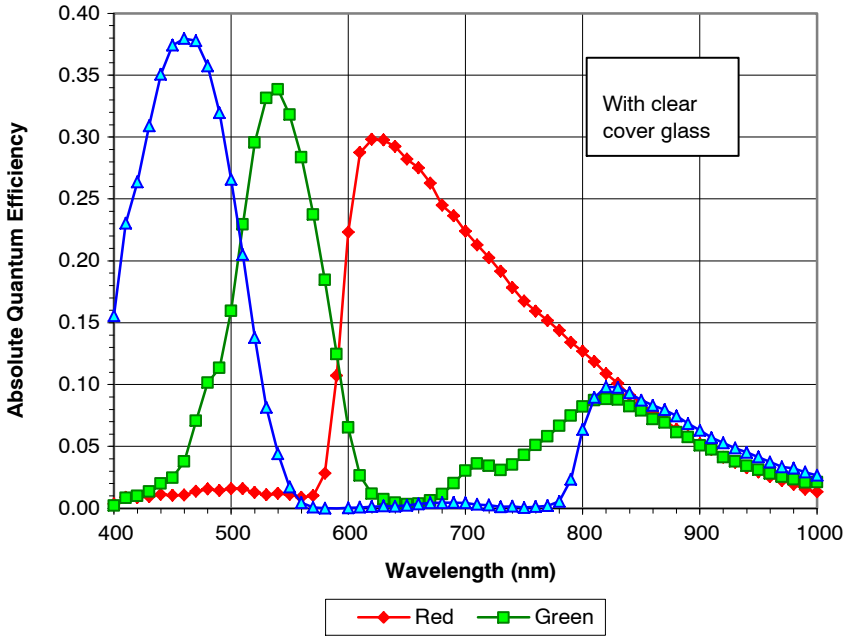


Figure 6. Quantum Efficiency Spectrum for Color Filter Array Sensors

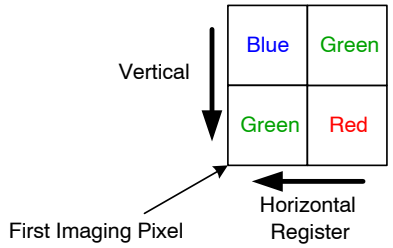


Figure 7. Color Filter Array Pattern

Frame Rates

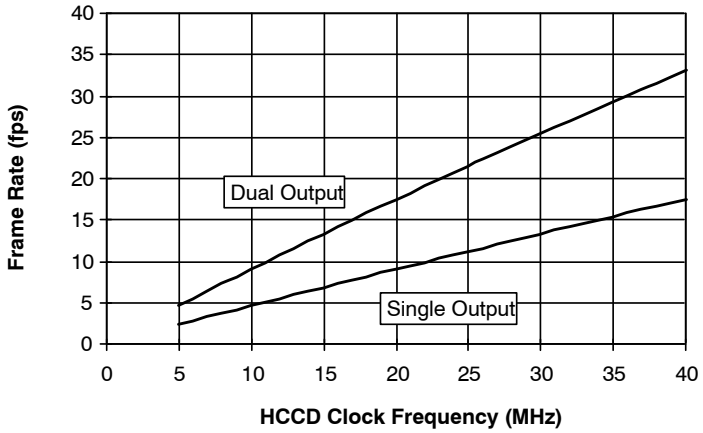


Figure 8. Frame Rates

DEFECT DEFINITIONS

Table 10. OPERATIONAL CONDITIONS

Description	Condition
Temperature	40°C
Integration Time	33 ms (40 MHz HCCD Frequency, No Binning, 30 fps Frame Rate)
Light Source	Continuous Green Illumination Centered at 550 nm
Operation	Nominal Voltages and Timing

Table 11. SPECIFICATIONS

Name	Definition
Major Defective Pixel	A pixel whose signal deviates by more than 25 mV from the mean value of all active pixels under dark field condition or by more than 15% from the mean value of all active pixels under uniform illumination of 80% of saturation.
Minor Defective Pixel	A pixel whose signal deviates by more than 8 mV from the mean value of all active pixels under dark field conditions.
Cluster Defect	A group of 2 to 10 contiguous major defective pixels with a width no wider than 2 defective pixels.
Column Defect	A group of more than 10 contiguous major defective pixels along a single column.

1. There will be at least two non−defective pixels separating any two major defective pixels.
2. Buffer and dark reference pixels are not used for defect tests.

Defect Zones

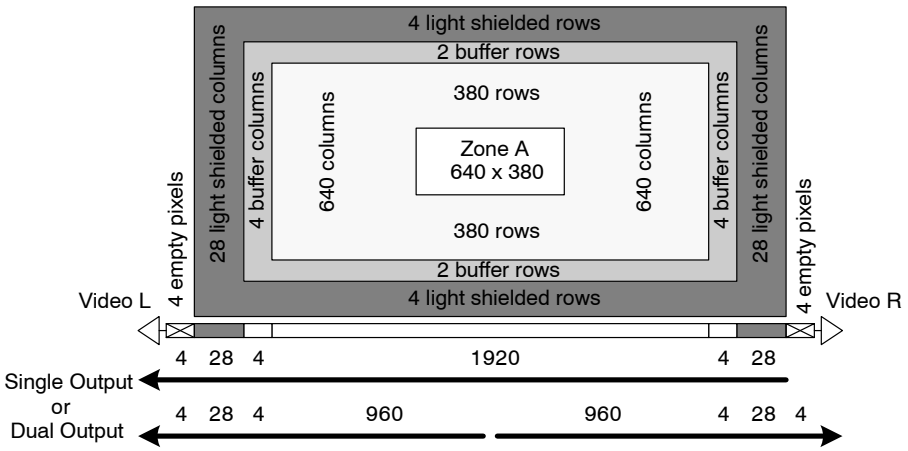


Figure 9. Defect Zones

Defect Classes

Table 12. MAXIMUM NUMBER OF DEFECTS

Major Point		Minor Point		Cluster		Column	
KAI−2093−ABA−CB−B1							
Within Zone A	Outside Zone A	Within Zone A	Outside Zone A	Within Zone A	Outside Zone A	Within Zone A	Outside Zone A
3	10	20	100	0	4	0	0
All Other Part Numbers (Zone A is not used)							
10		100		4		0	

OPERATION

Table 13. ABSOLUTE MAXIMUM RATINGS

Description		Minimum	Maximum	Units	Notes
Temperature	Operation without damage	−50	70	°C	
Voltage between pins	VSUB to GND	8	20	V	1, 3
	VDD, OG to GND	0	17	V	
	VRD to GND	0	14	V	
	ϕV1 to ϕV2	−20	20	V	
	ϕH1 to ϕH2	−15	15	V	
	ϕR to GND	−15	15	V	
	ϕH1, ϕH2 to OG	−15	15	V	
	ϕH1, ϕH2 to ϕV1, ϕV2	−15	15	V	
Current	Video Output Bias Current	0	10	mA	2

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For electronic shuttering VSUB may be pulsed to 50 V for up to 10 μs.
2. Total for both outputs. Current is 5 mA for each output. Note that the current bias affects the amplifier bandwidth.
3. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visibility Lighting Conditions*.

Table 14. DC BIAS OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Output Gate	OG	−3.0	−2.5	−2.0	V	
Reset Drain	VRD	10.0	10.5	11.0	V	
Output Amplifier Return	V_{SS}	0.0	0.7	1.0	V	
Output Amplifier Supply	V_{DD}	14.5	15.0	15.5	V	
Ground, P−well	GND		0.0		V	
Substrate	VSUB	8.0	TBD	17.0	V	2
ESD Protection	VESD	−8.0	−7.0	−6.0	V	1

1. V_{ESD} must be at least 1 V more negative than ϕH1L and ϕH2L during sensors operation AND during camera power turn on.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

AC Operating Conditions

Table 15. CLOCK LEVELS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Vertical CCD Clock High	ϕV2H	7.5	8.0	8.5	V	
Vertical CCD Clocks Midlevel	ϕV1M, ϕV2M	−1.6	−1.5	−1.4	V	
Vertical CCD Clocks Low	ϕV1L, ϕV2L	−9.5	−9.0	−8.5	V	
Horizontal CCD Clocks High	ϕH1H, ϕH2H	0.5	1.0	2.0	V	
Horizontal CCD Clocks Low	ϕH1L, ϕH2L	−5.0	−4.0	−3.8	V	
Reset Clock Amplitude	ϕR		5.0		V	
Reset Clock Low	ϕRL	−4.0	−3.5	−3.0	V	
Electronic Shutter Voltage	$V_{SHUTTER}$	44	48	52	V	1

1. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

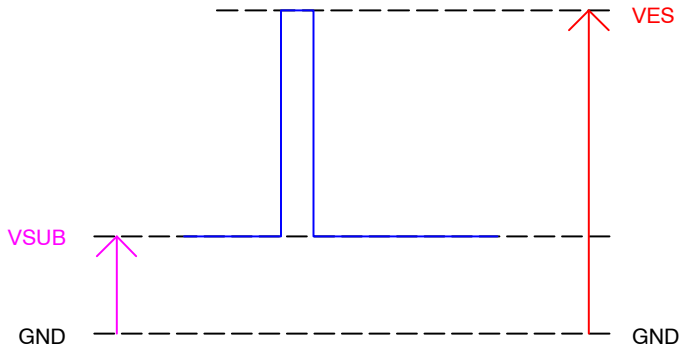


Figure 10. DC Bias and AC Clock Applied to the SUB Pin

Table 16. CLOCK CAPACITANCE

Clocks	Capacitance	Units	Notes
ϕV1 to GND	25	nF	1
ϕV2 to GND	25	nF	1
ϕV1 to ϕV2	5	nF	
ϕH1S to GND	45	pF	2
ϕH2S to GND	38	pF	2
ϕH1B to GND	21	pF	2
ϕH2B to GND	20	pF	2
ϕH2B to ϕH1S	10	pF	2
ϕH1B to ϕH1S	10	pF	2
ϕH2B to ϕH2S	10	pF	2
ϕH1B to ϕH2S	10	pF	2
ϕR to GND	10	pF	

1. Gate capacitance to GND is voltage dependent. Value is for nominal VCCD clock voltages.
2. For nominal HCCD clock voltages, total capacitance for one half (H1SR only or H1SL only).

Operation Notes

Progressive and Interlaced Timing

Progressive and interlaced output modes are achieved by the applying the proper waveforms to the vertical clock input pins ϕV1, ϕV2E and ϕV2O. For progressive output, ϕV2 = ϕV2E = ϕV2O, with each of the 1092 lines read out individually using the timing in Figures 11 and 12.

For interlaced output, there are two modes, field integration mode and frame integration mode. In both modes, 1092/2 = 546 lines are read in each frame readout, with one even frame readout and one odd frame readout necessary for a complete frame. Field integration mode bins together alternate lines, and the timing is shown in Figures 14 and 15. As with progressive readout, ϕV2 = ϕV2E = ϕV2O.

Frame integration mode reads out the photodiodes of the even and odd lines separately, and the timing is shown in Figures 16 and 17. In this case, ϕV2E and ϕV2O are clocked individually.

Single Output Mode

When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 31). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 24) and VOUTR (pin 18) to GND (zero volts).

The ϕH1 timing from the timing diagrams should be applied to ϕH1SL, ϕH1BL, ϕH1SR, ϕH2BR, and the ϕH2 timing should be applied ϕH2SL, ϕH2BL, ϕH2SR, ϕH1BR. In other words, the clock driver generating the ϕH1 timing should be connected to pins 4, 3, 13, and 15. The clock driver generating the ϕH2 timing should be connected to pins 2, 5, 12, and 14.

The horizontal CCD should be clocked for 4 empty pixels plus 28 light shielded pixels plus 1928 photoactive pixels plus 28 light shielded pixels for a total of 1988 pixels.

Dual Output Mode

In dual output mode the connections to the ϕH1BR and ϕH2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 25, 24) should be connected to 15 V.

The ϕH1 timing from the timing diagrams should be applied to ϕH1SL, ϕH1BL, ϕH1SR, ϕH1BR, and the ϕH2 timing should be applied to ϕH2SL, ϕH2BL, ϕH2SR, ϕH2BR. The clock driver generating the ϕH1 timing should be connected to pins 4, 3, 13, and 14. The clock driver generating the ϕH2 timing should be connected to pins 2, 5, 12, and 15.

The horizontal CCD should be clocked for 4 empty pixels plus 28 light shielded pixels plus 964 photoactive pixels for a total of 996 pixels.

If the camera is to have the option of dual or single output mode, the clock driver signals sent to ϕH1BR and ϕH2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for ϕH1BR and ϕH2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the ϕH1BR and ϕH2BR clocks occur at the same time (within 3 ns) as the other HCCD clocks.

Exposure Control

If the sensor is operated at 20 MHz horizontal CCD frequency then the frame rate will be 9 fps and the integration time will be 1/9 s or 111 ms. To achieve shorter integration times, the electronic shutter option may be used by applying a pulse to the substrate (pins 22 and 27). The time between the falling edge of the substrate pulse and the falling edge of the transition of the ϕV2 clock from ϕV2H to ϕV2M is defined as the integration time. The substrate pulse and integration time are shown in Figure 14.

Integration times longer than one frame time (111 ms in this example) do not require use of the electronic shutter. Without the electronic shutter the integration time is defined as the time between when the ϕV2 clock is at the ϕV2H level of 9.5 V (when the ϕV2 clock is at the ϕV2H level charge collected in the photodiodes is transferred to the vertical shift register). To extend the integration time, increase the time between each ϕV2H level of the ϕV2 clock. While the photodiodes are integrating photoelectrons the vertical and horizontal shift registers should be continuously clocked to prevent the collection of dark current in the vertical shift register. This is most easily done by increasing the number of lines read out of the image sensor. For example, to double the integration time read out 2184 lines instead of 1092 lines (but remember only the first 1092 lines will contain image data).

Depending on the image quality desired and temperature of the sensor, integration times longer than one second may require the sensor to be cooled to control dark current. The output amplifiers will also generate a non−uniform dark current pattern near the bottom corners of the sensor. This can be reduced at long integration times by only turning on VDD to each amplifier during image readout. If the vertical and horizontal shift registers are also stopped during integration time, the dark current in the shift registers should be flushed out completely before transferring charge from the photodiodes to the vertical shift register.

Dark Reference

There are 28 light shielded columns at the left and right side of the image sensor. The first and last two light shielded columns should not be used as a dark reference due to some light leakage under the edges of the light shielding. Only the center 24 columns should be used for dark reference line clamping. There are 4 light shielded rows at the top and bottom of the image sensor. Only the center two light shielded rows should be used as a dark reference.

Connections to the Image Sensor

The reset clock signal operates at the pixel frequency. The traces on the circuit board to the reset clock pins should be kept short and of equal length to ensure that the reset pulse arrives at each pin simultaneously. The circuit board traces to the horizontal clock pins should also be placed to ensure that the clock edges arrive at each pin simultaneously. If reset pulses and the horizontal clock edges are misaligned the noise performance of the sensor will be degraded and balancing the offset and gain of the two output amplifiers will be difficult.

The bias voltages on OG, RD, VSS and VDD should be well filtered with capacitors placed as close to the pins as possible. Noise on the video outputs will be most strongly affected by noise on VSS, VDD, GND, and VSUB. If the electronic shutter is not used then a filtering capacitor should also be placed on VSUB. If the electronic shutter is used, the VSUB voltage should be kept as clean and noise free as possible.

The voltage on VSS may be set by using the 0.6 to 0.7 volt drop across a diode. Place the diode from VSS to GND. To disable one of the output amplifiers connect VDD to GND, do not let VDD float.

The ESD voltage must reach its operating point before any of the horizontal clocks reach their low level. If any pin on the sensor comes within 1 V of the ESD pin the electrostatic damage protection circuit will become active and will not turn off until all voltages are powered down. Operating the sensor with the ESD protection circuit active may damage the sensor.

TIMING

Table 17. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Unit
HCCD Delay	t_{HD}	1.3	1.5	10.0	μs
VCCD Transfer Time	t_{VCCD}	1.3	1.5		μs
Photodiode Transfer Time	t_{V3rd}	8.0	12.0	15.0	μs
VCCD Pedestal Time	t_{3P}	20.0	25.0	50.0	μs
VCCD Delay	t_{3D}	15.0	20.0	100.0	μs
Reset Pulse Time	t_{R}	5.0	10.0		ns
Shutter Pulse Time	t_{S}	3.0	5.0	10.0	μs
Shutter Pulse Delay	t_{SD}	1.0	1.6	10.0	μs
HCCD Clock Period	t_{H}	25.0	50.0	200.0	ns
VCCD Rise/Fall Time	t_{VR}	0.0	0.1	1.0	μs
Vertical Clock Edge Alignment	t_{VE}	0.0		100.0	ns

Frame Timing

Frame Timing − Progressive Scan

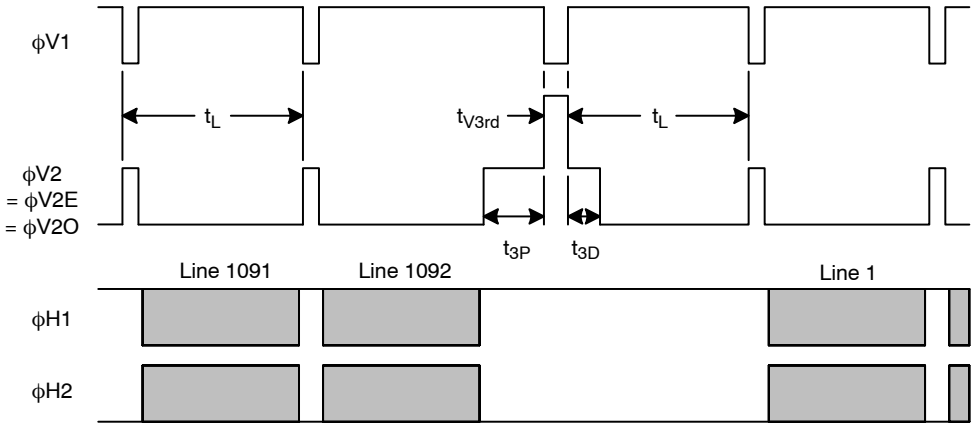


Figure 11. Progressive Frame Timing

Frame Timing for Vertical Binning by 2 − Progressive Scan

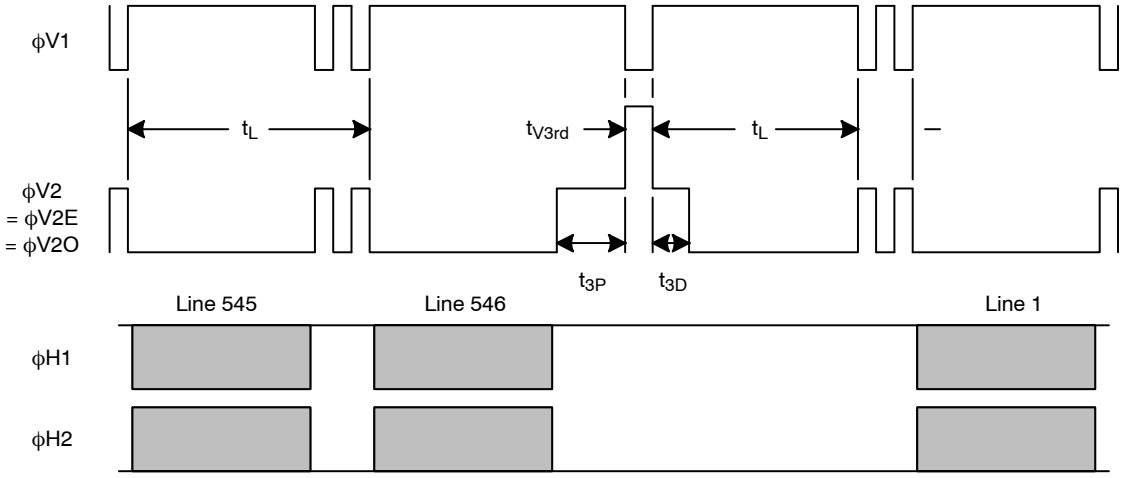


Figure 12. Frame Timing for Vertical Binning by 2

Vertical Clock Edge Alignment

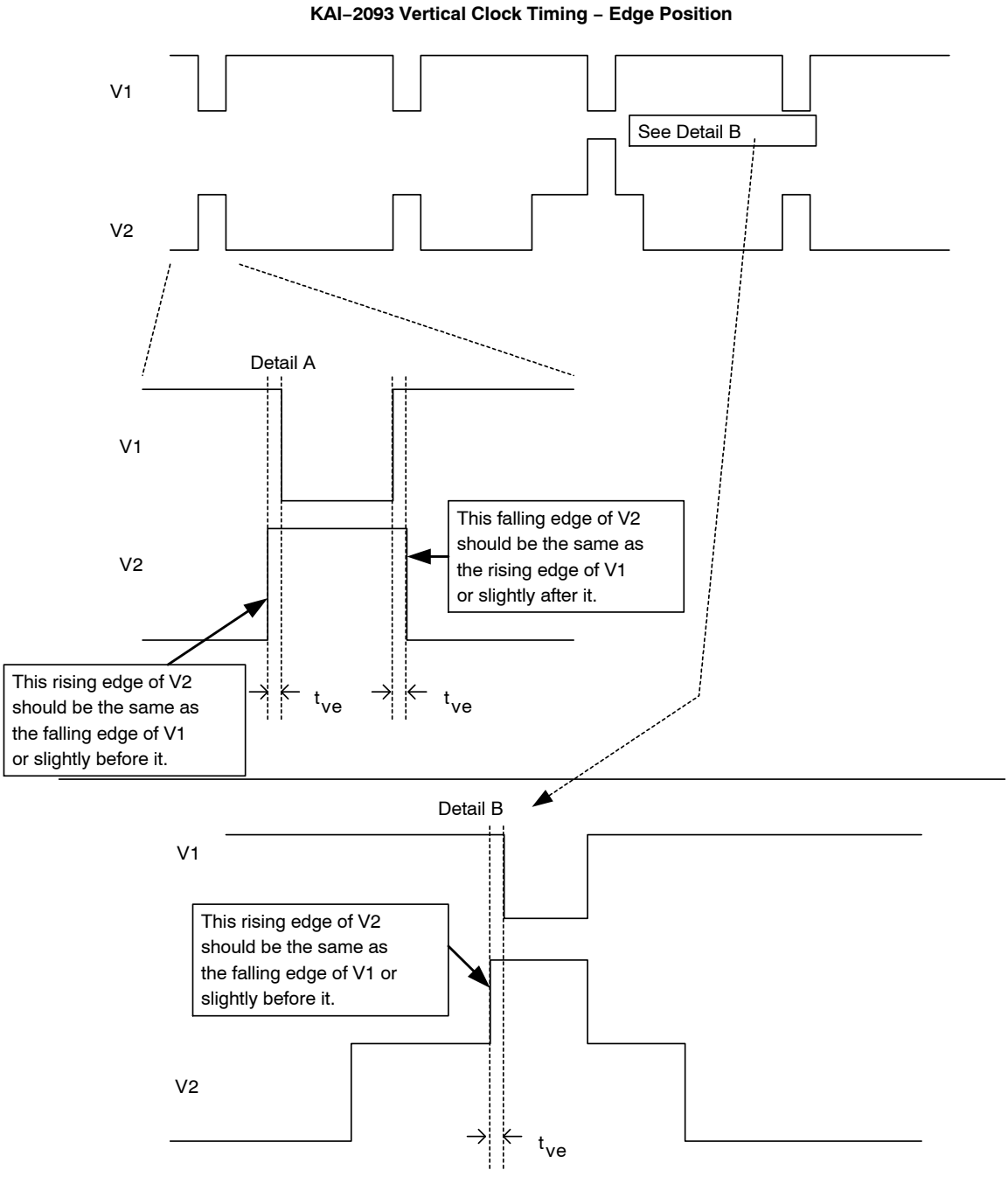


Figure 13. Ideal Vertical Clock Edge Position

Frame Timing − Field Integration Mode

Interlaced Frame Timing − Field Integration Mode − Even Field Readout

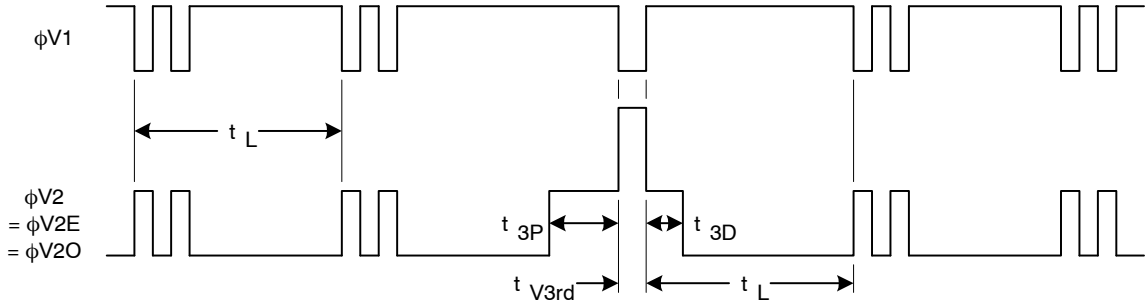


Figure 14. Interlaced Frame Timing − Field Integration Mode − Even Field Readout

Interlaced Frame Timing − Field Integration Mode − Odd Field Readout

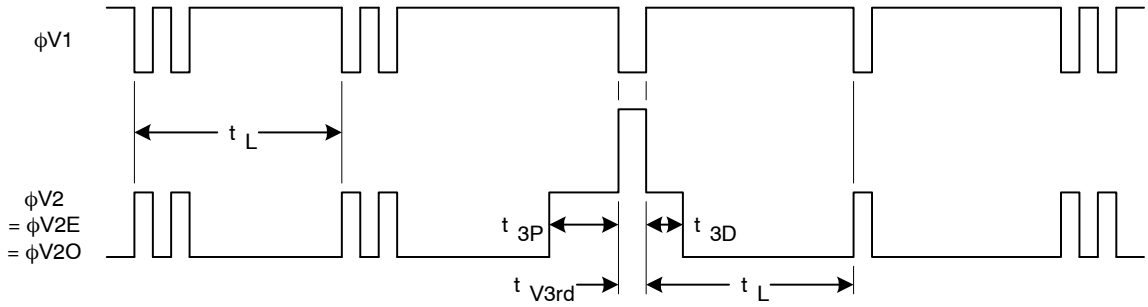


Figure 15. Interlaced Frame Timing − Field Integration Mode − Odd Field Readout

Frame Timing − Frame Integration Mode

Interlaced Frame Timing − Frame Integration Mode − Even Field Readout

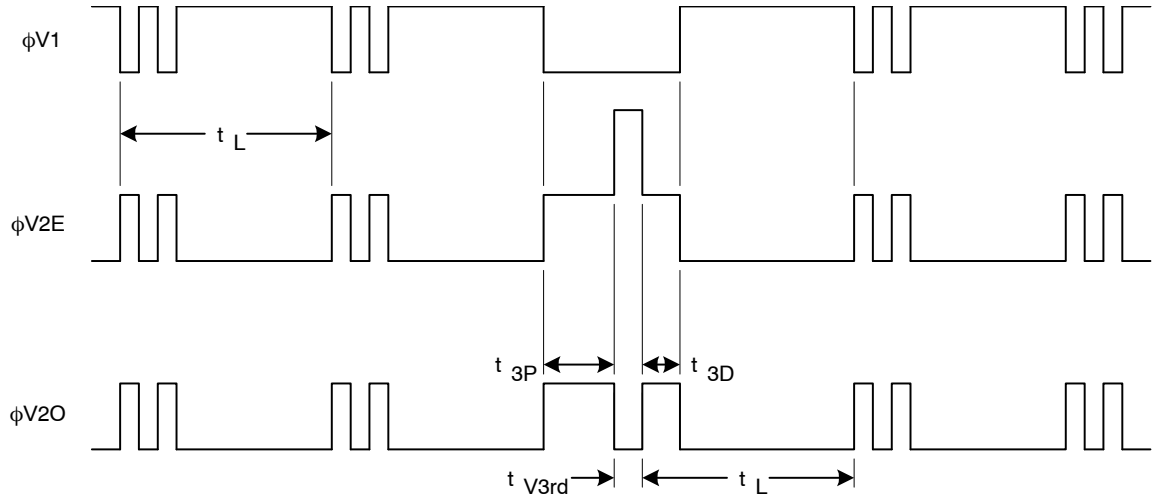


Figure 16. Interlaced Frame Timing − Frame Integration Mode − Even Field Readout

Interlaced Frame Timing − Frame Integration Mode − Odd Field Readout

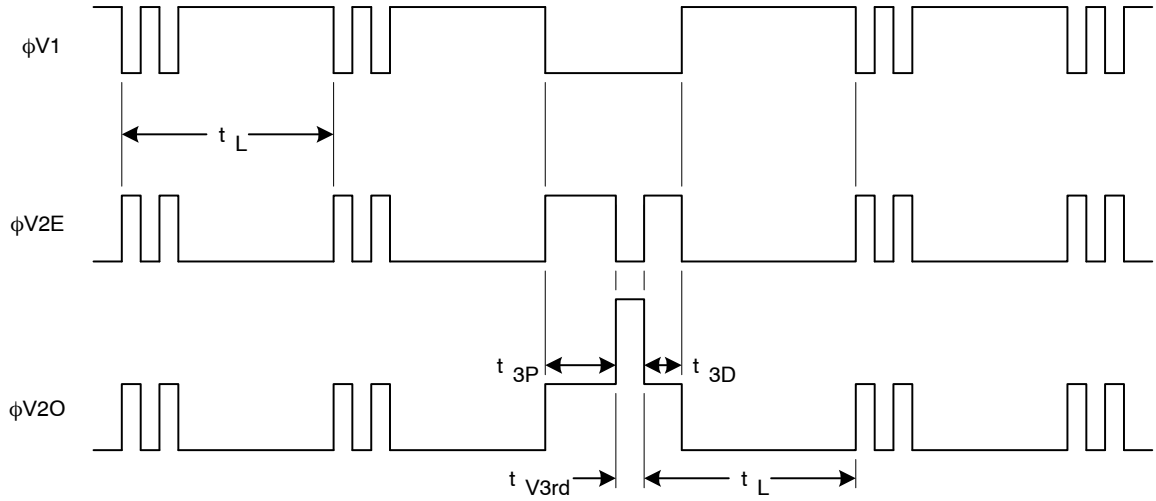


Figure 17. Interlaced Frame Timing − Frame Integration Mode − Odd Field Readout

Line Timing

Progressive Line Timing

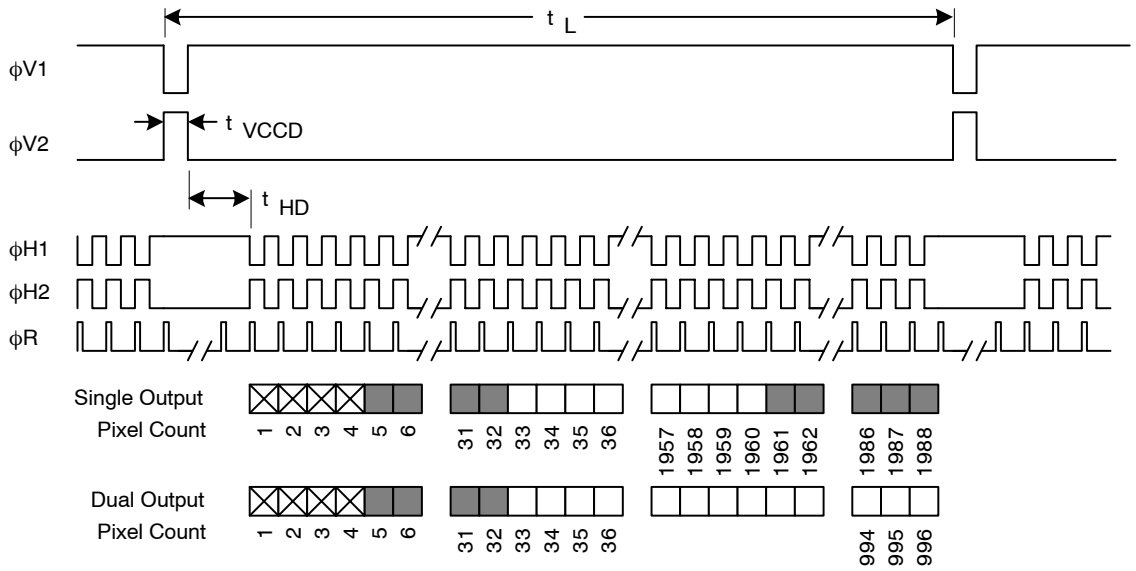


Figure 18. Progressive Line Timing

Interlaced Line Timing and Line Timing for Vertical Binning by Two

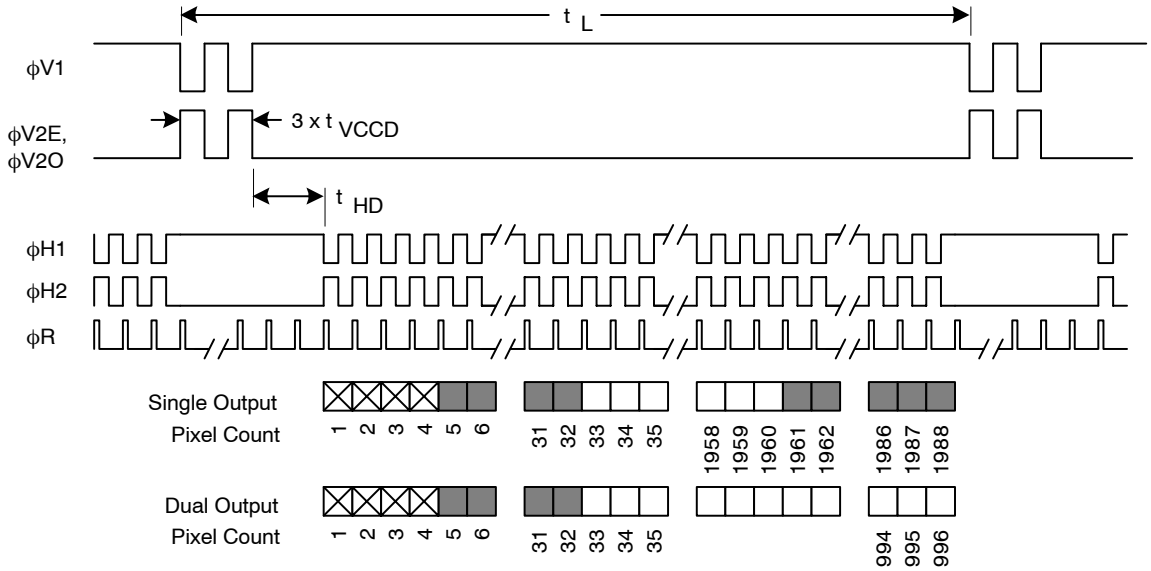


Figure 19. Interlaced Line Timing and Line Timing for Vertical Binning by Two

Electronic Shutter Timing

Electronic Shutter Line Timing

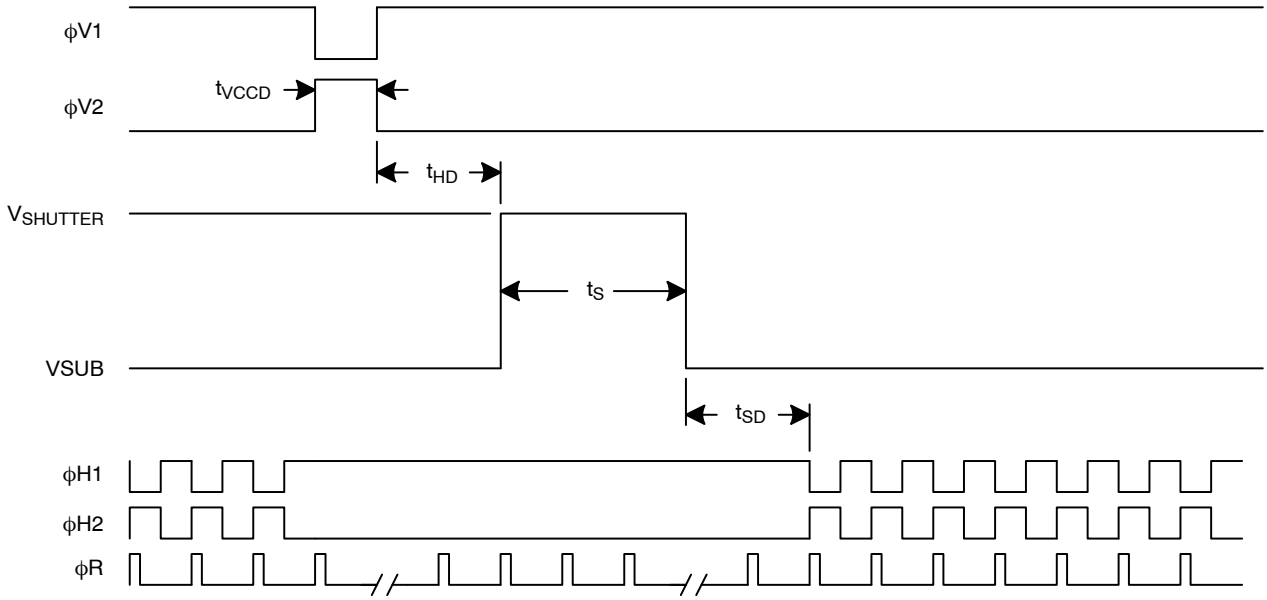


Figure 20. Electronic Shutter Line Timing

Electronic Shutter − Integration Time Definition

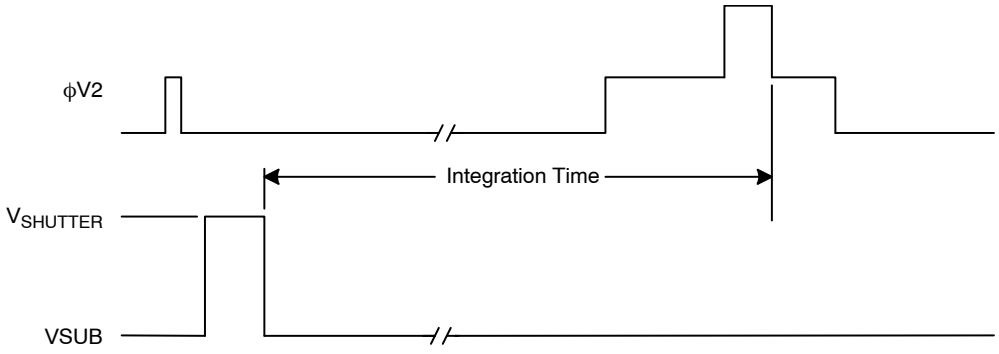


Figure 21. Integration Time Definition

STORAGE AND HANDLING

Table 18. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Unit	Notes
Storage Temperature	T_{ST}	−55	80	°C	1
Humidity	RH	5	90	%	2

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

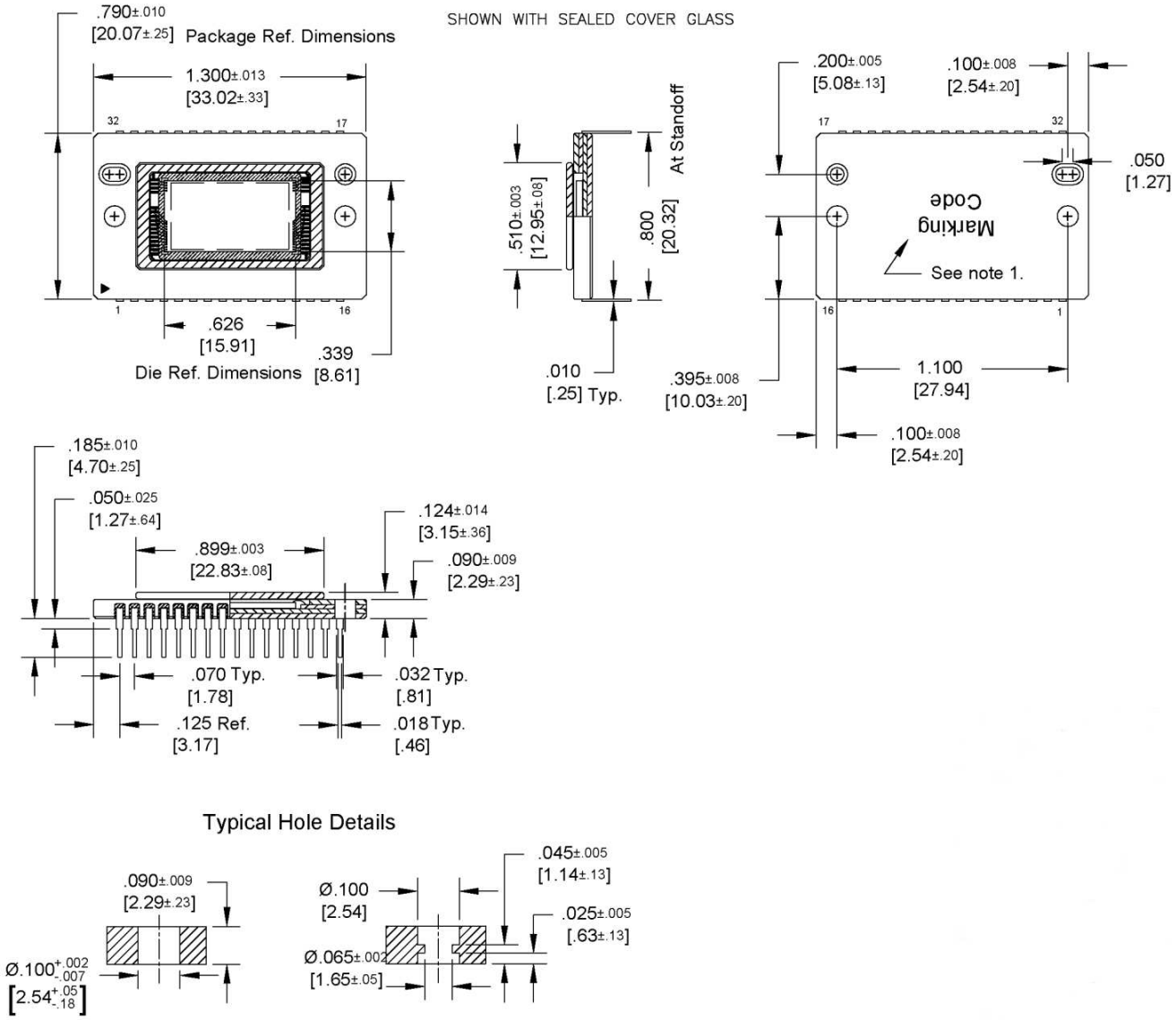
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL DRAWINGS

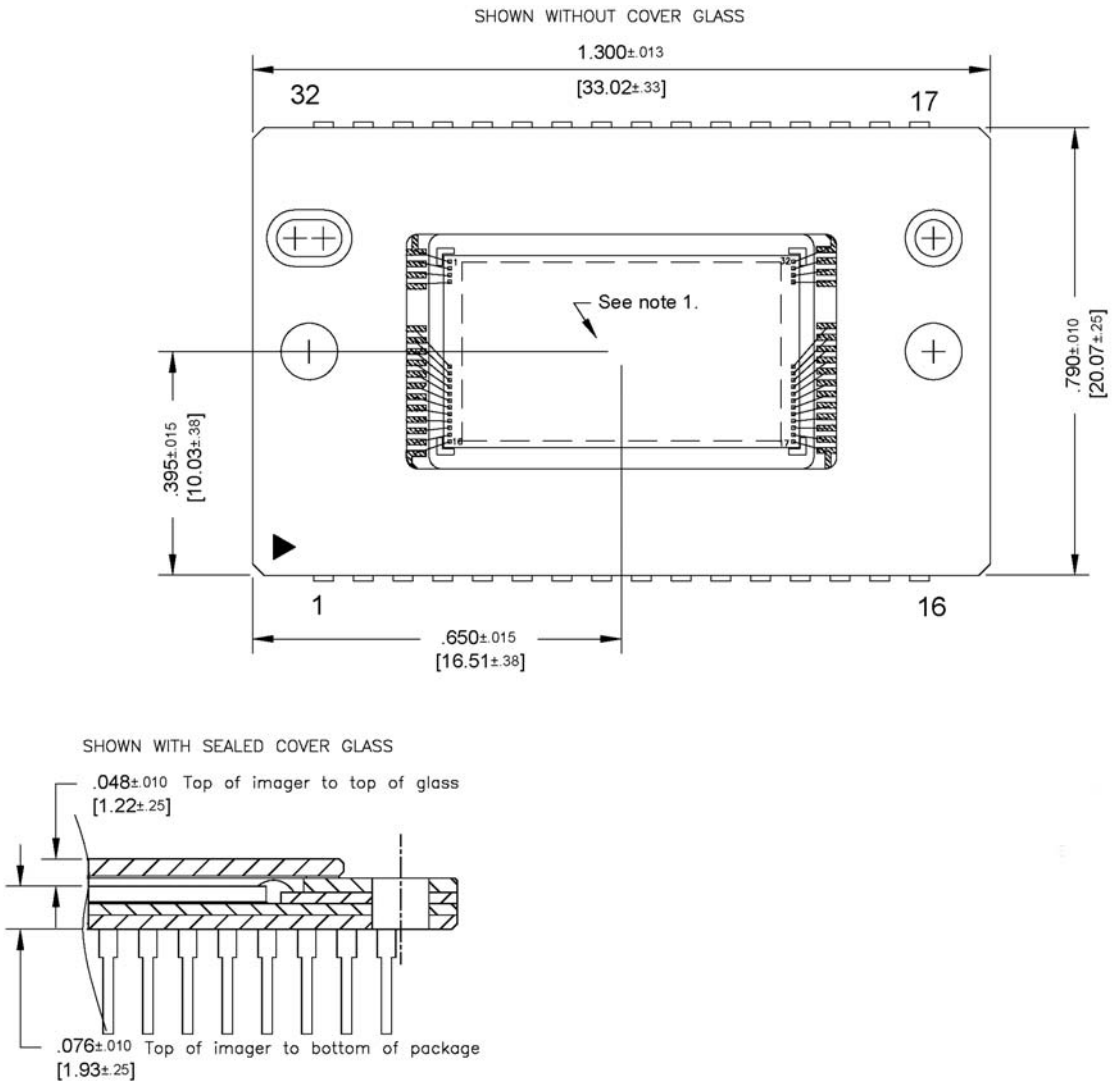
Completed Assembly



Notes:

1. See Ordering Information for marking code.
2. Cover glass is manually placed and visually aligned over die − location accuracy is not guaranteed.

Figure 22. Completed Assembly (1 of 2)



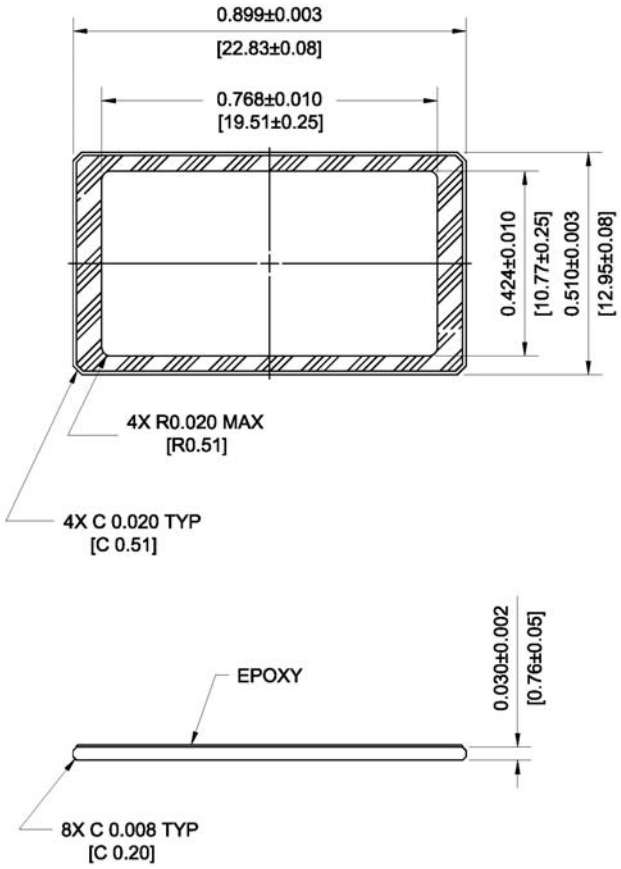
Notes:

1. Center of image is nominally coincident with the center of the package.
2. Die is aligned within ±2 degree of any package cavity edge.

Figure 23. Completed Assembly (2 of 2)

Cover Glass

Clear Cover Glass

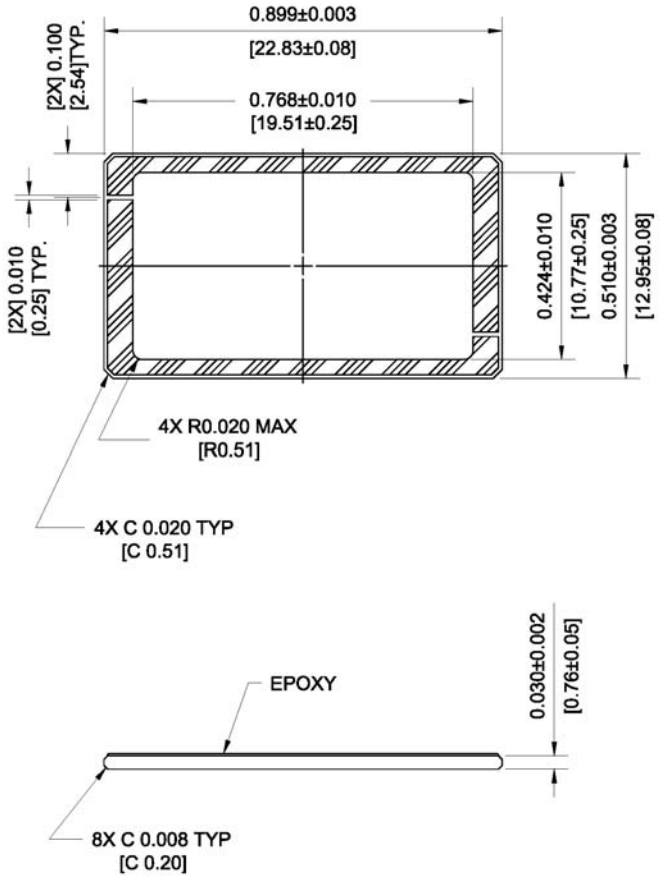


Notes:

1. Cover Glass Material: Schott D236T eco or equivalent
2. Dust/Scratch: 5 microns maximum

Figure 24. Clear Cover Glass Drawing

Quartz Cover Glass with AR Coatings



Notes:

1. Cover Glass Material: SK1300 or equivalent
2. Dust/Scratch: 10 microns maximum
3. MAR Coat Each Side:
   340 nm − 360 nm: Reflectance ≤ 0.5%
   520 nm − 550 nm: Reflectance ≤ 4%

Figure 25. Quartz Cover Glass with AR Coating Drawing