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Freescale Semiconductor
Users Guide

Documentation Number: KT34712UG
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Using the 3.0 A 1.0 MHz Fully Integrated DDR Switch-Mode Power Supply (KIT34712EPEVBE)

1 Introduction

This User's Guide will help the designer get better acquainted with the 34712 IC and Evaluation board. It contains a procedure to configure each block of the 34712 in a practical way, which is based on a working Evaluation Board designed by Freescale (KIT34712EPEVBE).

2 34712 Specification

The 34712 is a highly integrated, space-efficient, low cost, single synchronous buck-switching regulator with integrated N-channel power MOSFETs. It is a high performance point-of-load (PoL) power supply with the ability to track an external reference voltage. Its high efficient 3.0 A sink and source capability combined with its voltage tracking/sequencing ability and tight output regulation, makes it ideal to provide the termination voltage (V_{TT}) for modern data buses such as Double-Data-Rate (DDR) memory buses. It also provides a buffered output reference voltage (V_{REF}) to the memory chipset

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3 Application Diagram

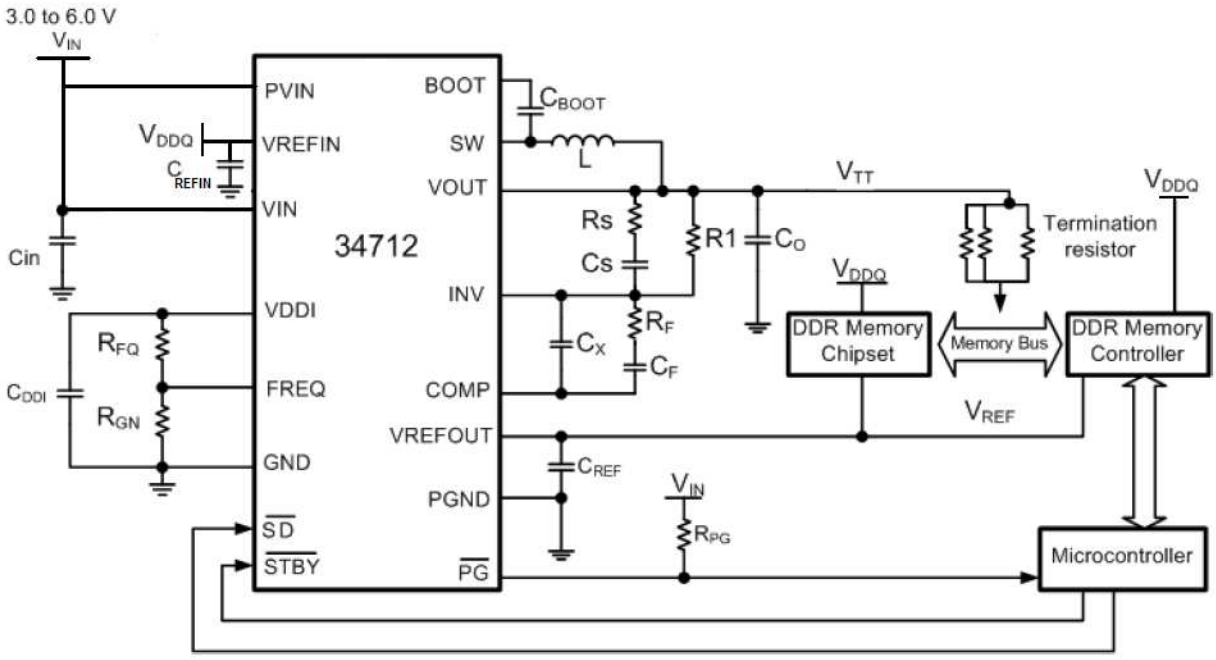

Figure 1. Application diagram for 34712

4 Board's Specifications

The Board was designed to have an operating range defined by:

P_{VIN_MIN} = 3.0 V P_{VIN_MAX} = 6.0 V

V_{OUT_MIN} = 0.7 V V_{OUT_MAX} = 1.35 V

I_{OUT_MIN} = -3.0A I_{OUT_MAX} = 3A

5 Component Selection for 34712 Eval Board

5.1 I/O Parameters:

V_{IN} = 3.3V

P_{VIN} = V_{REFIN} = VDDQ =1.5 V (DDR III Standard)

V_O =V_{TT} = 0.750 V

I_O = 3 A

FSW = 1 MHz

5.2 Configuring the Output Voltage:

The output voltage is given by the equation:

$$V_{TT} = \frac{V_{REFIN}}{2}$$

5.3 Switching Frequency Configuration

The switching frequency will have a default value of 1.0 MHz by connecting the FREQ terminal to the GND terminal. If the smallest frequency value of 200 KHz is desired, then connect the FREQ terminal to VDDI. To program the switching frequency to another value, an external resistor divider will be connected to the FREQ terminal to achieve the voltages given by the Frequency Selection Table.

Frequency Khz	Voltage applied to pin FREQ [V]
200	2.341 – 2.500
253	2.185 - 2.340
307	2.029 - 2.184
360	1.873 - 2.028
413	1.717 – 1.872
466	1.561 – 1.716
520	1.405 - 1.560
573	1.249 - 1.404
627	1.093 - 1.248
680	0.936 - 1.092
733	0.781 - 0.936
787	0.625 - 0.780
840	0.469 - 0.624
893	0.313 - 0.468
947	0.157 - 0.312
1000	0.000 - 0.156

Table 1. Frequency Selection Table

For the EVB the frequency was set to 1 MHz connecting the FREQ terminal directly to GND.

5.4 Selecting Inductor

Inductor calculation is as follows:

$$L = D'_{MAX} * T * \frac{(Vo + I_0 * (Rds(on)\_ls + r\_w))}{\Delta I_o}$$

$D'_{MAX} = 1 - \frac{Vo}{Vin\_\max} = 1 - \frac{0.75}{6.0} = 0.88$ Maximum Off time percentage

$T = 1\mu s$ Switching period

$Rds(on)\_ls = 45m\Omega$ Drain – to – source resistance of FET

$r\_w = 10m\Omega$ Winding resistance of Inductor

$\Delta Io = 0.4 * Io$ Output current ripple

$L = 0.67\mu H$

We have selected $L = 1.5\mu H$ to allow some operating margin.

5.5 Input Capacitors

Input capacitor selection should be based on the current ripple allowed on the input line. The input capacitor should provide the ripple current generated during the inductor charge time. This ripple is dependent on the output current sourced by 34712 so that:

$$I_{RMS} = Io\sqrt{d(1-d)}$$

Where:

I_{RMS} is the RMS value of the input capacitor current

I_0 is the output current

d= Vo/Vin is the duty cycle

For a buck converter, I_{RMS} has its maximum at Vin = 2Vo

Since

$$I_{RMS\_MAX} = \sqrt{\frac{P_{MAX}}{ESR}}$$

Where PMAX is the maximum power dissipation of the capacitor and is a constant based on physical size (generally given in the datasheets under the heading AC power dissipation). We derive that the lower the ESR, the higher would be the ripple current capability. In other words, a low ESR capacitor (i.e., with high ripple current capability) can withstand high ripple current levels without overheating.

Therefore, for greater efficiency and because the overall voltage ripple on the input line also depends on the input capacitor ESR, we recommend using low ESR capacitors.

$$Cin_{MIN} = \frac{0.5 * L * (I_{RMS})^2}{\Delta Vo * Vin}$$

For a ΔVo = 0.5*Vin, Then Cin_{MIN} = 30.4µF

On the EVB there was selected an input capacitor of 300µF to assure less input voltage ripple and have better regulation.

5.6 Selecting the Output Filter Capacitor

For the output capacitor, the following considerations are most important and not the actual Farad value: the physical size, the ESR of the capacitor, and the voltage rating.

Calculate the minimum output capacitor using the following formula:

$$C_0 = \frac{\Delta I_0}{8 \cdot F_{SW} \cdot \Delta V_0}$$

However, a more significative calculation is to include the transient response in order to calculate the real minimum capacitor value to assure a good performance.

Transient Response percentage	TR_% = 3%
Maximum Transient Voltage	TR_V_dip = Vo*TR_% = 0.75*0.03 = 0.0225V
Maximum current step	$\Delta Io\_step = \frac{(Vin\_\min - Vo) * D\_\max}{Fsw * L}$ =1.35A
Inductor Current rise time	$dt\_I\_rise = \frac{T * Io}{\Delta Io\_step}$ = 2.2µs
	$Co = \frac{Io * dt\_I\_rise}{TR\_V\_dip} = 296.3\mu F$

To find the Maximum allowed ESR, the following formula was used:

$$ESR_{\max} = \frac{\Delta Vo * Fsw * L}{Vo(1 - D\min)} = 3m\Omega$$

As a DDR specification, the ESR should be around 2 mΩ, to achieve this, an array of capacitors in parallel where used, with 3 Low ESR Ceramic capacitor of 100 µF.

5.7 Bootstrap Capacitor

Freescale recommends a 0.1 µF for this capacitor.

5.8 Compensation Network

1. Choose a value for R1 = 20KΩ
2. Using a Crossover frequency of 50 kHz, set the Zero pole frequency to Fcross/10

$$F_{P0} = \frac{1}{10} Fcross = \frac{1}{2\pi * R_1 C_F} = 5.0kHz$$

$$C_F = \frac{1}{2\pi * R_1 F_{PO}} = 1.45nF$$

3. Knowing the LC frequency, the Frequency of Zero 1 and Zero 2 in the compensation network are equal to F_{LC}

$$F_{LC} = \frac{1}{2\pi\sqrt{L\ C_O}} = 7.5kHz = F_{Z1} = F_{Z2} \qquad F_{Z1} = \frac{1}{2\pi * R_F C_F} \qquad F_{Z2} = \frac{1}{2\pi * R_1 C_S}$$

$$R_F = \frac{1}{2\pi * C_F F_{Z1}} = 14.66K\Omega \qquad C_S = \frac{1}{2\pi * R_1 F_{Z2}} = 1.06nF$$

4. Calculate Rs by placing the first pole at the ESR zero frequency:

$$F_{ESR} = \frac{1}{2\pi * C_o * ESR} = 265.2kHz = F_{P1} \qquad F_{P1} = \frac{1}{2\pi * R_S C_S}$$

$$R_S = \frac{1}{2\pi * F_{P1} C_S} = 570\Omega$$

$$F_{P2} = \frac{1}{2\pi * R_F \dfrac{C_F Cx}{C_F + C_x}} = 500kHz$$

5. Set the second pole at ten times the Crossover Frequency to achieve a faster response and a proper phase margin.

$$F_{P2} = \frac{1}{2\pi * R_F \frac{C_F Cx}{C_F + C_x}} = 500kHz \qquad C_X = \frac{C_F}{2\pi * R_F C_F F_{P2} - 1} = 24\,pF$$

The Actual values used on the EVB might change due to precision of L and C components thus, on EVB where selected as follows.

C_F = 1.9 nf R_F = 15 kΩ Cs = 1 nf Rs = 300 Ω Cx = 20 pf

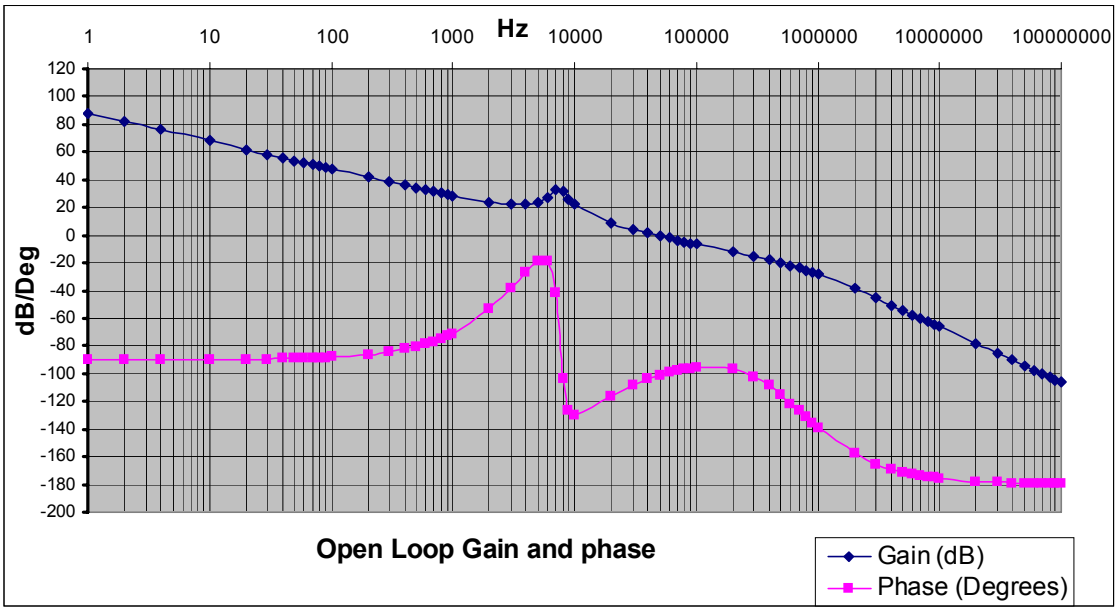

Figure 2. Compensated Open Loop Bode Plot

5.9 EVB Schematic Design

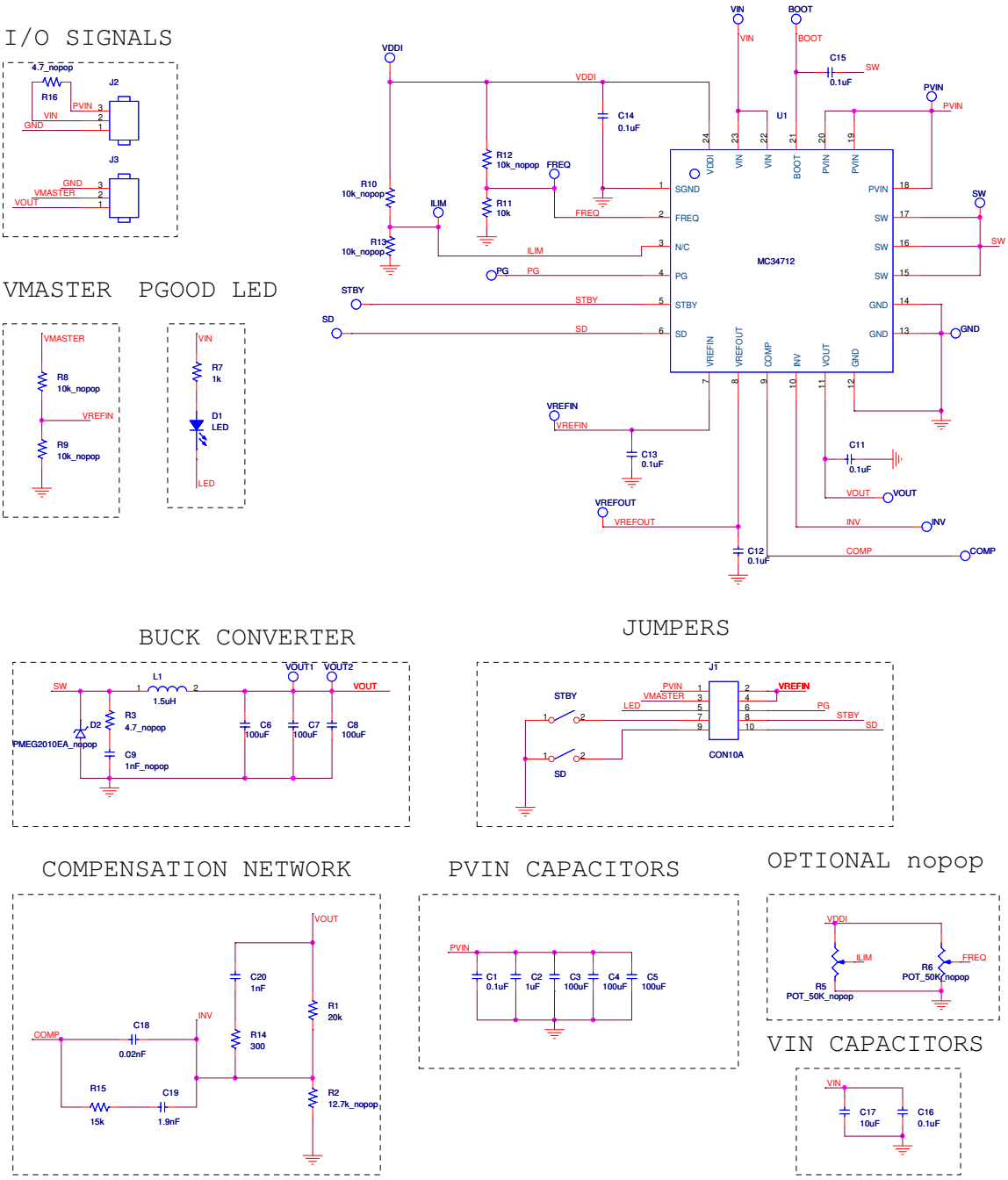

Figure 3. 34712 Schematic

6 Layout Design

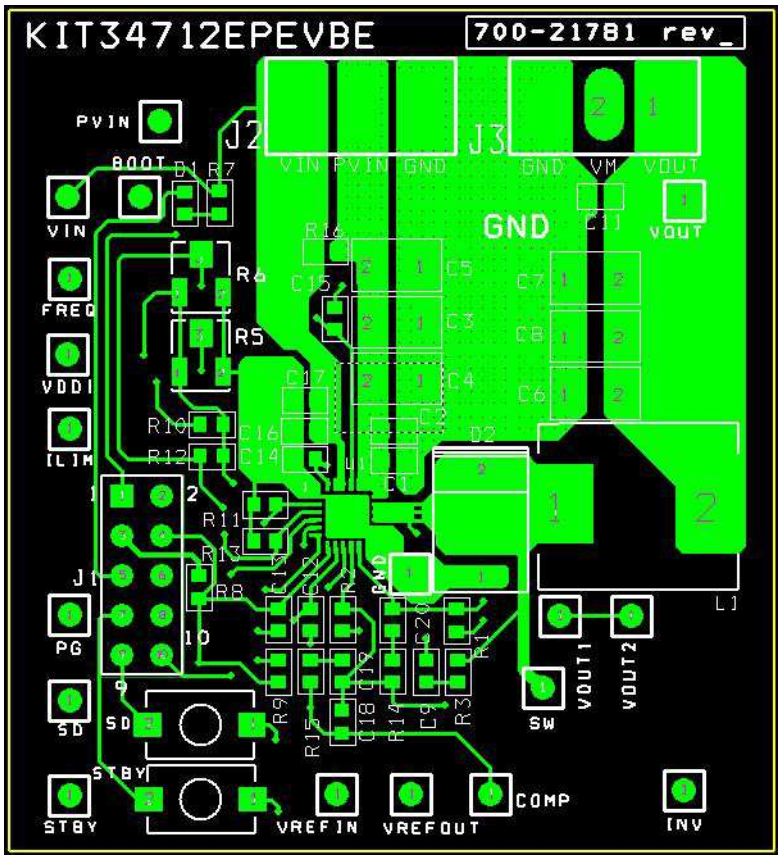

Figure 4. PCB Layout Top View

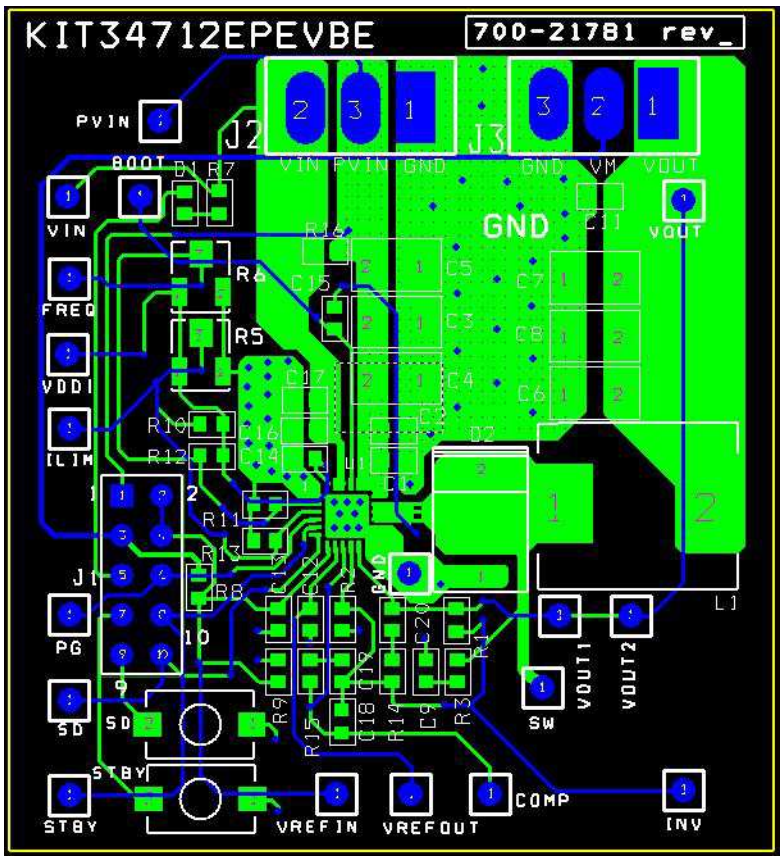

Figure 5. PCB Layout Inner Layer

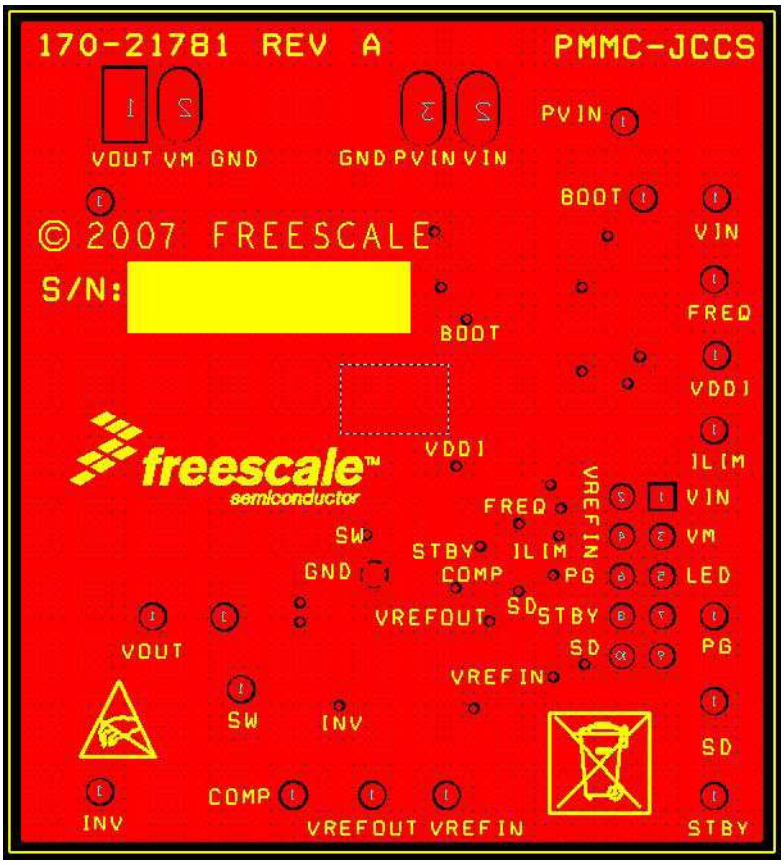

Figure 6. PCB Layout Bottom Layer

6.1 PCB Layout Recommendations

- Place decoupling capacitors as close as possible to their corresponding pad(s)
- Try to place all components on just one Layer
- Do not place a Ground Plane on component and routing side
- Create a Ground plane layer and tie it to ground signals with vias
- To effectively transfer heat from the center thermal pad on the top layer to the ground plane, vias need to be used in the center pad. Use 5 to 9 vias spaced evenly with a finished diameter of 0.3mm.
- Place Test vias as close as possible to the IC to ensure a good measurement value
- P_{VIN}, V_{IN}, V_{OUT} signals have to be tracked with a widely and straight copper area
- Never trace the Feedback signal in parallel to the SW signal
- Ensure the SW Inductor is placed as close as possible to its pads
- SW track has to be as thin and short as possible
- Make sure the I/O connectors are capable to manage the Load current

Note: Freescale does not recommend connecting the PGND pins to the thermal pad. The thermal pad is connected to the signal ground and should not be used to make the connection from the PGND pins to the ground plane. Doing so can cause ground bounce on the signal ground from the high di/dt switch current and parasitic trace inductance.

6.2 Bill of Materials

Item	Quantity	Reference	Value	Description	Footprint
1	16	VREFOUT, VREFIN, VOUT, VIN, VDDI, SW, STBY, SD, PVIN, PG, INV, ILIM, GND, FREQ, COMP, BOOT	not populated	PC test point miniature SMT	TP1
2	1	C2	1µF	Cap Cer 1.0µF 6.3V 10% X5R 0603	SM/C_0603
3	6	C3, C4, C5, C6, C7, C8	100µF	Cap Cer 100µF 10% X5R 1210	SM/C_1210
4	1	C9	not populated		
5	7	C1, C11, C12, C13 , C14 C15, C16	0.1µF	Cap Cer 0.1µF 50V 10% X7R 0603	SM/C_0603
6	1	C17	10µF	Cap Cer 10µF 6.3V 20% X5R 0603	SM/C_0603
7	1	C18	20pF	Cap Cer 20pF50V 5% C0G 0603	SM/C_0603
8	1	C19	1.8nF	Cap Cer 1800pF 50V 5% C0G 0603	SM/C_0603
9	1	C20	1nF	Cap Cer 1000pF 25V 5% C0G CC0603	SM/C_0603
10	1	D1	LED	LED Green 0603	SM/C_0603
11	1	D2	not populated		SMC
12	1	J1	Pin Header (2X5)	HDR 2X5 TH 100MIL CTR 330H AU	0.1” (2.54mm)
13	2	100mils jumpers	Jumpers		100 mils
14	1	J2	not populated		
15	1	J3	not populated		
16	1	L1	1.5µH	Inductor Power 1.5µH 7.0A SMD	B82464G
17	1	R1	20k	Res MPF 20k ohm 1/10W 5% 0603	SM/C_0603
18	1	R2	12.7k	Res 12.7k ohm 1/10W 1% 0603 SMD	SM/C_0603
19	2	R3,R16	not populated		SM/C_0603
20	2	R5,R6	not populated		TRIMPOT
21	1	R7	1k	Res MF 1.0k 1/10W 1%0603	SM/C_0603

22	2	R12,R13	not populated		SM/C_0603
23	3	R8, R9, R10	10k	Res MF 10.0k 1/10W 1% 0603	SM/C_0603
24	1	R11	10k	Res MF 10.0k 1/10W 1% 0603	SM/C_0603
25	1	R14	300	Res MF 300 Ohm 1/10W 5% 0603	SM/C_0603
26	1	R15	15k	Res MF 15.0k 1/10W 1% 0603	SM/C_0603
27	1	SD	Push_button	Switch tact mini 200GF SLV GWING	
28	1	U1	MC34712		QFN_24
29	1	STBY	not populated	Switch tact mini 200GF SLV GWING	

Notes: Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

7 Conclusion

With this User's Guide, the user will be perfectly capable of configuring the 34712 as power supply for DDR memory chips as well as other devices that can make use of some of the capabilities the 34712 offers. The board is fully configured to work at any desirable reference voltage within 0 and 2.5 V. However, it is widely recommended to calculate all components for the specific application situation in order to assure a better efficiency and stability of the IC

8 References

- MC34712 Datasheet, "3 A, 1MHz Fully Integrated, Single Switch-mode, Power Supply"; Freescale semiconductor, Inc.
- Similar network compensation calculations are available in Application Note "AN1989 MC34701 and MC34702 Component Selection Guide", Freescale Semiconductor, Inc.
- Sanjaya Maniktala, "*Switching Power Supplies A to Z*", Newnes, 2006.

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