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MMA955xL Intelligent Motion-Sensing Platform

Devices Supported:

MMA9550L
MMA9551L
MMA9552L
MMA9553L

Document Number: MMA955xLRM
Rev. 0, 06/2011

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MMA955xLRM
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Chapter 1 About This Document

1.1 Overview

1.1.1 Purpose

This reference manual describes the features, architecture and programming model of the MMA955xL, an intelligent, three-axis accelerometer.

1.1.2 Audience

This document is primarily for system architects and software application developers who are using or considering use of the MMA955xL in a system.

1.2 Conventions

This document uses the following notational conventions:

cleared/set	When a bit takes the value 0, it is said to be cleared; when it takes a value of 1, it is said to be set.
MNEMONICS	In text, instruction mnemonics are shown in uppercase.
`mnemonics`	In code and tables, instruction mnemonics are shown in lowercase.
italics	Italics indicate variable command parameters. Book titles also are italicized.
0x0	Prefix to denote a hexadecimal number
0b0	Prefix to denote a binary number
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields or ranges appear in brackets. For example, RAMBAR[BA] identifies the base address field in the RAM base-address register.
nibble	A 4-bit data unit
byte	An 8-bit data unit
word	A 16-bit data unit
longword	A 32-bit data unit
x	In some contexts, such as signal encodings, x indicates a “do not care.”
n	Used to express an undefined numerical value.
~	NOT logical operator
&	AND logical operator

|	OR logical operator
||	Field concatenation operator
$\overline{\text{OVERBAR}}$	Indicates that a signal is active-low.

Register Figure Conventions

This document uses the following conventions for the register reset values:

—	The bit is undefined at reset.
u	The bit is unaffected by reset.
[*signal_name*]	Reset value is determined by the polarity of the indicated signal.

The following register fields are used:

R 0 W	Indicates a reserved bit field in a memory-mapped register. These bits are always read as 0.
R 1 W	Indicates a reserved bit field in a memory-mapped register. These bits are always read as 1.
R FIELDNAME W	Indicates a read/write bit.
R FIELDNAME W	Indicates a read-only bit field in a memory-mapped register.
R W FIELDNAME	Indicates a write-only bit field in a memory-mapped register.
R FIELDNAME W w1c	Write 1 to clear: indicates that writing a 1 to this bit field clears it.
R 0 W FIELDNAME	Indicates a self-clearing bit.

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7. *ITU-T X.25 Recommendation: Interface between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE) for terminals operating in the packet mode and connected to public data networks by dedicated circuit,* available at http://www.itu.int/publications/index.html.
8. *ITU-T T.30 Recommendation: Procedures for document facsimile transmission in the general switched telephone network,* available at http://www.itu.int/publications/index.html.

Chapter 2 Introduction

The MMA955xL three-axis accelerometer is a member of Freescale's Xtrinsic family of intelligent sensor platforms. This device incorporates dedicated accelerometer MEMS transducers, signal conditioning, data conversion and a 32-bit, programmable microcontroller.

This unique blend transforms Freescale's MMA955xL into an intelligent, high-precision motion-sensing platform able to manage multiple sensor inputs and make system-level decisions required for sophisticated applications such as gesture recognition, pedometer functionality and eCompass tilt compensation and calibration.

The MMA955xL is programmed and configured with CodeWarrior Development Studio software. This integrated-design environment enables customers to quickly and easily shape and implement custom algorithms and features to exactly match their application needs.

Using its master I^2C module, the MMA955xL can manage secondary sensors such as pressure sensors, magnetometers or gyroscopes. This allows sensor initialization, calibration, data compensation and computation functions to be off-loaded from the system application processor. Multiple sensor inputs can be easily consolidated by the MMA955xL which acts as an intelligent sensing hub and highly configurable decision engine. Total system power consumption is significantly reduced as the application processor stays powered down until absolutely needed.

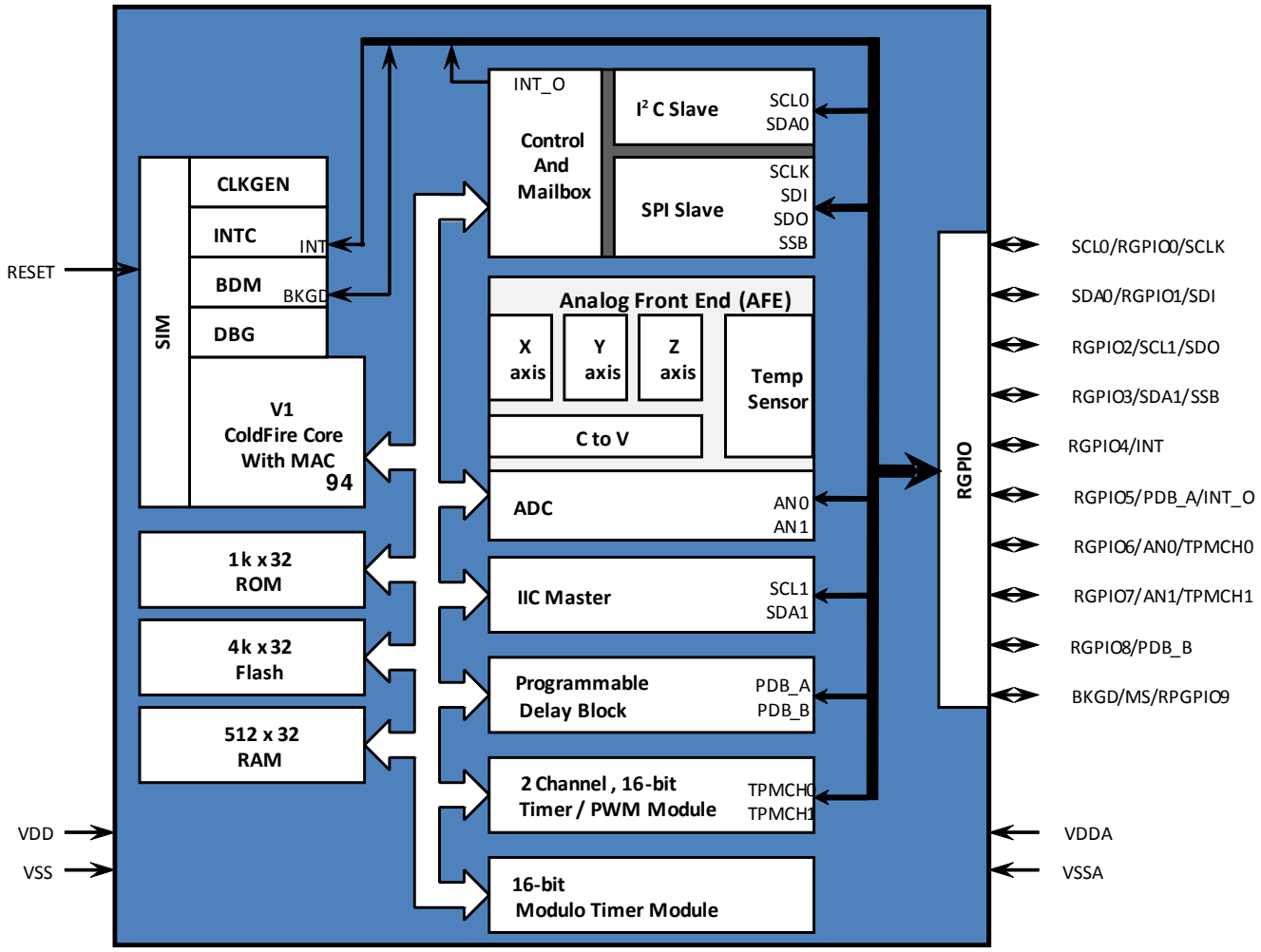

Figure 2-1. Block Diagram of the MMA955xL

2.1 Hardware Features

- Three accelerometer operating ranges:
  - ±2g: Suits most user-interaction (mouse) motions and free fall
  - ±4g: Covers most regular human dynamics (walking, jogging)
  - ±8g: Detects most abrupt activities (gaming)
- Integrated temperature sensor
- One slave SPI or I^2C interface operates up to 2 MHz dedicated to communication with host processor
- One master I^2C interface operates up to 400 kbps used to communicate with external sensors
- 10, 12, 14 and 16-bit ADC trimmed data formats available.
- 1.8V Supply Voltage
- 32-bit ColdFire V1 CPU
- Extensive set of power management features and low power modes.

- Single Wire Background Debug Mode (BDM) pin interface
- 16 KB Flash Memory
- 2 KB random access memory
- ROM-based flash controller and slave port command line interpreter
- Two channel timer with input capture, output capture or edge-aligned PWM
- Programmable delay block for scheduling events relative to start of frame
- Modulo timer for scheduling periodic events

2.2 Software Features

This device may be programmed to provide any of the following:

- Orientation Detection (Portrait/Landscape)
- High-g/Low-g Threshold Detection
- Pulse Detection (Single, Double and Directional Tap)
- Auto Wake/Sleep
- Linear and Rotational Freefall
- Flick Detection
- Embedded Smart FIFO
- Power Management
- Pedometer
- Shock, Vibration and Sudden Motion Detection
- Tilt Compensated eCompass and Calibration (soft iron and hard iron)

The association of a high-performance accelerometer with a powerful, embedded ColdFire V1 MCU core gives the possibility to grow and customize this list in an unprecedented way.

2.3 Typical Applications

This low-power intelligent sensor is optimized for use in portable and mobile consumer products such as:

- Mobile phones/PMP/PDA/digital cameras
  - — Orientation Detection (Portrait/Landscape)
  - — Image Stability
  - — Tilt control enabled with higher resolution
  - — Gesture Recognition
  - — Tap to Control
  - — Auto Wake/Sleep for low power consumption
- Smartbooks/eReaders/Netbooks/Laptops
  - — Anti-theft
  - — Freefall Detection for Hard Disk Drives
  - — Orientation Detection

  - Tap Detection
- Pedometers
- Gaming and Toys
- eCompass Tilt Compensation
- Personal Navigation Devices (PNDs)
- Public Transportation Ticketing Systems
- Activity Monitoring in Medical Applications
- Security
  - Anti-theft
  - Shock Detection
  - Tilt
- Fleet Monitoring, Tracking
  - Dead Reckoning
  - System Auto Wake-up on Movement
  - Detection
  - Shock Recording
  - Anti-theft
- Power Tools and Small Appliances
  - Tilt
  - Safety Shut-off

Chapter 3 Pins and Connections

3.1 Package Pinout

The package pinout definition for this device is designed as a superset of functions found on competitive devices, as well as other Freescale offerings. All pins on the device are utilized and many have multiple possible uses.

The following sections describe the pinout. Users may select from multiple pin functions via the SIM pin mux-control registers.

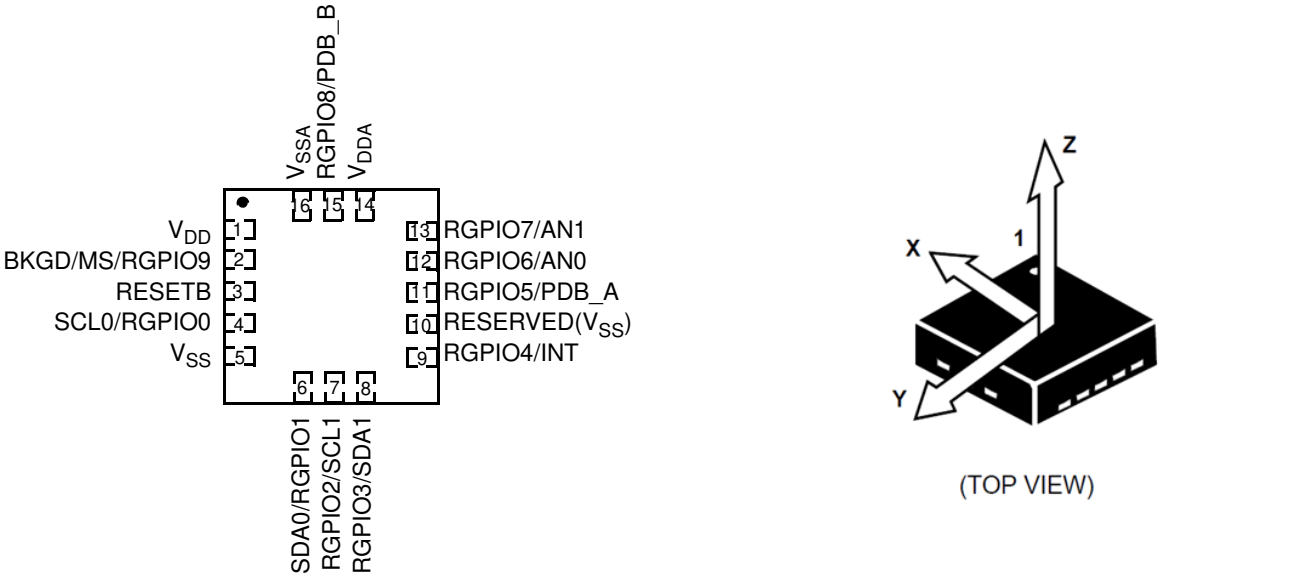

Figure 3-1. Device Pinout and Coordinate System

3.1.1 Pin Functions

Table 3-1 summarizes functional options for each of the device's pins.

Table 3-1. Pin Functions

Pin #	Pin Function #1[1]	Pin Function #2	Pin Function #3	Description
1	V_{DD}			Digital power supply
2	BKGD/MS	RGPIO9		Background debug/mode select RGPIO9
3	RESETB[2]			Active low reset
4	SCL0	RGPIO0	SCLK	Serial clock for slave I^2C/RGPIO0/Serial clock for slave SPI
5	V_{SS}			Digital ground
6	SDA0	RGPIO1	SDI	Serial data for slave I^2C/RGPIO1/SPI serial data input
7	RGPIO2	SCL1	SDO	RGPIO2/Serial clock for master I^2C/SPI serial data output
8[3]	RGPIO3	SDA1	SSB	RGPIO3/Serial data for master I^2C/SPI slave select
9	RGPIO4	INT		RGPIO4/Interrupt input
10	RESERVED (Connect to V_{SS})			Must be connected to GND externally
11	RGPIO5	PDB_A	INT_O	RGPIO5/PDB_A
12	RGPIO6	AN0	TPMCH0	RGPIO6/ADC Input 0 / TPM Channel 0
13	RGPIO7	AN1	TPMCH1	RGPIO7/ADC Input 1 / TPM Channel 1
14	V_{DDA}			Analog power
15	RGPIO8	PDB_B		RGPIO8/PDB_B
16	V_{SSA}			Analog ground

1 Pin Function 1 represents the reset state of the device. Pin functions may be changed via the SIM pin mux-control registers (Section 11.7.5, "SIM Pin Mux Control Registers").

2 RESETB is an open-drain, bidirectional pin. By default, the output function is not on.

3 RGPIO3/SDA1/SSB = LOW at startup indicates that SPI should be used as slave instead of the I^2C module.

3.1.2 Sensing Direction and Output Response

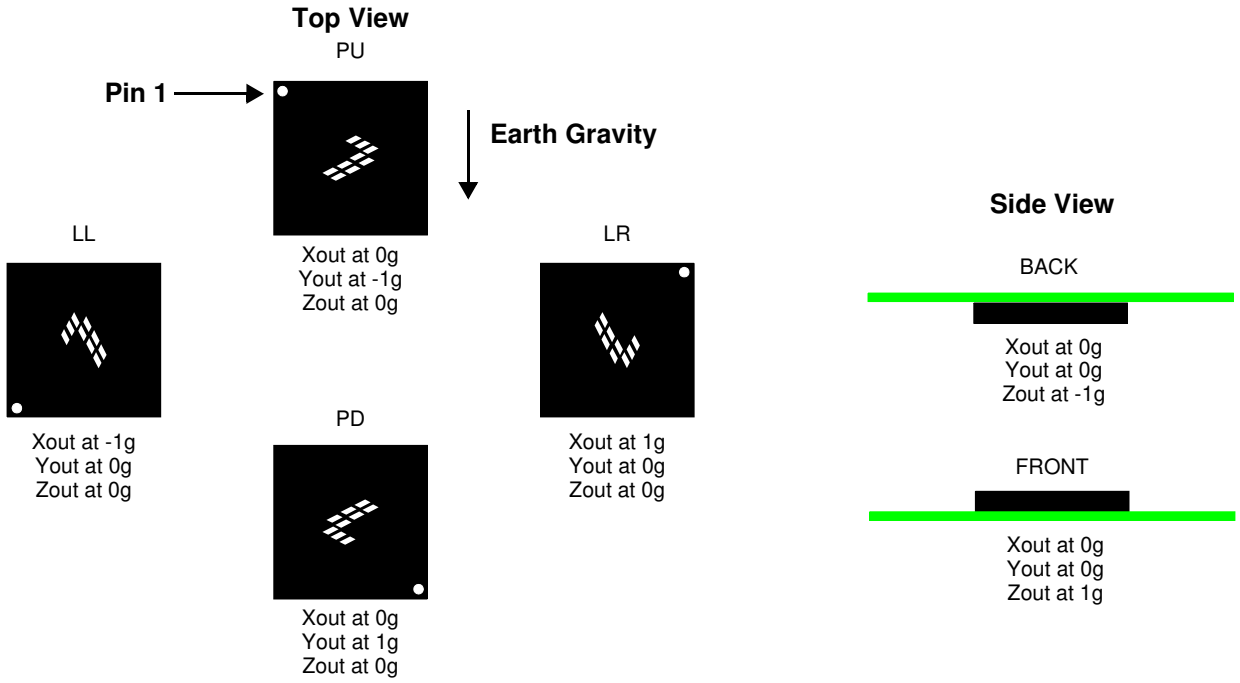

Figure 3-2. Sensing Direction and Output Response

3.2 Pin Descriptions

The following sections provide descriptions of the various pin functions available on the MMA955xL devices. Ten of the device pins are multiplexed with Rapid GPIO (RGPIO) functions. (See Chapter 15, "Rapid GPIO (RGPIO)".) The "Primary Pin Function #1" column of Table 3-1 lists the functions that are active when the device exits the reset state. The pin mux control registers in the System Integration Module (or SIM) can be used to change pin assignments for these pins after reset. (See Chapter 11, "System Integration Module (SIM)".)

3.2.1 V_{DD} and V_{SS}

These are the digital power and ground pins and must be connected to the same voltage. V_{DD} is nominally 1.8V for this device.

3.2.2 V_{DDA} and V_{SSA}

These are the analog-power and ground pins. V_{DDA} is nominally 1.8V for this device and must be filtered to remove any digital noise that may be present on the supply. V_{DDA} is usually connected to V_{DD} through an appropriate filtering network.