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# KITPF0100EPEVBE Evaluation Board

## Featuring the MMPF0100 14-Channel Configurable PMIC

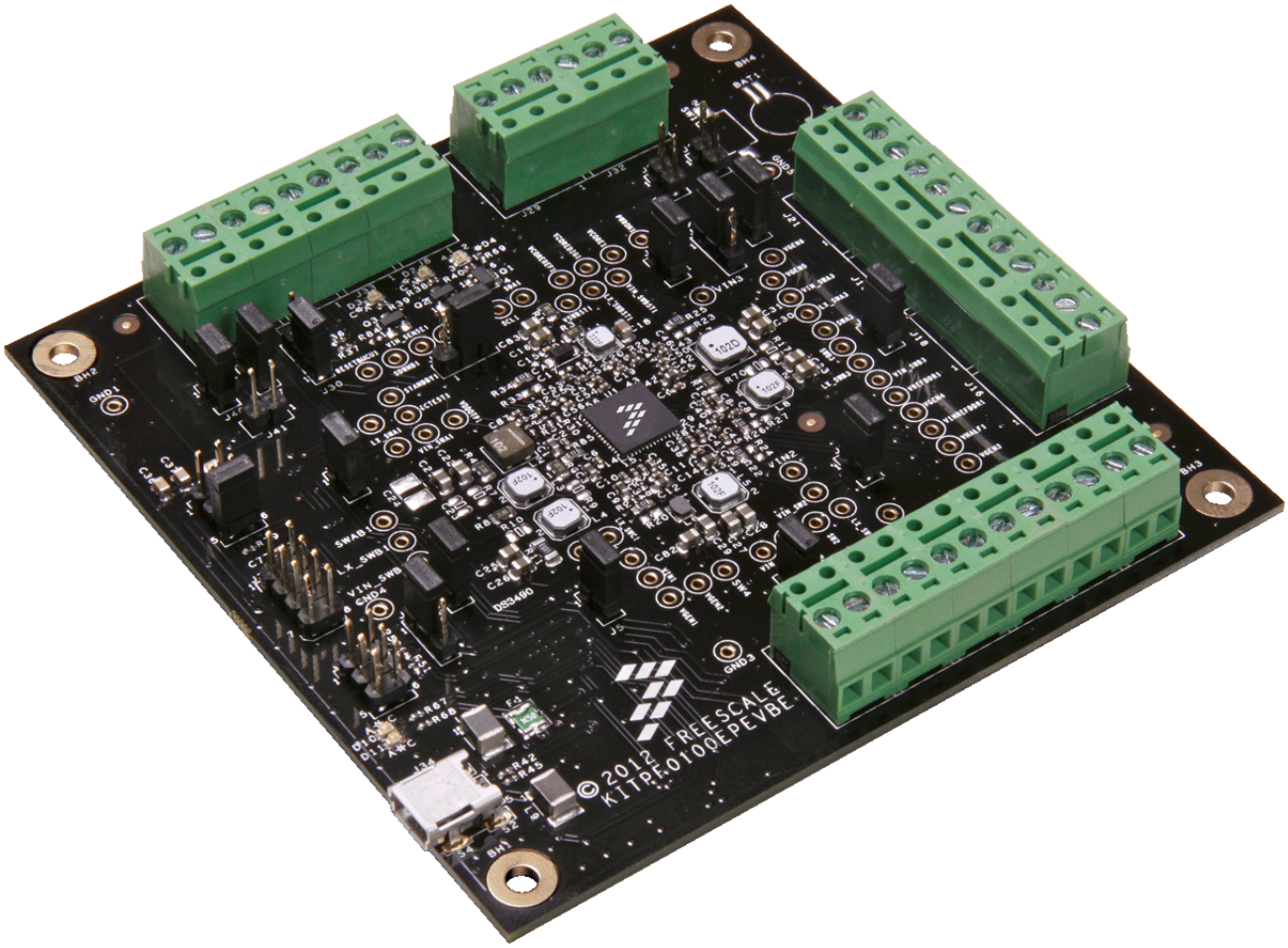


**Figure 1. KITPF0100EPEVBE Evaluation Board**

# Contents

# 1 Important Notice

Freescale provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation kit may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact Freescale sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

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# 2 Getting Started

## 2.1 Kit Contents/Packing List

- Customer evaluation board KITPF0100EPEVBE
- Warranty card and technical support brochure

# 3 Introduction

The KITPF0100EPEVBE evaluation board supports the development and testing of the PF0100 PMIC, a member of Freescale's i.MX6 family of application processors. The board provides access to all output voltage rails as well as control and signal pins through terminal block connectors. A single terminal block connector for the input power supply allows the user to supply the board with an external DC power supply to fully evaluate the performance of the device.

The KITPF0100EPEVBE comes with a non-programmed version of the PF0100 PMIC that is prepared to power up from the default sequence. However, an integrated control/fuse programming interface allows the customer to program the OTP/TBB (One Time Programmable/Try-Before-Buy) memory and also to select it as the default source for the power-up configuration. Likewise, the programming interface allows full control of the PF0100 through the $I^2C$ communication lines.

This document is intended to provide an overview of the KITPF0100EPEVBE evaluation board as well as detailed instruction for programming the PF0100 through its dedicated Graphic User Interface (GUI).

# 4 KITPF0100EPEVBE Features

- Input voltage operation range from 3.1 V to 4.5 V
- Output voltage supplies accessible through detachable terminal blocks
  - Four to six independent buck converters
  - One 5.0 V boost regulator
  - Six general purpose LDO regulators
  - One DDR memory termination voltage reference
  - One VSRTC supply
- Coin cell support for "Try-Before-Buy" (TBB) mode
- On/off push button support
- Hardware configuration flexibility through various jumper headers and resistors
- Integrated USB to $I^2C$ programming interface for full control/configuration
  - Onboard OTP programming supply and control
  - Onboard PMIC control through the $I^2C$ register map
  - Fully featured programmer through J36 for external device control/programming
- On board connectors for interfacing with future evaluation/debug tools
- Compact form factor (4 x 4 $in^2$)

# 5 MMPF0100 Features

The PF0100 Power Management Integrated Circuit (PMIC) provides a highly programmable/ configurable architecture with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF0100 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications.

- Four to six buck converters, depending on configuration
  - Single/Dual phase/ parallel options
  - DDR termination tracking mode option
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (One Time Programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- Individually programmable ON, OFF, and Standby modes

Freescale analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow which integrates precision analog, power functions, and dense CMOS logic on a single cost-effective die.

## 5.1 MC9S08JM60 Features

The KITPF0100EPEVBE implements a Freescale MC9S08JM60 low-cost, high-performance 8-bit HCS08 microcontroller to interface via USB to I2C to control the main PMIC.

- 8-bit HCS08 Central Processing Unit (CPU)
  - Up to 24 MHz internal bus (48 MHz HCS08 core) frequency offering 2.7 to 5.5 V across temperature range of -40 to +85 °C
  - Support for up to 32 peripheral interrupt/reset sources
- On-Chip Memory
  - Up to 60 K flash read/program/erase over full operating voltage and temperature
  - Up to 4 K RAM
  - 256 Byte USB RAM

# 6 Hardware/Software Requirements

## 6.1 Hardware Requirements

- Power supply:
  - Output voltage range from 3.1 V to 4.5 V
  - Current capability from 3 to 5 A (current requirement is dependent on output loading)
- Supply to board connection cables (capable of withstanding up to 5.0 A current)
- USB (male) to mini USB (male) communication cable.
- USB-enabled computer.

## 6.2 Software Requirements

- Windows XP or Windows 7 operating system

# 7 Hardware Configuration

Connect the power supply and the USB communication cables as shown in Figure 2. Voltmeters are optional but it is recommended in order to accurately verify that each one of the output supplies is providing the correct voltage level.

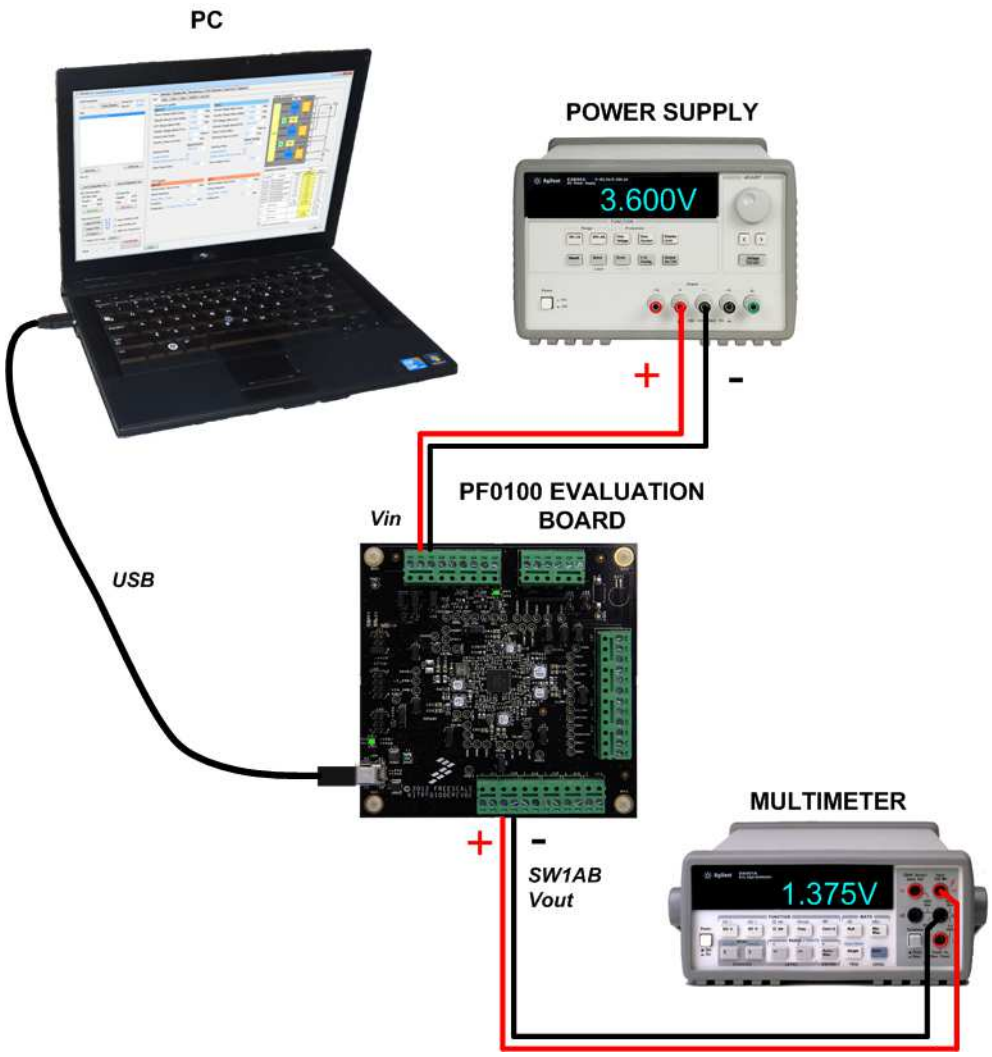



**Figure 2. Evaluation Board Setup**

Note: The KITPF0100EPEVBE allows the selection of SW2 regulator output or an external 3.3 V LDO output as the VDDIO/$I^2C$ pull-up supply. By default, the SW2 regulator is the source for the VDDIO supply (J46 = 3-4). If the SW2 regulator is to be set below 3.0 V then switch the 3.3 V LDO connection to VDDIO (J46 = 1-2.)

# 8 Evaluation Board Schematic

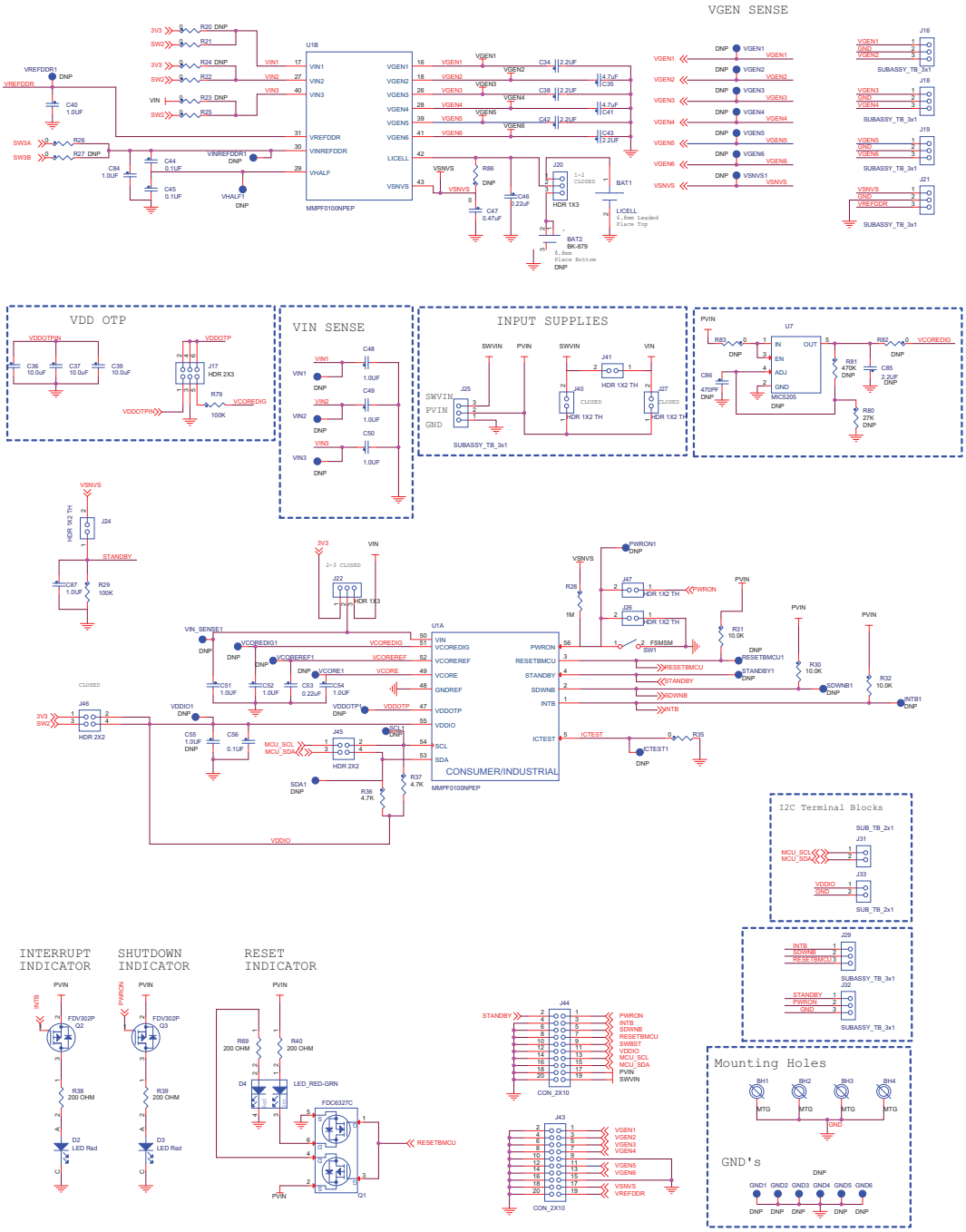



**Figure 3. KITPF0100EPEVBE LDO/Control Schematic Part 1**

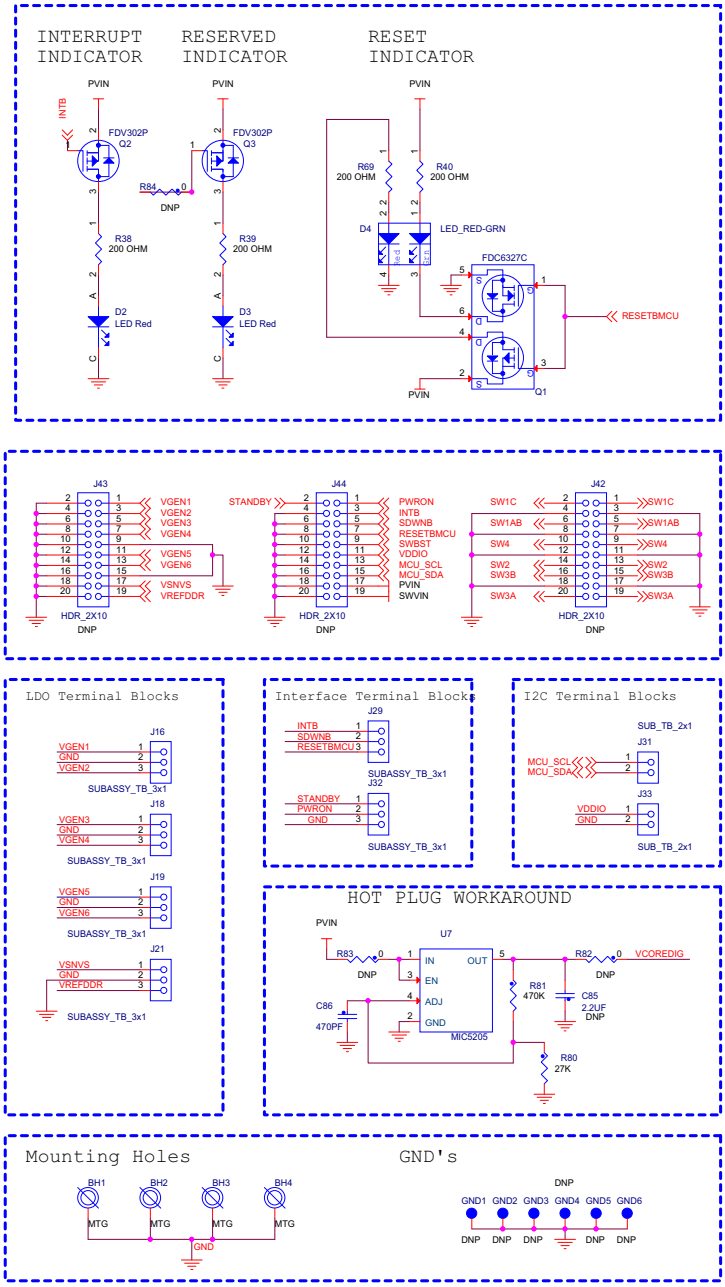



**Figure 4. KITPF0100EPEVBE LDO/Control Schematic Part 2**

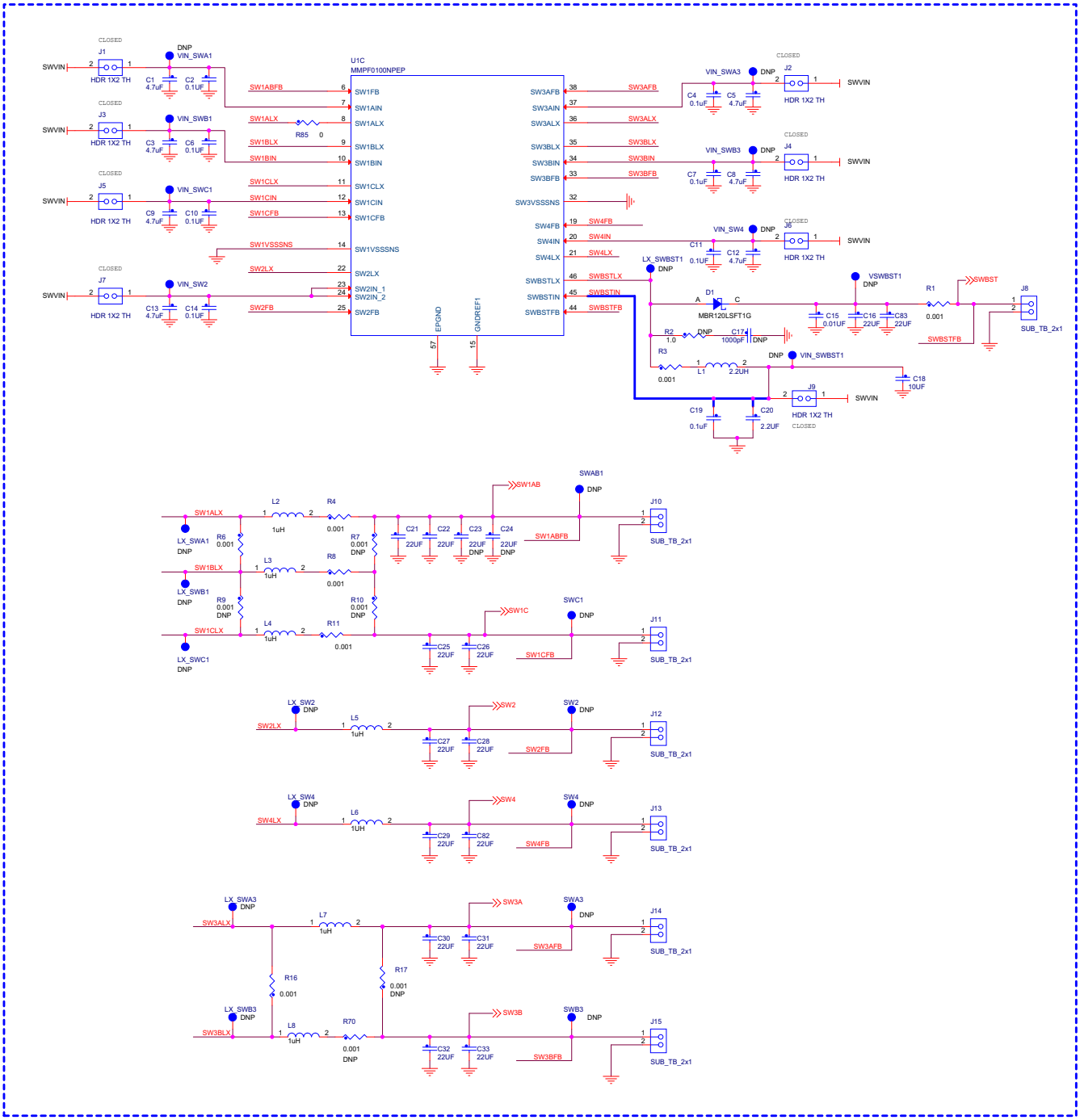



**Figure 5. KITPF0100EPEVBE Switching Regulators Schematic**

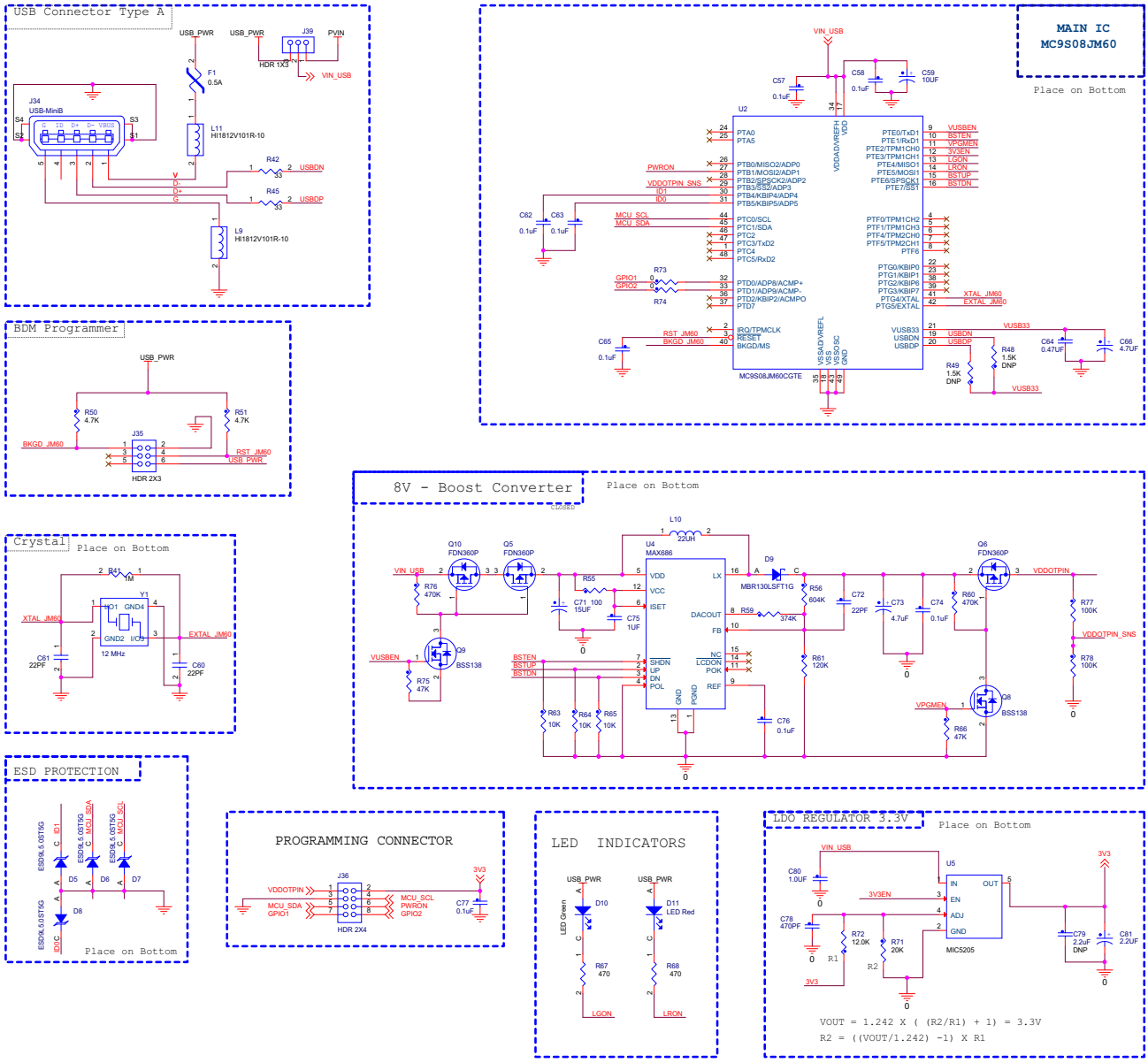



**Figure 6. KITPF0100EPEVBE Control/Programming Interface Schematic**

# 9 Hardware Description

The KITPF0100EPEVBE operates with a single power supply from 3.1 V to 4.5 V and is controlled via USB with help of an integrated USB-$I^2C$ communication bridge. By applying the input voltage supply, the KITPF0100EPEVBE powers up according to the default power-up sequence described in the MMPF0100 Data Sheet.

**Important notice:** If power-up sequences and configuration are to be modified, the user must ensure that the register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the start-up sequence. Refer to the MMPF0100 Data Sheet for details on buck regulator setup.

## 9.1 Jumper Description

By default, the KITPF0100EPEVBE evaluation board is set to power up from the default power-up sequence. Verify that the jumpers are placed in the right position as shown in Figure 7. For a detailed description of the jumper functionality, refer to Table 1.

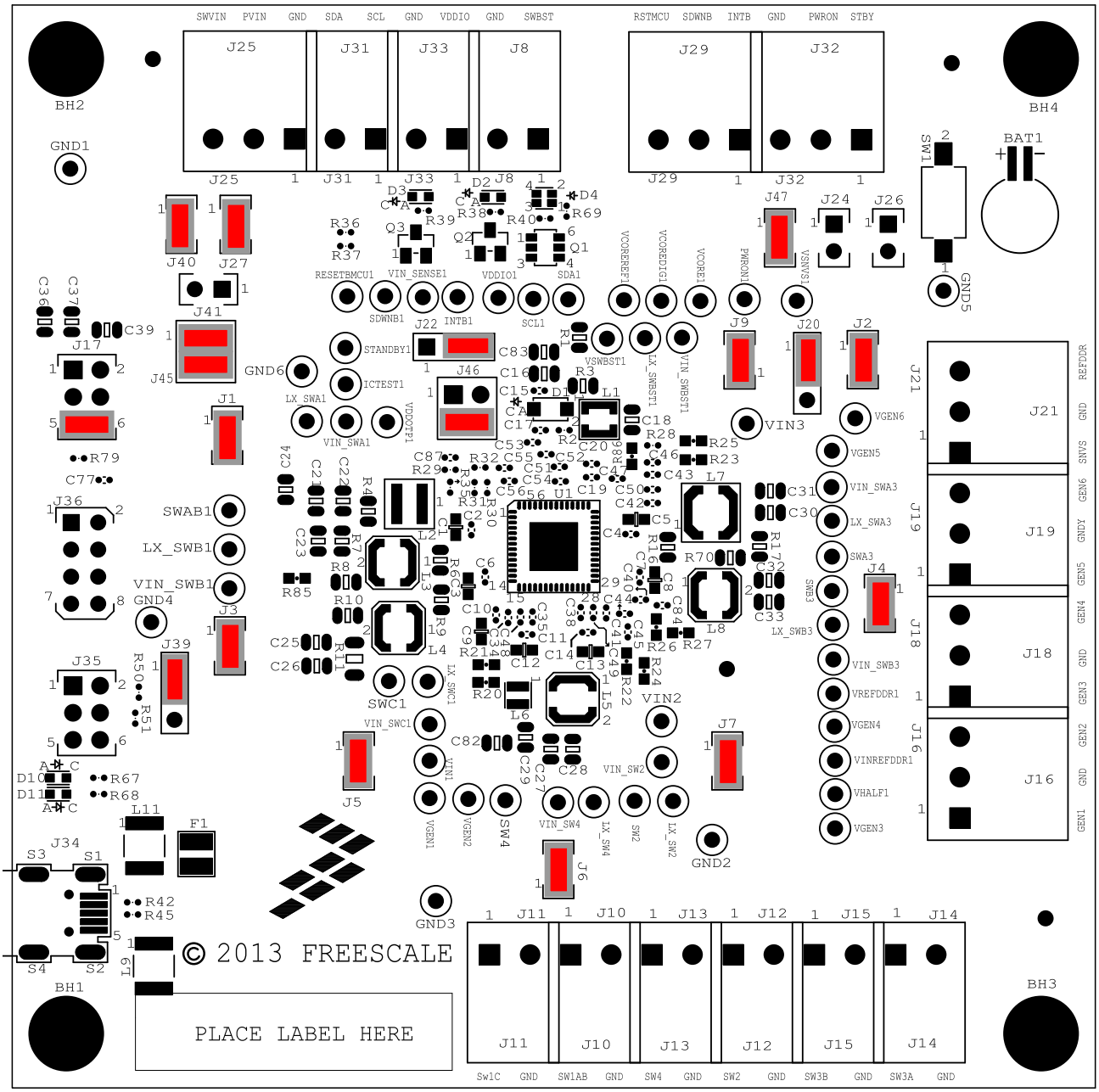



**Figure 7. Default Jumper Configuration Diagram**

**Table 1. KITPF0100EPEVBE Jumper Description**

| Jumper | Default | Description |
|---|---|---|
| J1-J7 | Closed | Buck regulators input power path isolation.<br>Short these jumpers to allow SWxIN to be powered from the SWVIN supply. |
| J9 | Closed | SWBST regulator input power path isolation.<br>Short this jumper to allow SWBSTIN to be powered from the SWVIN supply. |

**Table 1. KITPF0100EPEVBE Jumper Description (continued)**

| Jumper | Default | Description |
|---|---|---|
| J17 | 5-6 | VDDOTP Supply selector<br>• 1-2: Connect VDDOTP to the OTP Boost output (VDDOTPIN) for OTP programming.<br>• 3-4: Connect VDDOTP to GND to power up from OTP/TBB sequence.<br>• 5-6: Connect VDDOTP to VCOREDIG to power up from Default Power up sequence. |
| J20 | 1-2 | Coin cell selector.<br>• 1-2: Enables BAT1 as the main coin cell supply.<br>• 2-3: Enables BAT2 as the main coin cell supply. |
| J40 | Closed | Shorts PVIN and SWVIN. Allows supply isolation to provide more accurate efficiency readings on the switching supplies. |
| J41 | Open | Shorts SWVIN to VIN. Allows one to isolate or connect the PF0100 logic input supply to SWVIN net. (debugging option) |
| J27 | Closed | Shorts PVIN to VIN. Allows one to isolate or connect the PF0100 logic input supply to PVIN net. (debugging option) |
| J22 | 2-3 | PF0100 input logic supply selector.<br>• 1-2: Connects PF0100 VIN terminal to the 3.3 V external LDO regulator for debugging purposes.<br>• 2-3: Connects PF0100 VIN terminal to the main input supply. Refer to Figure 3. |
| J26 | Open | Short to hold PWRON pin low. |
| J24 | Open | Short to pull STANDBY to VSNVS voltage supply. |
| J39 | 1-2 | Control Interface input supply selector<br>• 1-2: Enables PVIN node as the input supply source for the control interface.<br>• 2-3: Enables USB power as the input supply source for the control interface. |

## 9.2 Connectors and Terminal Blocks Description

**Table 2. Terminal Blocks descriptions**

| Connector | Function | Pin definition |
|---|---|---|
| J8 | SWBST | Pin 1 - SWBST Output<br>Pin 2 - GND |
| J10 | SW1AB | Pin 1 - SW1AB Output<br>Pin 2 - GND |
| J11 | SW1C | Pin 1 - SW1C Output<br>Pin 2 - GND |
| J12 | SW2 | Pin 1 - SW2 Output<br>Pin 2 - GND |
| J13 | SW4 | Pin 1 - SW4 Output<br>Pin 2 - GND |
| J14 | SW3A | Pin 1 - SW3A Output<br>Pin 2 - GND |
| J15 | SW3B | Pin 1 - SW3B Output<br>Pin 2 - GND |
| J16 | VGEN1/VGEN2 | Pin 1 - VGEN1 Output<br>Pin 2 - GND<br>Pin 3 - VGEN2 Output |
| J18 | VGEN3/VGEN4 | Pin 1 - VGEN3 Output<br>Pin 2 - GND<br>Pin 3 - VGEN4 Output |
| J19 | VGEN5/VGEN6 | Pin 1 - VGEN5 Output<br>Pin 2 - GND<br>Pin 3 - VGEN6 Output |

**Table 2. Terminal Blocks descriptions (continued)**

| Connector | Function | Pin definition |
|---|---|---|
| J21 | VSNVS/VREFDDR | Pin 1 - VSNVS Output<br>Pin 2 - GND<br>Pin 3 - VREFDDR Output |
| J25 | Main Input Supply | Pin 1 - GND<br>Pin 2 - PVIN<br>Pin 3 - SWVIN |
| J29 | Interfacing 1 | Pin 1 - INTB<br>Pin 2 - SDWNB<br>Pin 3 - RESETBMCU |
| J32 | Interfacing 2 | Pin 1 - STANDBY<br>Pin 2 - PWRON<br>Pin 3 - GND |
| J31 | $I^2C$ Signals | Pin 1 - SCL<br>Pin 2 - SDA |
| J33 | VDDIO | Pin 1 - VDDIO<br>Pin 2 - GND |

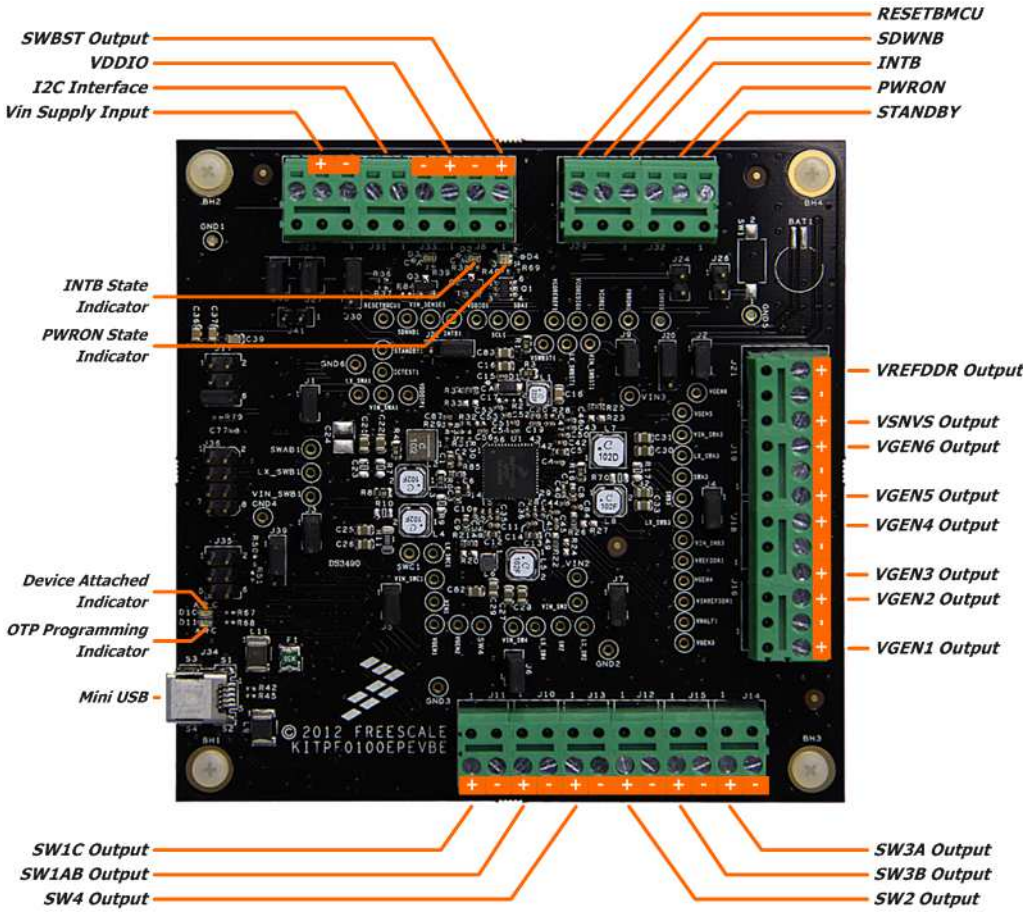
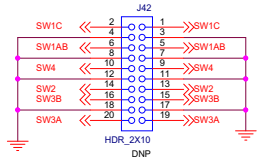
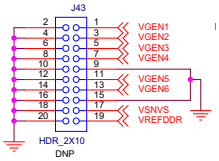
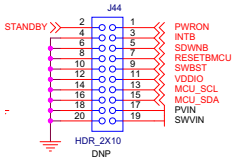



**Figure 8. Input/Output Terminal Blocks**

**Table 3. Connector Description**

| Connector | Function | Pin definition |
|---|---|---|
| J34 | Mini USB connector | Pin 1 - VBUS<br>Pin 2 - D-<br>Pin 3 - D+<br>Pin 4 - NC<br>Pin 5 - GND<br>Chassis - GND |
| J35 | BDM connector | Pin 1 - BKGD_JM60<br>Pin 2 - GND<br>Pin 3 - NC<br>Pin 4 - RST_JM60<br>Pin 5 - NC<br>Pin 6 - USB_PWR |
| J36 | Programmer connector | Pin 1 - VDDOTPIN (8.5V boost output)<br>Pin 2 - 3V3 (3.3 V LDO output)<br>Pin 3 - GND<br>Pin 4 - MCU_SCL ($I^2C$ clock signal)<br>Pin 5 - MCU_SDA ($I^2C$ data signal)<br>Pin 6 - PWRON (Controls the PWRON on the target device)<br>Pin 7 - GPIO 1 (General Purpose GPIO)<br>Pin 8 - GPIO 2 (General Purpose GPIO) |
| J42 | Debug Port 1 | Debugging connector for future development tools.<br>  |
| J43 | Debug Port 2 | Debugging connector for future development tools<br>  |
| J44 | Debug Port 3 | Debugging connector for future development tools<br>  |

## 9.3 Debug and Configuration Components

The KITPF0100EPEVBE allows full flexibility to change the default configuration of SW1A/B/C and SW3A/B outputs to one more suitable for a specific application scenario. It also provides several source options for the LDO supplies to test various loading and supplying scenarios.

Test points are provided on key nodes of the KITPF0100EPEVBE to allow full debugging capability during application development.

### 9.3.1 SW1A/B/C Configuration Components

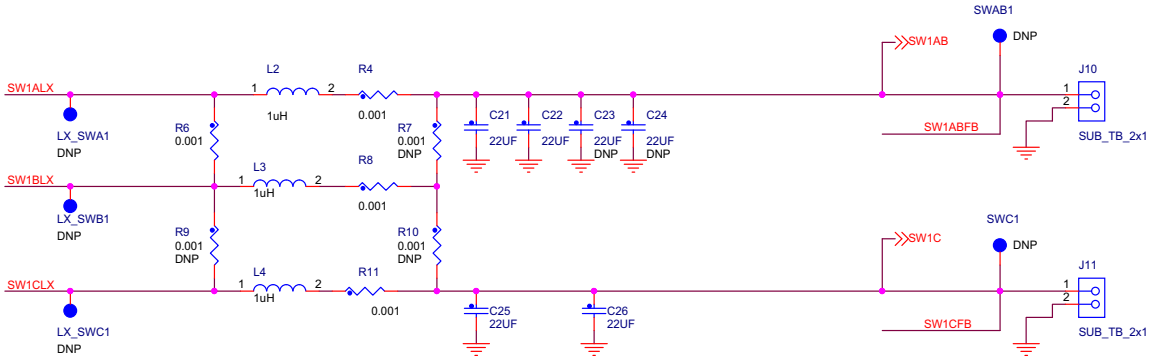



**Figure 9. SW1A/B/C Output Configuration**

The SW1A/B/C regulator can be configured in various operating modes as described in Table 4.

**Table 4. SW1ABC Configuration Chart**

| Component | SW1A/B/C Single phase | SW1A/B Single phase SW1C independent | SW1A/B Dual phase SW1C independent |
|---|---|---|---|
| R6 | Closed | Closed | DNP |
| R9 | Closed | DNP | DNP |
| R4 | Closed | Closed | Closed |
| R7 | Closed | DNP | Closed |
| R8 | DNP | DNP | Closed |
| R10 | Closed | DNP | DNP |
| R11 | DNP | Closed | Closed |
| L2 | 1.0 µH<br>ISAT = 6.0 A | 1.0 µH<br>ISAT = 4.5 A | 1.0 µH<br>ISAT = 2.4 A |
| L3 | N/A | N/A | 1.0 µH<br>ISAT = 2.4 A |
| L4 | N/A | 1.0 µH<br>ISAT = 2.4 A | 1.0 µH<br>ISAT = 2.4 A |

## 9.3.2 SW3A/B Configuration Components

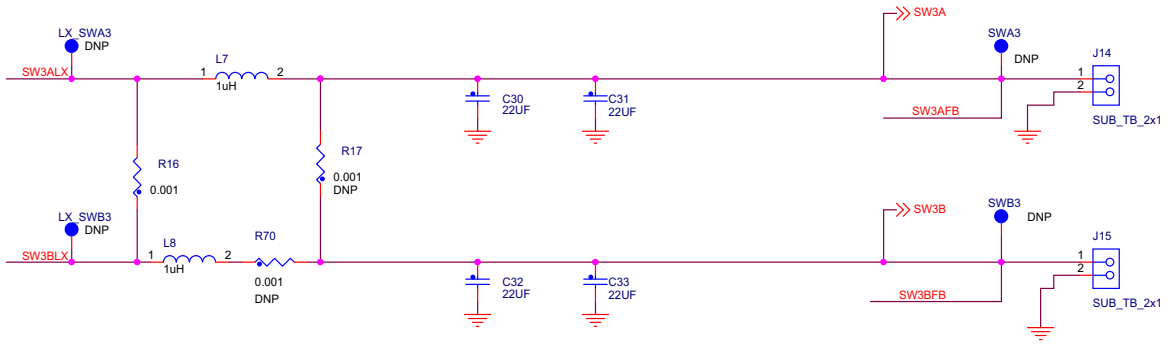



**Figure 10. SW3A/B Output Configuration**

The SW3A/B regulator can be configured in various operating modes as described in Table 5.

**Table 5. SW3ABC Configuration Chart**

| Component | SW3A/B Single phase | SW3A/B Dual phase | SW3A Independent SW3B Independent |
|---|---|---|---|
| R16 | Closed | DNP | DNP |
| R17 | Closed | Closed | DNP |
| R70 | DNP | Closed | Closed |
| L7 | 1.0 µH ISAT = 3.9A | 1.0 µH ISAT = 3.0A | 1.0 µH ISAT = 3.0 A |
| L8 | N/A | 1.0 µH ISAT = 3.0 A | 1.0 µH ISAT = 3.0 A |

## 9.3.3 LDO Input Supply Source Selection

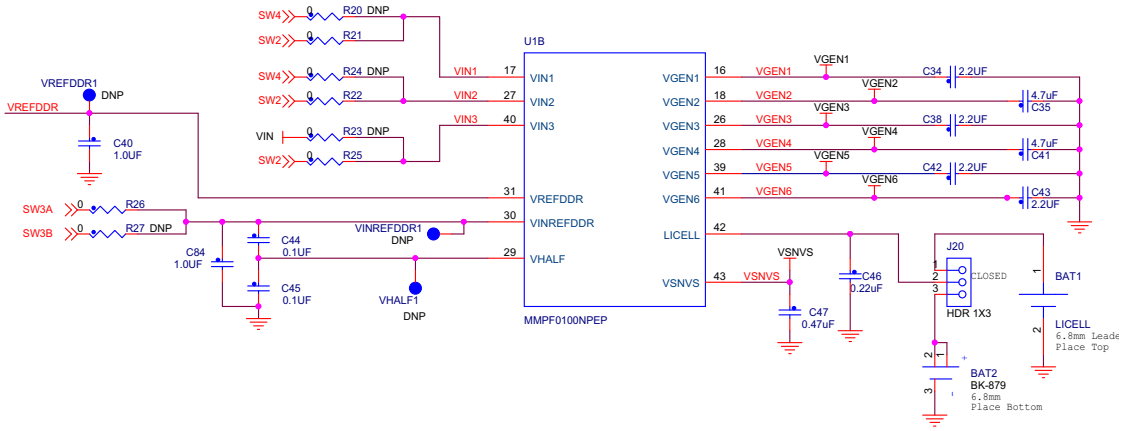



**Figure 11. LDO Schematic Configuration**

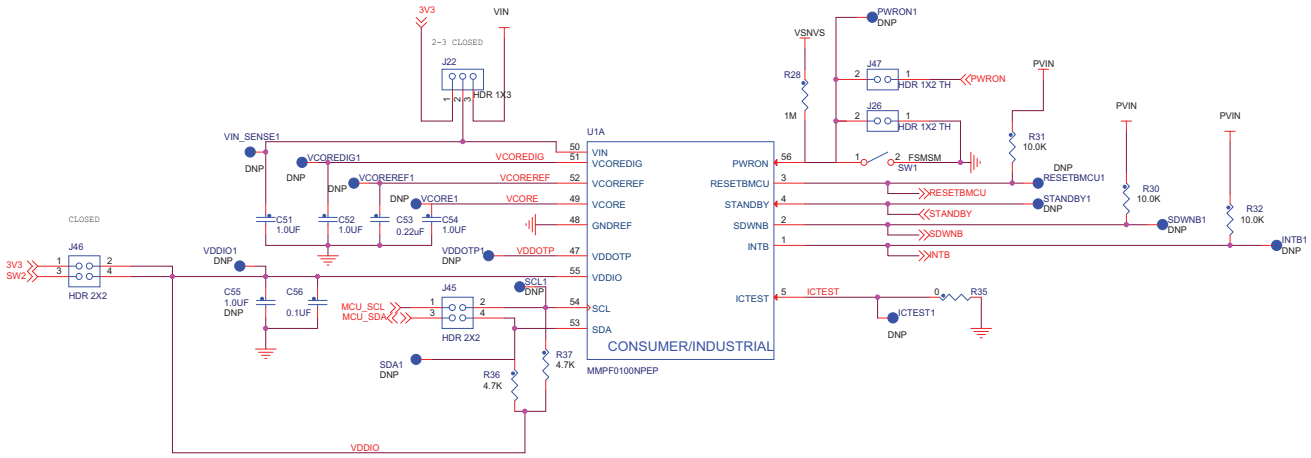



**Figure 12. Logic and Core Supplies Schematic**

**Table 6. LDO Input Supply Configuration Chart**

| Input Pin | Input options |
|---|---|
| VIN1 | Input supply for VGEN1 and VGEN2<br>R20 = SW4<br>R21 = SW2 |
| VIN2 | Input supply for VGEN3 and VGEN4<br>R24 = SW4<br>R22 = SW2 |
| VIN3 | Input supply for VGEN5 and VGEN6<br>R23 = VIN<br>R25 = SW2 |
| VINREFDDR | VREFDDR input supply<br>R26 = SW3A<br>R27 = SW3B |
| VDDIO | VDDIO Input supply<br>3V3 J46 = 1-2<br>SW2 J46 = 2-3 |

1. Make sure to populate only one option per input pin to avoid shorts between various sources.

### 9.3.4 Test point

All test points are clearly marked on the KITPF0100EPEVBE evaluation board. Figure 13 shows the location of various test points of interest during evaluation.

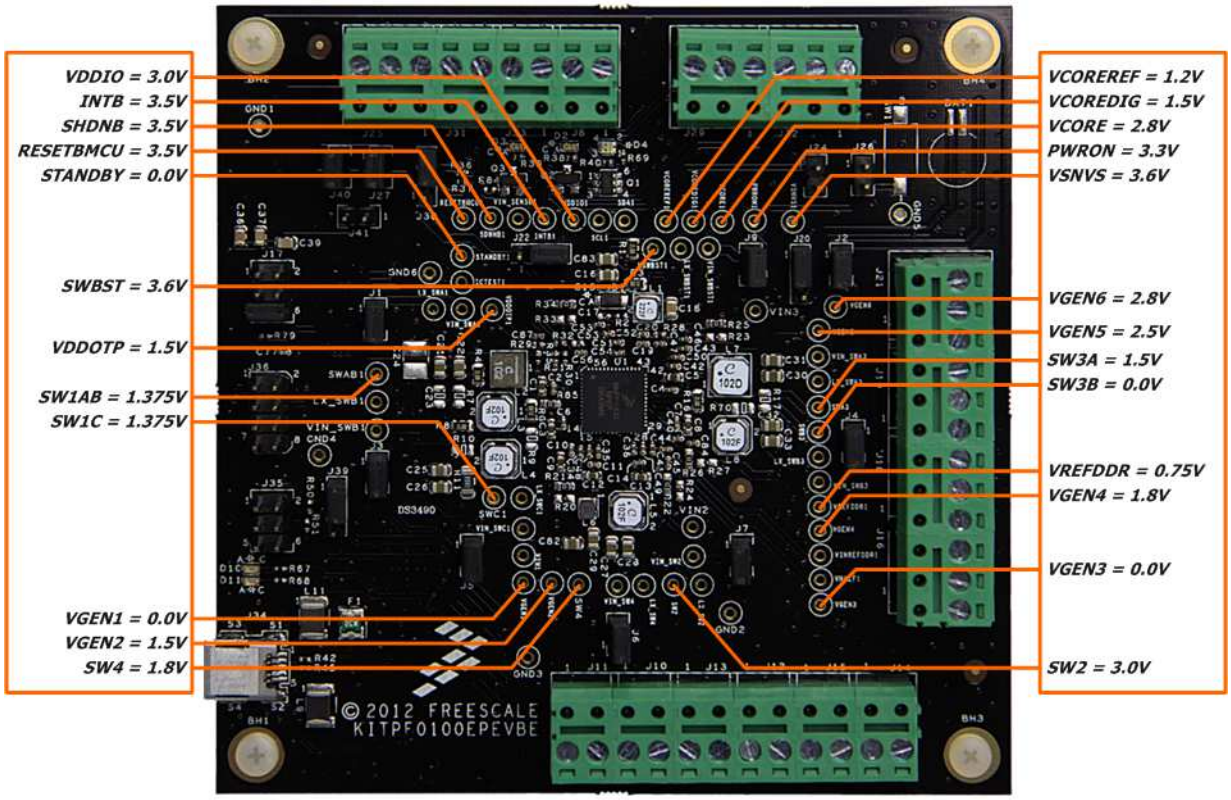



**Figure 13. Key Test Point Locations and Default Voltages**

# 9.4 Miscellaneous Components

## 9.4.1 Power on Push Button

A footprint for a normally open, momentary push-button is provided at the PWRON terminal to allow a momentary low state by pressing the push button. J47 allows isolation of the PWRON terminal from the MCU GPIO controlling this pin.

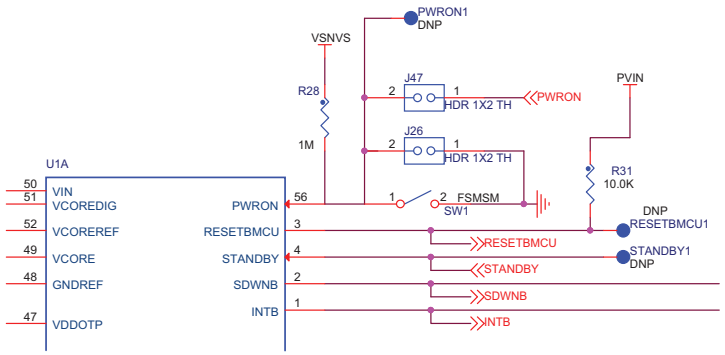



**Figure 14. Power on Circuit**

## 9.4.2 PMIC LED Indicators

LED indicators are provided to notify the PMIC status to the user. Figure 15 shows the PMIC status LEDs D2 and D4, and a Reserved LED indicator D3, that allows for an external rework connection to the transistor gate if any given signal debug is required.

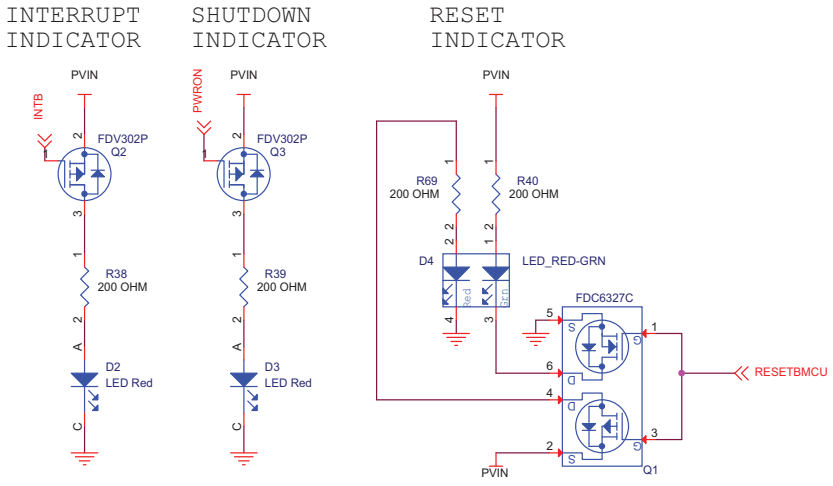



**Figure 15. PMIC Status Indicator**

Table 7 describes the meaning of the LED states.

**Table 7. LED State Description**

| LED | Description |
|---|---|
| D2 | Interrupt Notification<br>ON = PMIC has detected an unmasked interrupt<br>OFF = No interrupt detected |
| D4 | RESETBMCU Notification<br>Green = PMIC is in regulation and operating properly<br>Red = PMIC is out of regulation |
| D3 | Reserved debug LED<br>ON = Q3 gate (R84 pad) is low<br>OFF = Q3 gate (R84 pad) is high or floating |

## 9.4.3 Control/Programming Interface

This onboard USB-to-I$^2$C interface comprises three basic blocks.

1. Controlling MCU (MC9S08JM60CGTE) for USB-I$^2$C translation.
2. 3.3 V LDO supply for external device controlling.
3. 8.25 V boost converter for OTP programming.

The control/programming interface allows one to program the onboard PF0100 PMIC. Alternatively, the interface can serve as a programmer for external devices though the connector J36.

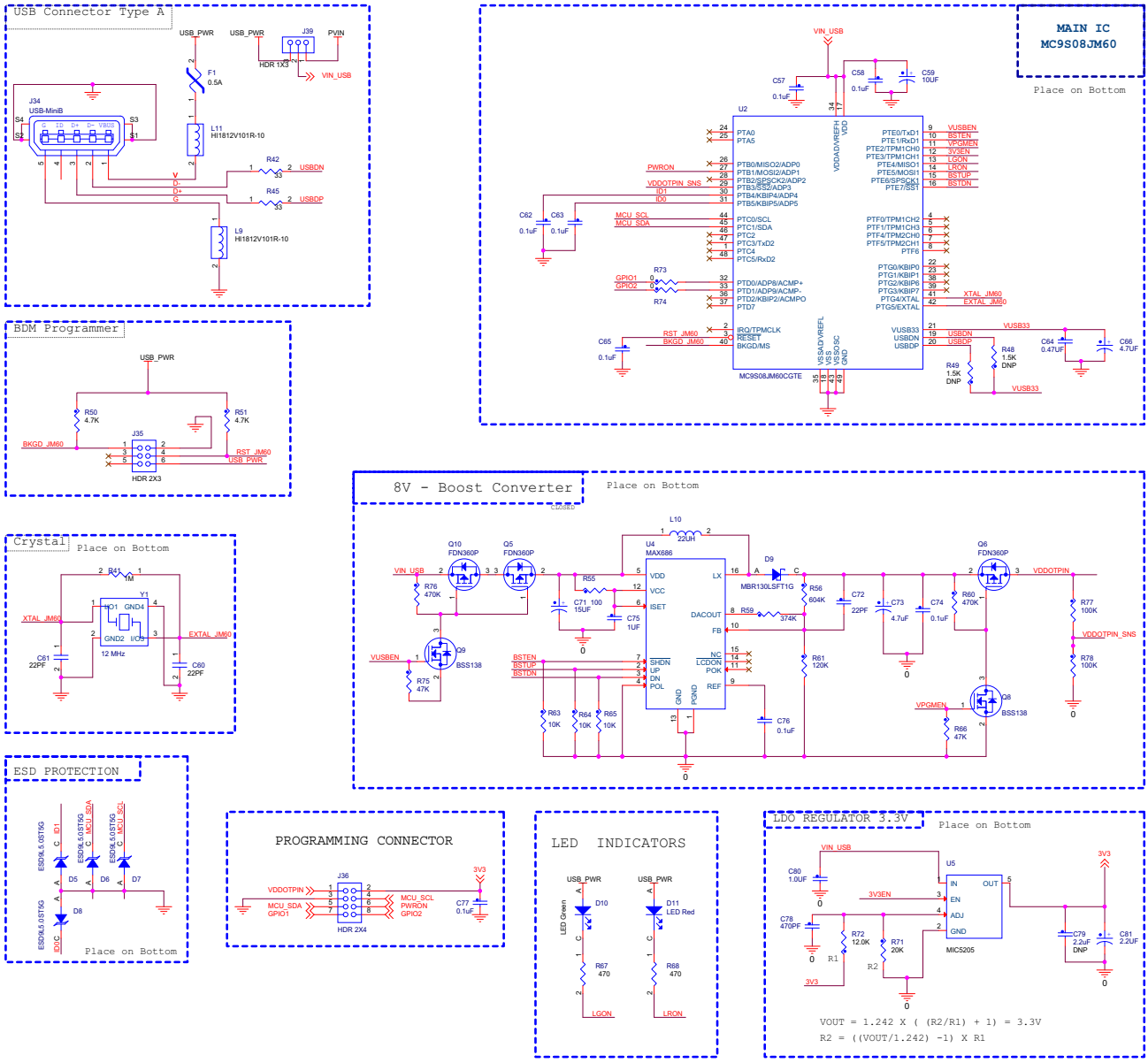



**Figure 16. Control/Programming Interface Schematic**

# 10 KITPF0100EPEVBE Board Layout

## 10.1 Assembly Layer Top

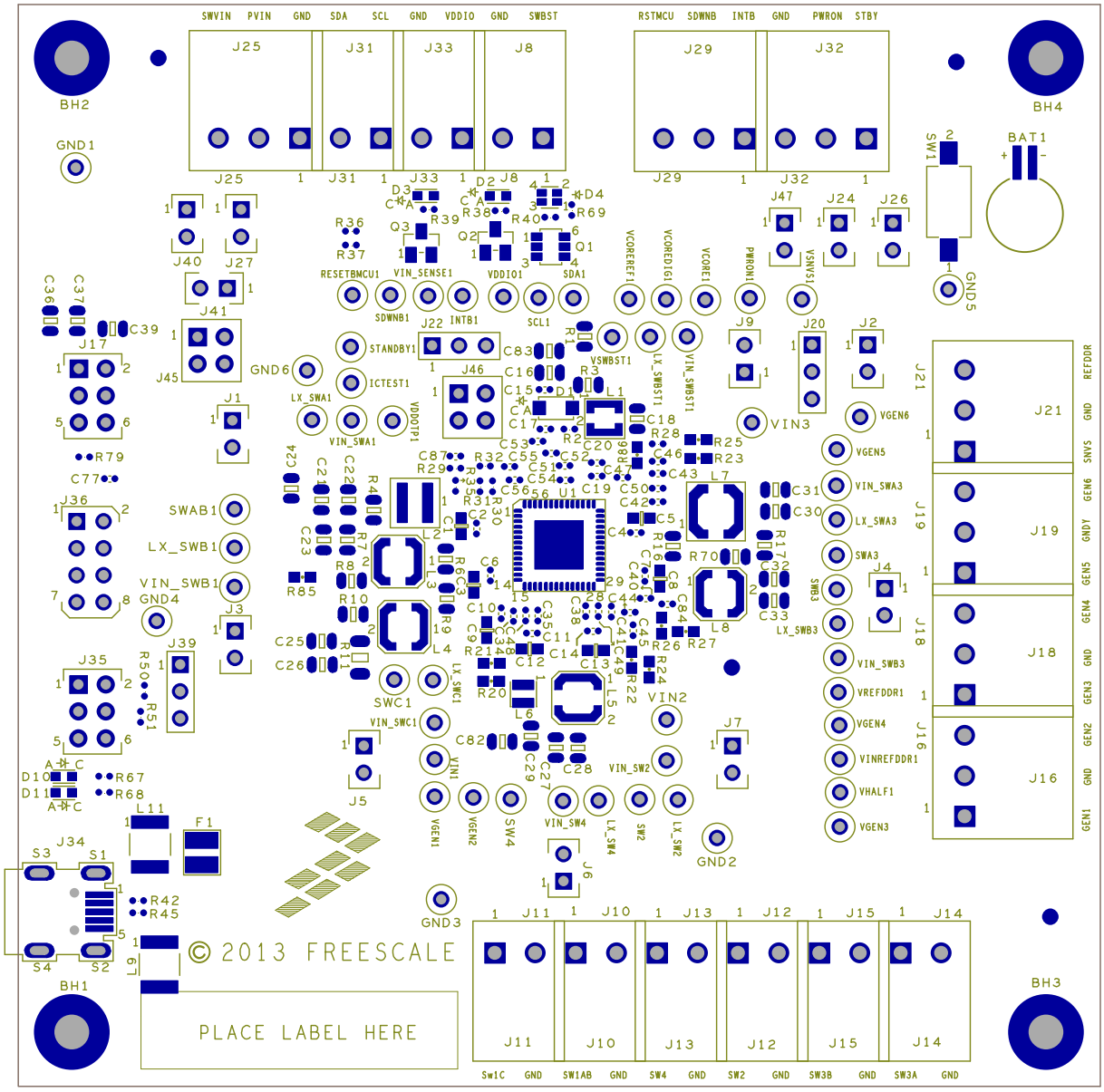



**Figure 17. Assembly Top Layer**

## 10.2 Assembly Layer Bottom

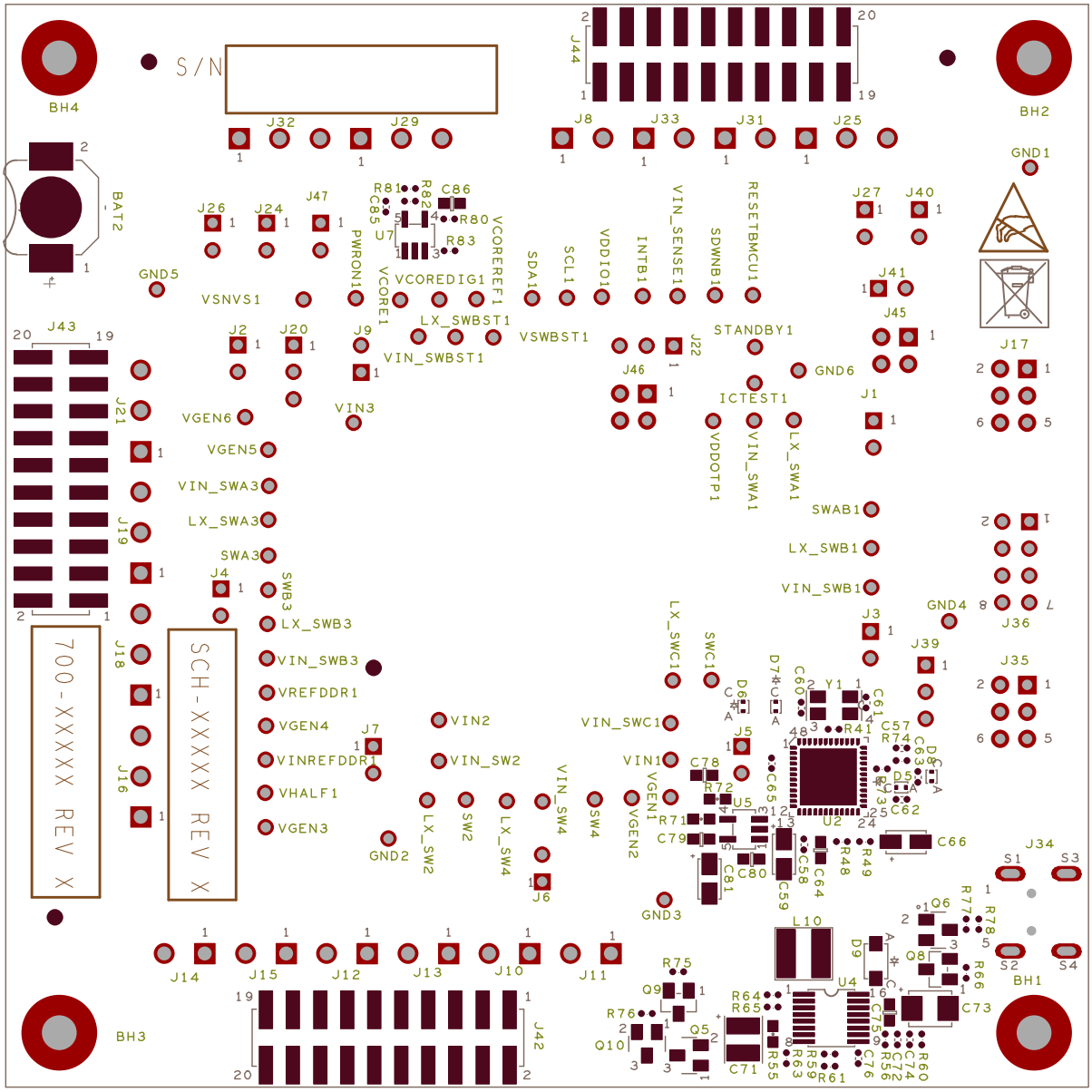



**Figure 18. Assembly Layer Bottom**

## 10.3 Top Layer Routing

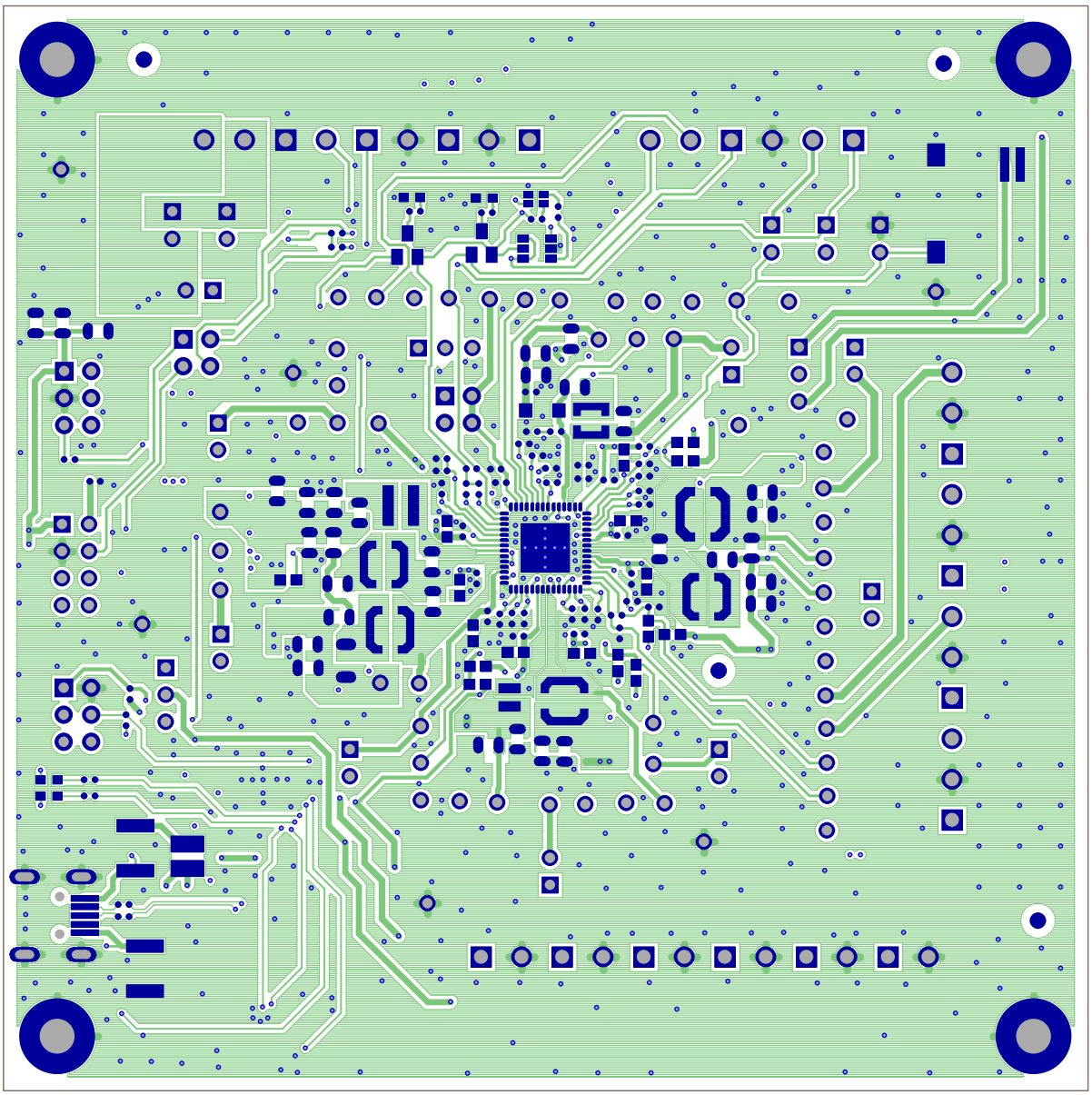


Figure 19. Top Layer Routing