Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

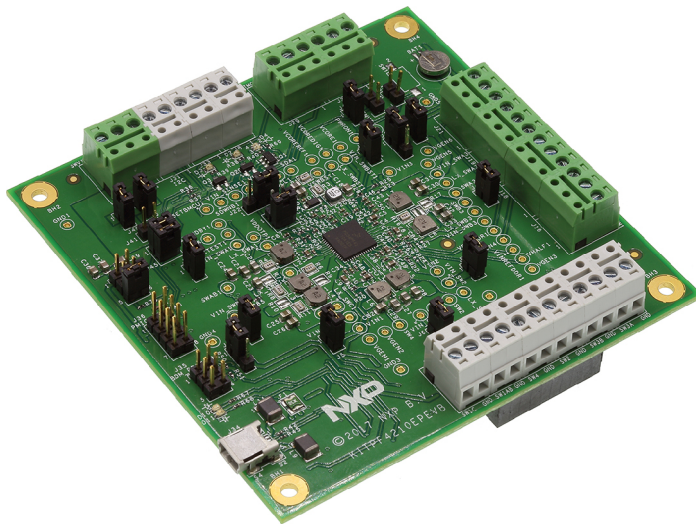# Contact us

# KTPF4210EPEVBUG
## KITPF4210EPEVB evaluation board
**Rev. 1.0 — 8 February 2018**    **User guide**

## 1    KITPF4210EPEVB



*aaa-029237*

## 2 Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typical", must be validated for each customer application by customer's technical experts.

NXP does not convey any license under its patent rights nor the rights of others. NXP products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the NXP product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use NXP products for any such unintended or unauthorized application, the Buyer shall indemnify and hold NXP and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges NXP was negligent regarding the design or manufacture of the part.

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. © NXP B.V. 2018.

# 3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

The tool summary page for KITPF4210EPEVB is located at http://www.nxp.com/ KITPF4210EPEVB. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, list of (and links to) any related products and a **Get Started** section.

The **Get Started** section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the KITPF4210EPEVB.

- Go to http://www.nxp.com/KITPF4210EPEVB.
- On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
- Select either the **Get Started** link or scroll in the main window of the **Overview** tab until the **Get Started** section is visible.
- Review each entry in the **Get Started** section.
- Download an entry by clicking on the title.
- After reviewing the **Overview** tab, visit the other product related tabs for additional information:
  - **Documentation**: download current documentation
  - **Software & Tools**: download current hardware and software tools
  - **Buy/Parametrics**: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

## 3.1 Kit contents/packing list

The KITPF4210EPEVB contents include:

- Assembled and tested KITPF4210EPEVB board in an anti-static bag
- Quick start guide
- Warranty card

## 3.2 Required equipment

To use this kit, you need:

- Power supply:
  - Output voltage range from 3.1 V to 4.5 V
  - Current capability from 3.0 to 5.0 A (current requirement is dependent on output loading)
- Supply to board connection cables (capable of withstanding up to 5.0 A current)
- USB (male) to mini USB (male) communication cable
- USB-enabled computer

### 3.3  System requirements

The kit requires the following to function properly with the software:

- Windows XP or Windows 7 operating system

## 4  Getting to know the hardware

### 4.1  Board features

- Input voltage operation range from 3.1 V to 4.5 V
- Output voltage supplies accessible through detachable terminal blocks
  - Four to six independent buck converters
  - One 5.0 V boost regulator
  - Six general purpose LDO regulators
  - One DDR memory termination voltage reference
  - One VSRTC supply
- Coin cell support for "Try-Before-Buy" (TBB) mode
- On/off push button support
- Hardware configuration flexibility through various jumper headers and resistors
- Integrated USB to I$^2$C programming interface for full control/configuration
  - Onboard PMIC control through the I$^2$C register map
  - Fully featured programmer through J36 for external device control/programming
- On board connectors for interfacing with future evaluation/debug tools
- Compact form factor (4 x 4 in$^2$)

## 4.2 Device features

**Table 1. Device features**

| Device | Description | Features |
|---|---|---|
| PF4210 | The PF4210 Power Management Integrated Circuit (PMIC) provides a highly programmable/configurable architecture with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF4210 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications. | • Four to six buck converters, depending on configuration<br>  – Single/Dual phase/ parallel options<br>  – DDR termination tracking mode option<br>• Boost regulator to 5.0 V output<br>• Six general purpose linear regulators<br>• Programmable output voltage, sequence, and timing<br>• OTP (One Time Programmable) memory for device configuration<br>• Coin cell charger and RTC supply<br>• DDR termination reference voltage<br>• Power control logic with processor interface and event detection<br>• $I^2C$ control<br>• Individually programmable ON, OFF, and Standby modes |
| MC9S08JM60 | The KITPF4210EPEVB implements a NXP MC9S08JM60 low-cost, high-performance 8-bit HCS08 microcontroller to interface via USB to $I^2C$ to control the main PMIC. | • 8-bit HCS08 Central Processing Unit (CPU)<br>  – Up to 24 MHz internal bus (48 MHz HCS08 core) frequency offering 2.7 to 5.5 V across temperature range of −40 °C to +85 °C<br>  – Support for up to 32 peripheral interrupt/reset sources<br>• On-chip memory<br>  – Up to 60 K flash read/program/erase over full operating voltage and temperature<br>  – Up to 4 K RAM<br>  – 256 Byte USB RAM |

## 4.3 Board description

The KITPF4210EPEVB operates with a single power supply from 3.1 V to 4.5 V and is controlled via USB with help of an integrated USB-I2C communication bridge. By applying the input voltage supply, the KITPF4210EPEVB powers up according to the default power-up sequence described in the PF4210 data sheet.

*Important: If power-up sequences and configurations are to be modified, the user must ensure that the register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the start-up sequence. See PF4210 data sheet for details on buck regulator setup.*

### 4.3.1 Jumper definitions

By default, the KITPF4210EPEVB evaluation board is set to power up from the default power-up sequence. Verify that the jumpers are placed in the right position as shown in Figure 1. For a detailed description of the jumper functionality, see Table 2.

*aaa-029239*
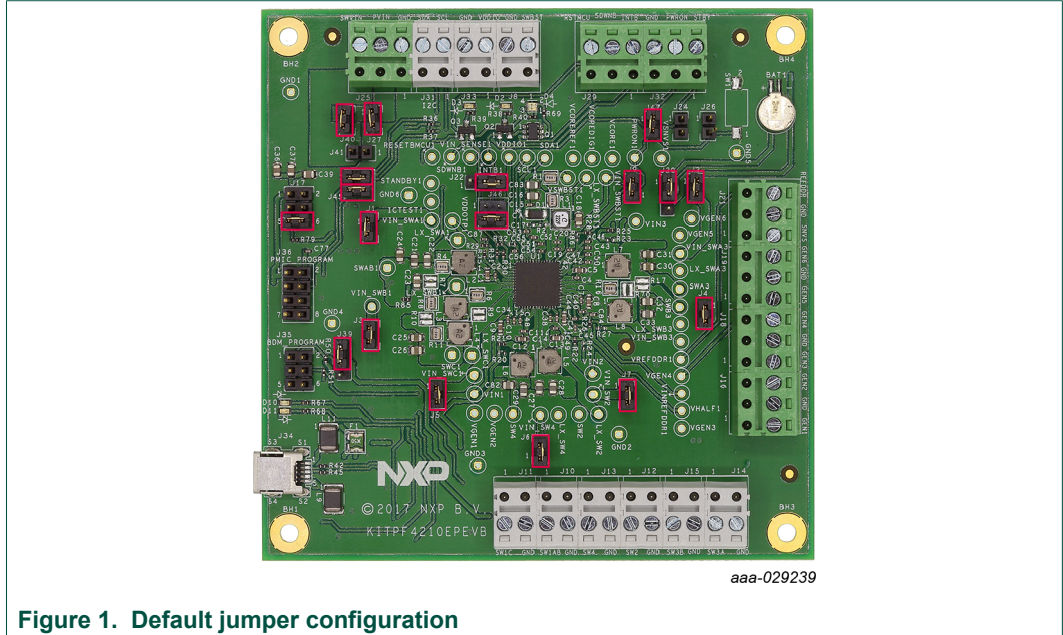
**Figure 1. Default jumper configuration**

**Table 2. Jumper definitions**

| Jumper | Default | Description |
|---|---|---|
| J1-J7 | Closed | Buck regulators input power path isolation<br>Short these jumpers to allow SWxIN to be powered from the SWVIN supply |
| J9 | Closed | SWBST regulator input power path isolation<br>Short this jumper to allow SWBSTIN to be powered from the SWVIN supply |
| J17 | 5-6 | VDDOTP supply selector<br>• 1-2: Connect VDDOTP to the OTP Boost output (VDDOTPIN) for OTP programming<br>• 3-4: Connect VDDOTP to GND to power up from OTP/TBB sequence<br>• 5-6: Connect VDDOTP to VCOREDIG to power up from default power-up sequence |
| J20 | 1-2 | Coin cell selector<br>• 1-2: Enables BAT1 as the main coin cell supply<br>• 2-3: Enables BAT2 as the main coin cell supply |
| J40 | Closed | Shorts PVIN and SWVIN<br>Allows supply isolation to provide more accurate efficiency readings on the switching supplies |
| J41 | Open | Shorts SWVIN to VIN<br>Allows one to isolate or connect the PF4210 logic input supply to SWVIN net. (debugging option) |
| J27 | Closed | Shorts PVIN to VIN<br>Allows one to isolate or connect the PF4210 logic input supply to PVIN net. (debugging option) |
| J22 | 2-3 | PF4210 input logic supply selector<br>• 1-2: Connects PF4210 VIN terminal to the 3.3 V external LDO regulator for debugging purposes<br>• 2-3: Connects PF420 VIN terminal to the main input supply |
| J26 | Open | Short to hold PWRON pin low |
| J24 | Open | Short to pull STANDBY to VSNVS voltage supply |
| J39 | 1-2 | Control interface input supply selector<br>• 1-2: Enables PVIN node as the input supply source for the control interface<br>• 2-3: Enables USB power as the input supply source for the control interface |

### 4.3.2  Connector and terminal block definitions

**Table 3. Terminal block definitions**

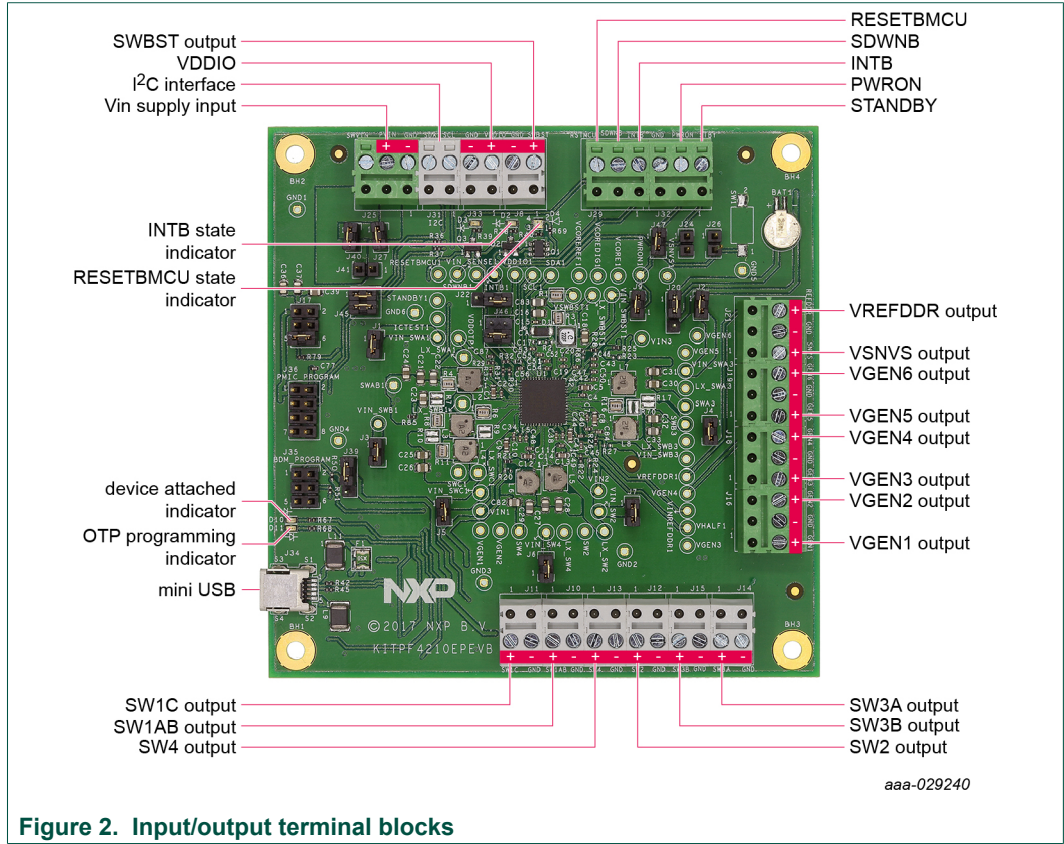| Connector | Function | Pin definition |
|---|---|---|
| J8 | SWBST | Pin 1 - SWBST output<br>Pin 2 - GND |
| J10 | SW1AB | Pin 1 - SW1AB output<br>Pin 2 - GND |
| J11 | SW1C | Pin 1 - SW1C output<br>Pin 2 - GND |
| J12 | SW2 | Pin 1 - SW2 output<br>Pin 2 - GND |
| J13 | SW4 | Pin 1 - SW4 output<br>Pin 2 - GND |
| J14 | SW3A | Pin 1 - SW3A output<br>Pin 2 - GND |
| J15 | SW3B | Pin 1 - SW3B output<br>Pin 2 - GND |
| J16 | VGEN1/VGEN2 | Pin 1 - VGEN1 output<br>Pin 2 - GND<br>Pin 3 - VGEN2 output |
| J18 | VGEN3/VGEN4 | Pin 1 - VGEN3 output<br>Pin 2 - GND<br>Pin 3 - VGEN4 output |
| J19 | VGEN5/VGEN6 | Pin 1 - VGEN5 output<br>Pin 2 - GND<br>Pin 3 - VGEN6 output |
| J21 | VSNVS/VREFDDR | Pin 1 - VSNVS output<br>Pin 2 - GND<br>Pin 3 - VREFDDR output |
| J25 | Main input supply | Pin 1 - GND<br>Pin 2 - PVIN<br>Pin 3 - SWVIN |
| J29 | Interfacing 1 | Pin 1 - INTB<br>Pin 2 - SDWNB<br>Pin 3 - RESETBMCU |
| J32 | Interfacing 2 | Pin 1 - STANDBY<br>Pin 2 - PWRON<br>Pin 3 - GND |
| J31 | $I^2C$ signals | Pin 1 - SCL<br>Pin 2 - SDA |
| J33 | VDDIO | Pin 1 - VDDIO<br>Pin 2 - GND |

**Figure 2. Input/output terminal blocks**

**Table 4. Connector definitions**

| Connector | Function | Pin definition |
|---|---|---|
| J34 | Mini USB connector | Pin 1 - VBUS<br>Pin 2 - D−<br>Pin 3 - D+<br>Pin 4 - NC<br>Pin 5 - GND<br>Chassis - GND |
| J35 | BDM connector | Pin 1 - BKGD_JM60<br>Pin 2 - GND<br>Pin 3 - NC<br>Pin 4 - RST_JM60<br>Pin 5 - NC<br>Pin 6 - USB_PWR |
| J36 | Programmer connector | Pin 1 - VDDOTPIN (8.5 V boost output)<br>Pin 2 - 3V3 (3.3 V LDO output)<br>Pin 3 - GND<br>Pin 4 - MCU_SCL ($I^2C$ clock signal)<br>Pin 5 - MCU_SDA ($I^2C$ data signal)<br>Pin 6 - PWRON (controls the PWRON on the target device)<br>Pin 7 - GPIO 1 (general purpose GPIO)<br>Pin 8 - GPIO 2 (general purpose GPIO) |
| J42 | Debug Port 1 | Debugging connector for future development tools |
| J43 | Debug Port 2 | Debugging connector for future development tools |
| J44 | Debug Port 3 | Debugging connector for future development tools |

KTPF4210EPEVBUG

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

**User guide**

**Rev. 1.0 — 8 February 2018**

**8 / 18**

### 4.3.3 Debug and configuration components

The KITPF4210EPEVB allows full flexibility to change the default configuration of SW1A/B/C and SW3A/B outputs to one more suitable for a specific application scenario. It also provides several source options for the LDO supplies to test various loading and supplying scenarios.

Test points are provided on key nodes of the KITPF4210EPEVB to allow full debugging capability during application development.

#### 4.3.3.1 SW1A/B/C configuration components

The SW1A/B/C regulator can be configured in various operating modes as described in Table 5.
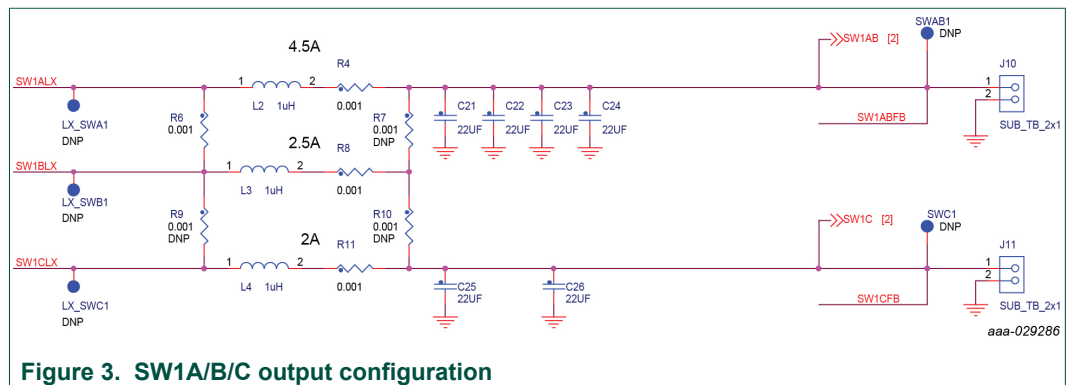


**Figure 3. SW1A/B/C output configuration**

**Table 5. SW1A/B/C configuration chart**

| Component | SW1A/B/C single phase | SW1A/B single phase SW1C independent | SW1A/B dual phase SW1C independent |
|---|---|---|---|
| R6 | Closed | Closed | DNP |
| R9 | Closed | DNP | DNP |
| R4 | Closed | Closed | Closed |
| R7 | Closed | DNP | Closed |
| R8 | DNP | DNP | Closed |
| R10 | Closed | DNP | DNP |
| R11 | DNP | Closed | Closed |
| L2 | 1.0 µH ISAT = 6.0 A | 1.0 µH ISAT = 4.5 A | 1.0 µH ISAT = 2.4 A |
| L3 | N/A | N/A | 1.0 µH ISAT = 2.4 A |
| L4 | N/A | 1.0 µH ISAT = 2.4 A | 1.0 µH ISAT = 2.4 A |

#### 4.3.3.2 SW3A/B configuration components

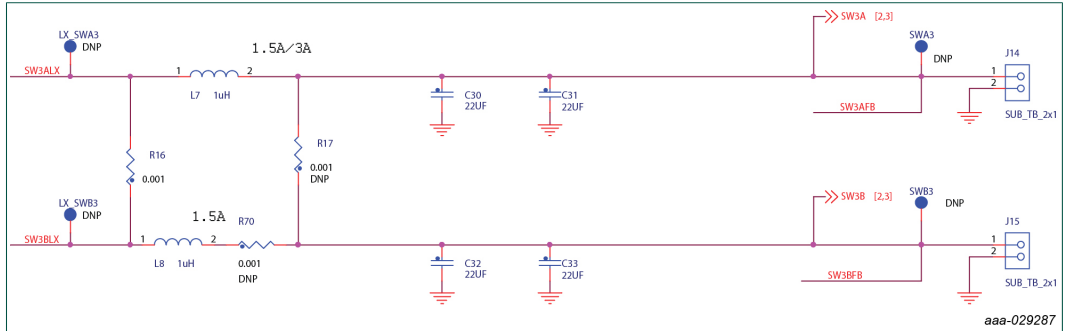The SW3A/B regulator can be configured in various operating modes as described in Table 6.

KTPF4210EPEVBUG

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

**User guide**

**Rev. 1.0 — 8 February 2018**

**9 / 18**

**Figure 4. SW3A/B output configuration**

**Table 6. SW3A/B configuration chart**

| Component | SW3A/B single phase | SW3A/B dual phase | SW3A independent SW3B independent |
|---|---|---|---|
| R16 | Closed | DNP | DNP |
| R17 | Closed | Closed | DNP |
| R70 | DNP | Closed | Closed |
| L7 | 1.0 µH ISAT = 3.9 A | 1.0 µH ISAT = 3.0 A | 1.0 µH ISAT = 3.0 A |
| L8 | N/A | 1.0 µH ISAT = 3.0 A | 1.0 µH ISAT = 3.0 A |

#### 4.3.3.3 LDO input supply source selection
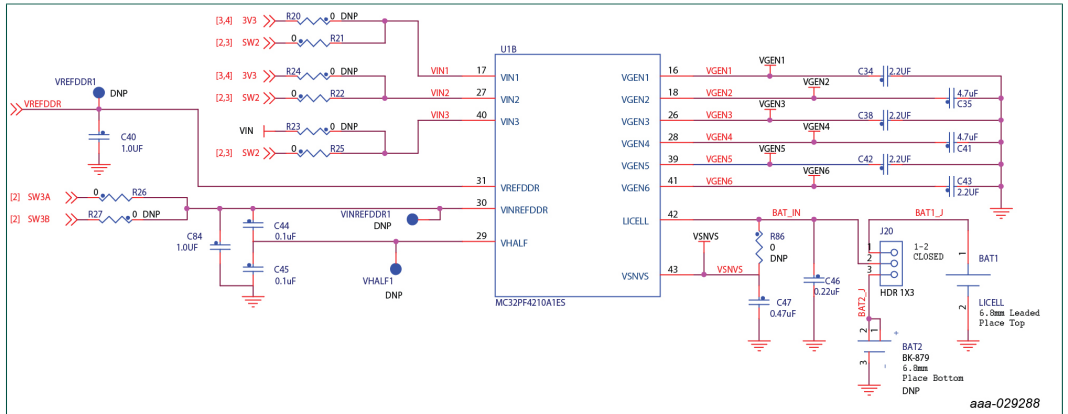


**Figure 5. LDO schematic configuration**
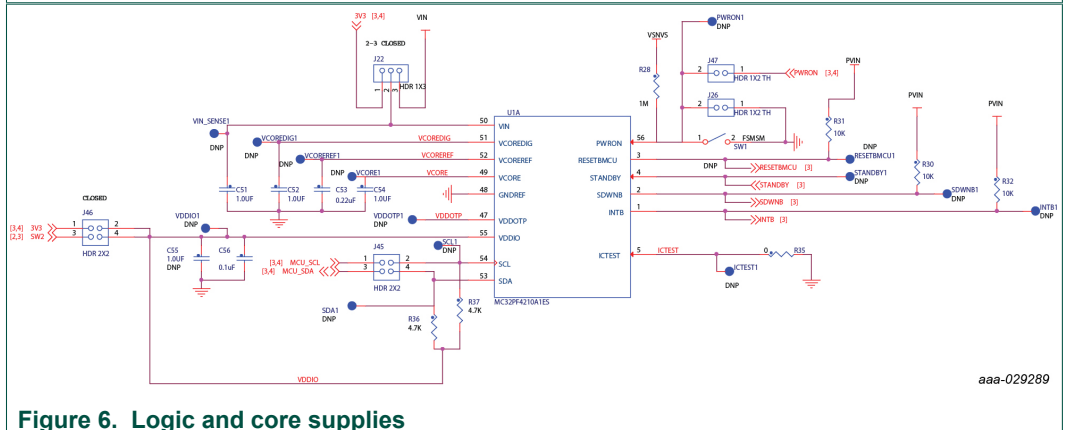


**Figure 6. Logic and core supplies**

KTPF4210EPEVBUG

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

**User guide**

**Rev. 1.0 — 8 February 2018**

**10 / 18**

**Table 7. LDO input supply configuration chart**

| Input pin | Input options [1] |
|---|---|
| VIN1 | Input supply for VGEN1 and VGEN2<br>R20 = SW4<br>R21 = SW2 |
| VIN2 | Input supply for VGEN3 and VGEN4<br>R24 = SW4<br>R22 = SW2 |
| VIN3 | Input supply for VGEN5 and VGEN6<br>R23 = VIN<br>R25 = SW2 |
| VINREFDDR | VREFDDR input supply<br>R26 = SW3A<br>R27 = SW3B |
| VDDIO | VDDIO input supply<br>3V3 J46 = 1-2<br>SW2 J46 = 2-3 |

[1] Make sure to populate only one option per input pin to avoid shorts between various sources.

### 4.3.3.4 Test point definitions

All test points are clearly marked on the KITPF4210EPEVB evaluation board. Figure 7 shows the location of various test points.
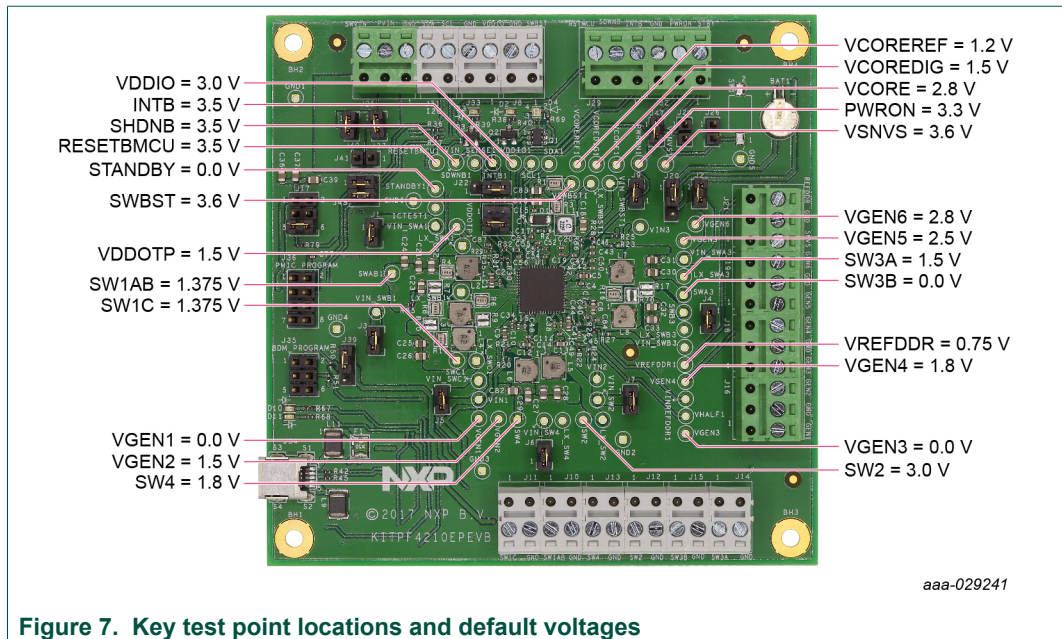


**Figure 7. Key test point locations and default voltages**

## 4.3.4 Miscellaneous components

### 4.3.4.1 Power on push button

A footprint for a normally open, momentary push-button is provided at the PWRON terminal to allow a momentary low state by pressing the push button. J47 allows isolation of the PWRON terminal from the MCU GPIO controlling this pin.
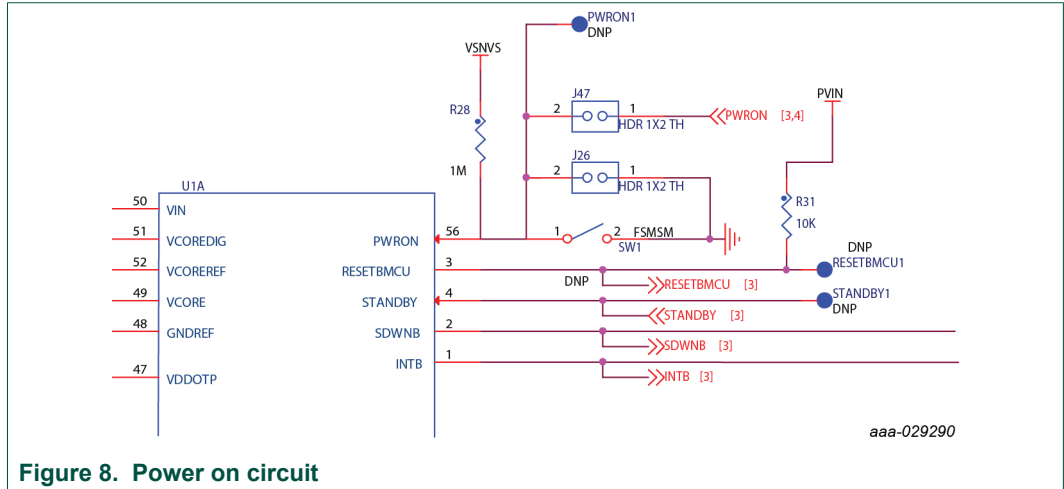
**Figure 8.  Power on circuit**

#### 4.3.4.2  PMIC LED indicators

LED indicators are provided to notify the PMIC status to the user. Figure 9 shows the PMIC status. LEDs D2 and D4, and a reserved LED indicator D3, allow an external rework connection to the transistor gate if any given signal debug is required.
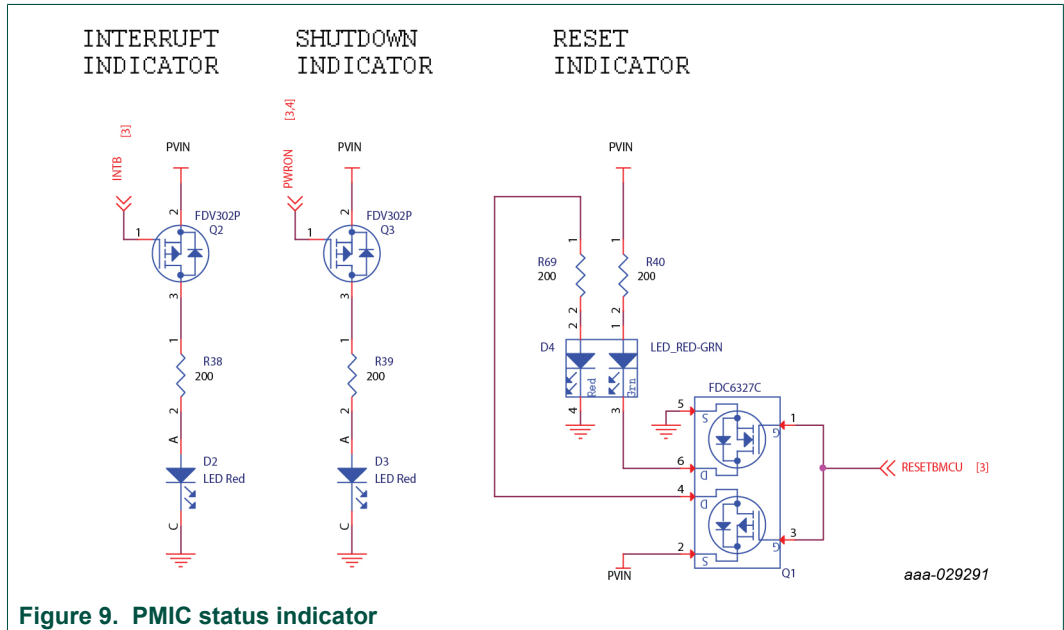


**Figure 9.  PMIC status indicator**

**Table 8.  LED state description**

| LED | Description |
|---|---|
| D2 | Interrupt notification<br>ON = PMIC has detected an unmasked interrupt<br>OFF = No interrupt detected |
| D4 | RESETBMCU notification<br>Green = PMIC is in regulation and operating properly<br>Red = PMIC is out of regulation |
| D3 | PWRON notification<br>ON = PWRON is low<br>OFF = PWRON is high |

KTPF4210EPEVBUG

**User guide**

All information provided in this document is subject to legal disclaimers.

**Rev. 1.0 — 8 February 2018**

© NXP B.V. 2018. All rights reserved.

**12 / 18**

### 4.3.4.3  Control/programming interface

This onboard USB-to-I$^2$C interface comprises three basic blocks.

1. Controlling MCU (MC9S08JM60CGTE) for USB-I2C translation
2. 3.3 V LDO supply for external device controlling
3. 8.25 V boost converter for OTP programming

The control/programming interface allows one to program the onboard PF4210 PMIC. Alternatively, the interface can serve as a programmer for external devices though the connector J36.
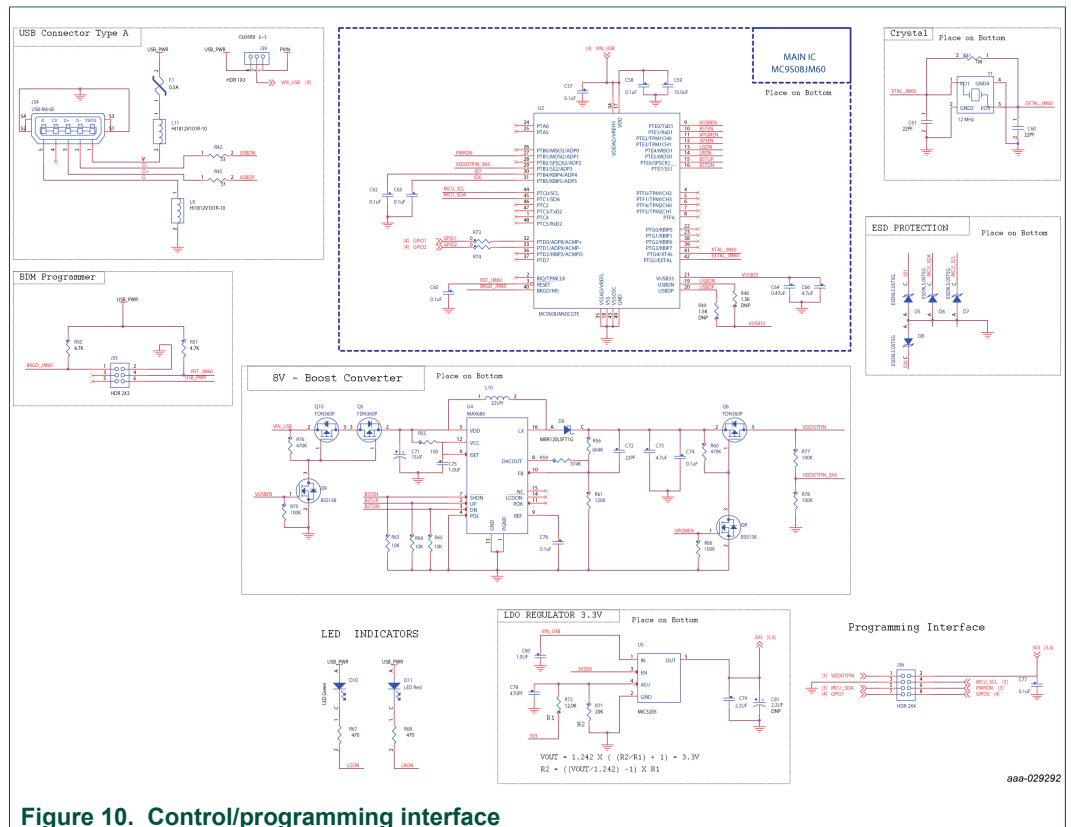


**Figure 10.  Control/programming interface**

# 5    Configuring the hardware

Connect the power supply and the USB communication cables as shown in . Voltmeters are optional but it is recommended in order to accurately verify that each one of the output supplies is providing the correct voltage level.
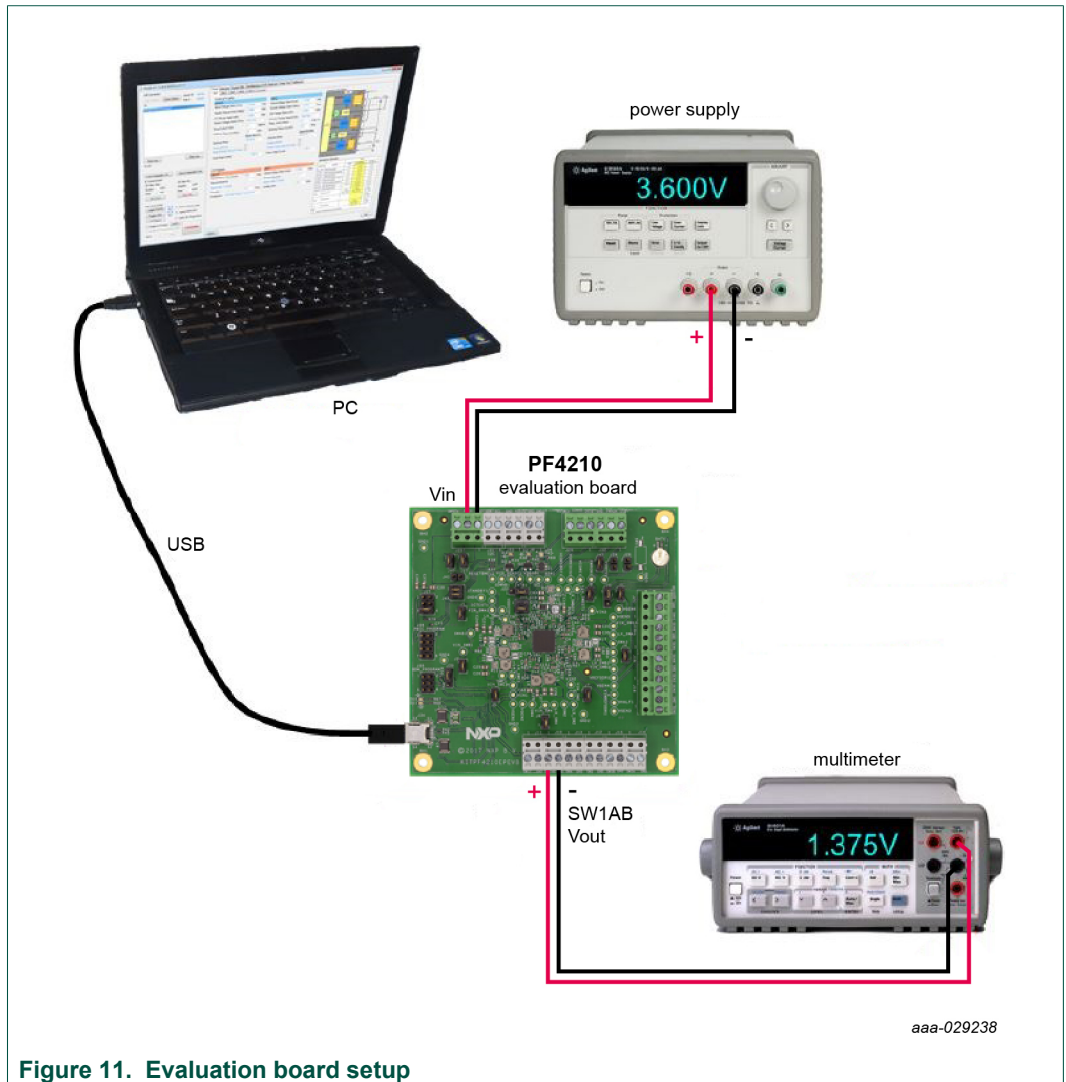
*aaa-029238*

**Figure 11. Evaluation board setup**

*Note: The KITPF4210EPEVB allows the selection of SW2 regulator output or an external 3.3 V LDO output as the VDDIO/I²C pull-up supply. By default, the SW2 regulator is the source for the VDDIO supply (J46 = 3-4). If the SW2 regulator is to be set below 3.0 V, then switch the 3.3 V LDO connection to VDDIO (J46 = 1-2).*

# 6 Schematics, board layout and bill of materials

Board schematics, board layout and bill of materials are available in the download tab of the tool summary page: http://www.nxp.com/KITPF4210EPEVB.

KTPF4210EPEVBUG

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

**User guide**

**Rev. 1.0 — 8 February 2018**

**14 / 18**

## 7    References

Following are URLs where you can obtain information on related NXP products and application solutions:

| NXP.com support pages | Description | URL |
|---|---|---|
| KITPF4210EPEVB | Tool summary page | http://www.nxp.com/KITPF4210EPEVB |
| PF4210 | Product summary page | http://www.nxp.com/PF4210 |

## Revision history

| **Revision history** | | |
|---|---|---|
| **Rev** | **Date** | **Description** |
| v.1 | 20180208 | Initial version |

# 8  Legal information

## 8.1  Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

## 8.2  Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based

on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Evaluation products** — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 8.3  Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

KTPF4210EPEVBUG

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

**User guide**

**Rev. 1.0 — 8 February 2018**

**16 / 18**

## Tables

## Figures

KTPF4210EPEVBUG

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

**User guide**

**Rev. 1.0 — 8 February 2018**

**17 / 18**

# Contents