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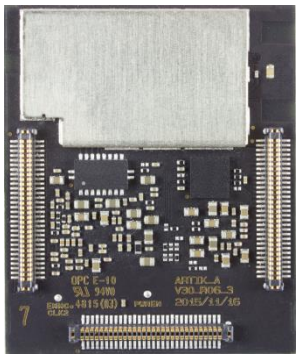
Samsung
ARTIK™

5

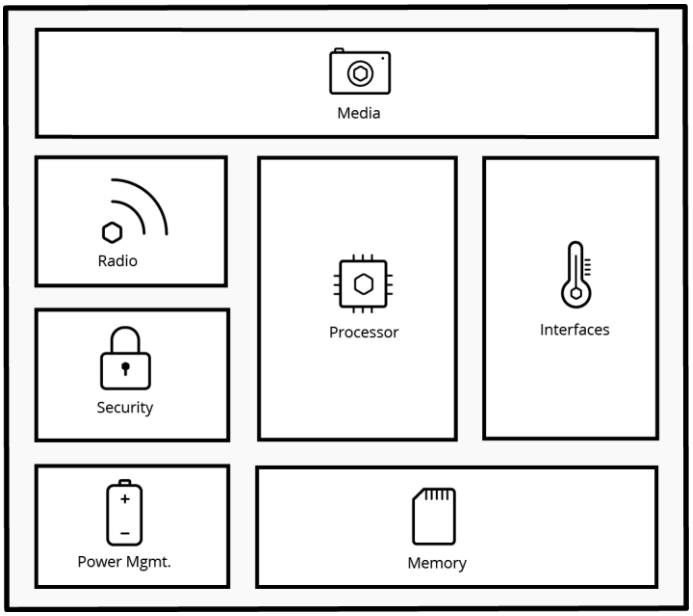
520 Data Sheet

TOP VIEW



BOTTOM VIEW

Samsung's ARTIK™ 520 Module is a highly-integrated System-in-Module that utilizes a dual core ARM® Cortex®-A7 processor packaged DRAM and Flash memories, a Secure Element and a wide range of wireless communication options such as 802.11a/b/g/n/ac, Bluetooth® 4.1, Bluetooth Low Energy (BLE), and 802.15.4/ZigBee® communications all into a 30x25mm footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module capabilities. With the combination of Wi-Fi, Bluetooth and ZigBee the ARTIK 520 Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability with the camera and display options. The hardware based Secure Element works with the ARM TrustZone® and Trustonic's Trusted Execution Environment (TEE) to provide "bank level" security end-to-end.



ARTIK 520 Module Block Diagram

Processor	
CPU	Dual core ARM® Cortex®-A7@1.0GHz
GPU	Mali™-400MP2 core
Media	
Camera I/F	1x 2-Lane MIPI CSI up to 3MP@30fps (Supports YUV and MJPEG format)
Display	2-Lane MIPI DSI up to qHD 960x540@24bpp
Audio	1-channel PCM and 1-channel 24-bit I²S audio interface
Memory	
DRAM	512MB LPDDR3
FLASH	4GB eMMC
Security	
Secure Element	Secure point to point authentication and data transfer
Trusted Execution Environment	Trustonic TEE (NDA required)
Radio	
WLAN	IEEE802.11a/b/g/n/ac
Bluetooth	BT, BLE
IEEE802.15.4	ZigBee
Power Management	
PMIC	Provides all power of the ARTIK 520 module using on board bucks and LDOs
Interfaces	
Analog and Digital I/O	GPIO, I²C, SPI, UART, SDIO, USB 2.0, JTAG, Analog Input

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VERSION HISTORY

Revision	Date	Description	Maturity
1.07	10/19/2016	ARTIK 520 Module Data Sheet	Release

ARTIK 520 Module Block Diagram

Figure 1 shows the functional block diagram of the ARTIK 520 Module. It consists of a dual-core ARM® Cortex®-A7 application processor with 512MB DRAM and 4GB eMMC Flash, PMIC, Secure Element, Wi-Fi/BT chipset, ZigBee chipset, RF connectors and socket-type connectors.

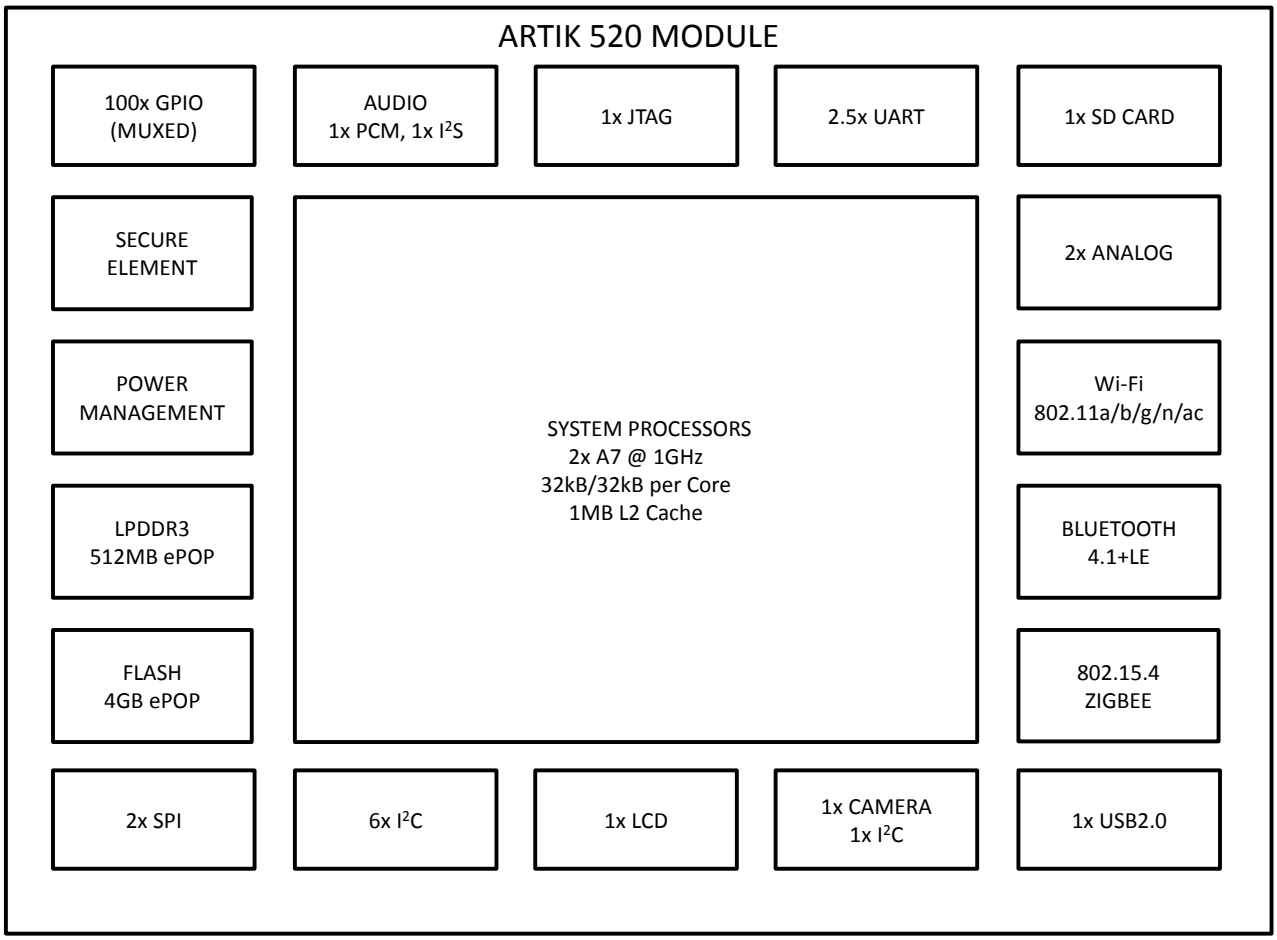

Figure 1. ARTIK 520 Module Functional Block Diagram

The top side is populated with the ARM® application processor, PMIC, Wi-Fi/BT combo chipset and RF connectors for Wi-Fi/BT and ZigBee antenna. The bottom side is populated with the ZigBee chipset, ZigBee front-end for RF and Secure Element, two main connectors for function connection to main set and one debug connector for debug interface connection.

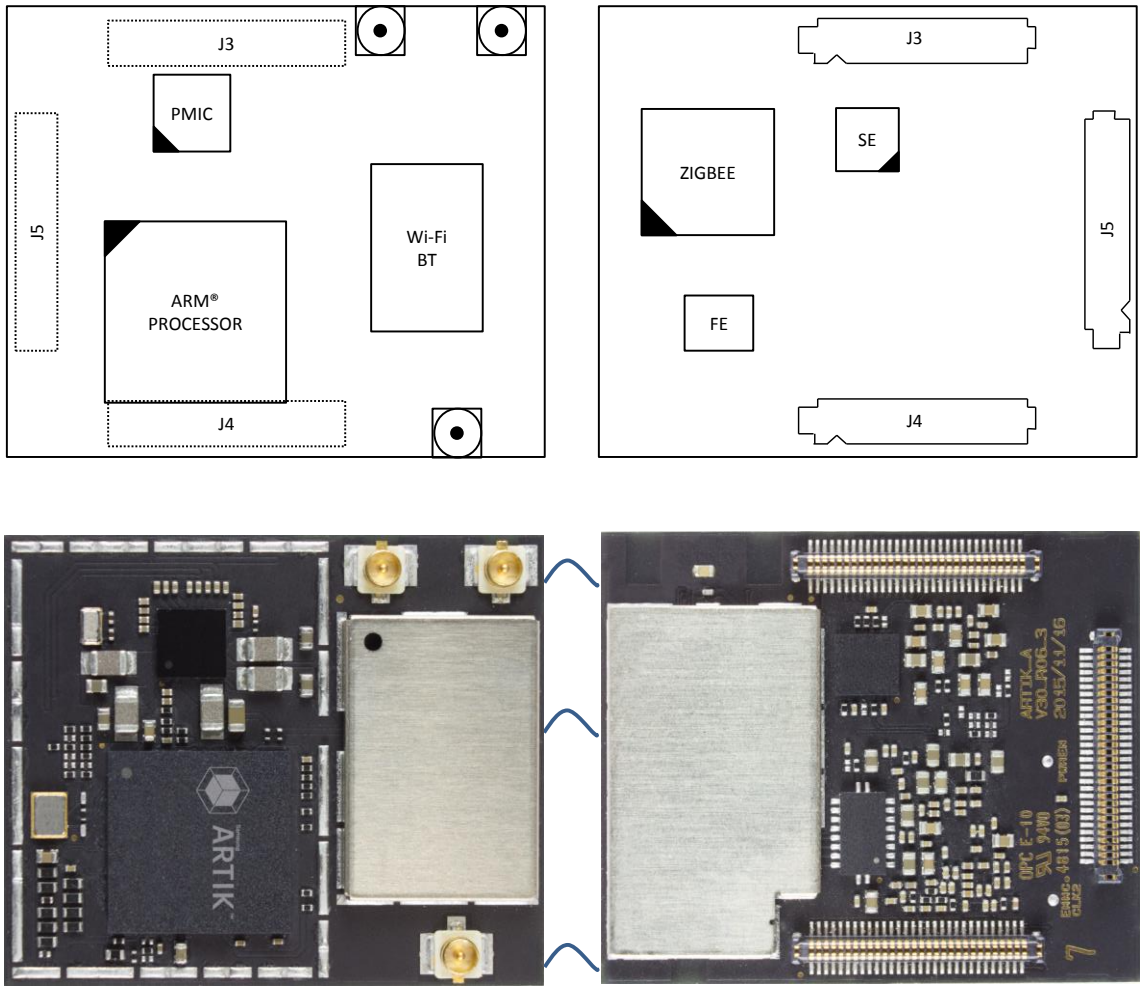

Figure 2. ARTIK 520 Module – Top View / Bottom View

ARTIK 520 Module ZigBee

The ARTIK 520 Module carries a fully-integrated ZigBee unit called the Ember® EM3587. It integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM® Cortex®-M3 microprocessor, flash and RAM memory and peripherals. The most important hardware features of the ZigBee module are:

- Complete system-on-chip using 32-bit ARM® Cortex®-M3 processor.
- Low power consumption:
  - RX current typical 27mA
  - TX current typical 31mA
  - Deep sleep current ≤ 1.25µA
- RF performance:
  - Normal mode link budget up to 110dB
  - RX sensitivity up to 102dBm
- Robust Wi-Fi and Bluetooth coexistence
- Single-voltage operation

For more information on EM3587 contact a sales representative from Silicon Laboratories, Inc.

ARTIK 520 Module ZigBee Front End

The ARTIK 520 Module carries a fully integrated RF Front-End Module (FEM) designed specifically for ZigBee Smart Energy IoT environments. The device provides integrated and fully matched input baluns, an integrated inter-stage matching and harmonic filter, and digital controls compatible with 1.6 to 3.6 V CMOS levels. The RF blocks of the SE2432L support a wide range supply voltage tailored toward battery operated environments. The most important hardware features of the ZigBee front-end are:

- Integrated Power Amplifier up to 24dBm
- Integrated Low-Noise Amplifier with programmable bypass
- Integrated antenna switching, with transmit and receive diversity function
- Low NF, 2dB typical
- Differential transmit/receive interface with integrated baluns
- Fast-switch on/off time ≤ 800ns
- Sleep-mode current ≤ 0.05µA

For more information on SE2432L contact a sales representative from Skyworks Solutions, Inc.

ARTIK 520 Module PMIC

The ARTIK 520 Module has a fully-integrated PMIC containing 5 Bucks and 25 LDOs. This unit provides all power requirements for the ARTIK 520 Module in one compact form factor. In addition, various stable power outputs are offered at the connectors, such that additional customer-defined use cases can be defined and efficiently implemented.

For more information on S2MPS14 contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 520 Module Wi-Fi/Bluetooth

The ARTIK 520 Module has a fully-integrated MIMO combo BCM4354 for IEEE 802.11 a/b/g/n/ac wireless LAN with Bluetooth 4.0+LE and FM. The most important hardware features of the Wireless/Bluetooth combo module are:

- WLAN 802.11ac compliant:
  - Single-stream spatial multiplexing up to 433Mbps
  - Support for 20, 40 and 80 MHz channels with optional SGI (256 QAM modulation)
- WLAN 802.11 a/b/g/n/ac compliant
- Bluetooth 4.0+LE
- 2G and 5G MIMO support
- FM Receiver, 65MHz-108MHz bands

For more information on BCM 4354 contact a sales representative from Broadcom Ltd.

ARTIK 520 Module Secure Element

The ARTIK 520 Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The most important hardware features of the Secure Element are:

- Dedicated secure CPU SC300
- Crypto Accelerator
  - Hardware based AES/DES/3DES
  - TORNADO-E
  - 5KB crypto RAM
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 4128bits/ECC 544 bits
- Data security
  - Abnormal-condition detectors for: reset, interrupt, voltage, temperature, laser exposure, shield removal
  - Random Wait Generator, Random Current Generator
  - Secure optimized layout
  - Dynamic bus encryption
- Embedded tamper-free memory
  - 1.5MB flash (program and data)
  - 32KB MASK ROM
  - 48KB Static RAM
  - 5KB Crypto RAM
  - Memory Protection Unit with 4GB addressable space
  - Secure flash write operation with fast page (0.5ms) and sector erase (4ms)
  - 500K erase/write cycles/s
- Serial interfaces:
  - I^2C/SPI/UART (ISO 7816)
- A guaranteed 25 years data retention at room temperature

For more information on S3FV5RP contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 520 Module Secure JTAG

Our secure JTAG core that is part of the ARTIK 520 Module provides debug capabilities for the developer. The secure JTAG core authenticates the legal user. In addition, it provides an access level that the legal user can operate under. The main features of the secure JTAG core are:

- Dedicated authentication process through password
- Dedicated Hash engine (SHA-1) with hash sequencer
- Two access levels “access-on” and “access-off”
- Industry standard JTAG capabilities

ARTIK 520 Module Processor System

The processor system architecture that resides on the ARTIK 520 Module is a system-on-a-chip (SoC) based on a 32-bit RISC processor. Designed using the 28nm low power process, the processor system architecture provides superior performance using a dual-core CORTEX®-A7 CPU. The ARTIK 520 Module contains 3D graphics hardware, image signal-processor hardware and a variety of high-speed interfaces such as eMMC5.0.

The ARTIK 520 Module contains the dual Cortex®-A7. The ARTIK 520 Module allows for heavy traffic operations such as
720p video encoding/decoding, 3D graphics display and high resolution image signal processing.

The application processor supports dynamic virtual-address mapping aiding software engineers to fully utilize the memory resources. The key features of the ARTIK 520 Module are:

- Dual-core ARM® Cortex®-A7, 32 KB I$/32 KB D$ and 1MB L2 Cache
- 128-bit multi-layer AXI bus architecture
- Internal ROM and RAM for secure booting and general-use purposes
- Memory subsystem:
  - 1-port 32-bit 400MHz LPDDR2/LPDDR3 interface
- Supports 3D and 2D graphics hardware
- LCD single qHD display supports MIPI
- Support for 2-lane MIPI DSI interface
- Support for 2-lane MIPI CSI interface
- Support for 1-channel PCM and 1-channel 24-bit I^2S audio interface
- Support for 6-channel I^2C general-purpose multi-master interface and 1-channel dedicated camera I^2C interface
- Support for 2-channel high-speed SPI interface
- Support for 2.5-channel high-speed UART (up to 3Mbps data rate for Bluetooth 2.1 EDR and IrDA 1.0 SIR)
- Support for USB 2.0, 1-channel supports LS/FS/HS (1.5Mbps/12Mbps/480Mbps) with on-chip PHY
- Support for 2-channel SD/MMC interface supports SDIO3.0, eMMC5.0 DDR with 8-bit interface
- Support for up to 100 configurable GPIO (multiplexed)
- Real time clock, PLLs, timer with PWM, and watchdog timer
- Support for 2-channel (multiplexed) general-purpose ADC

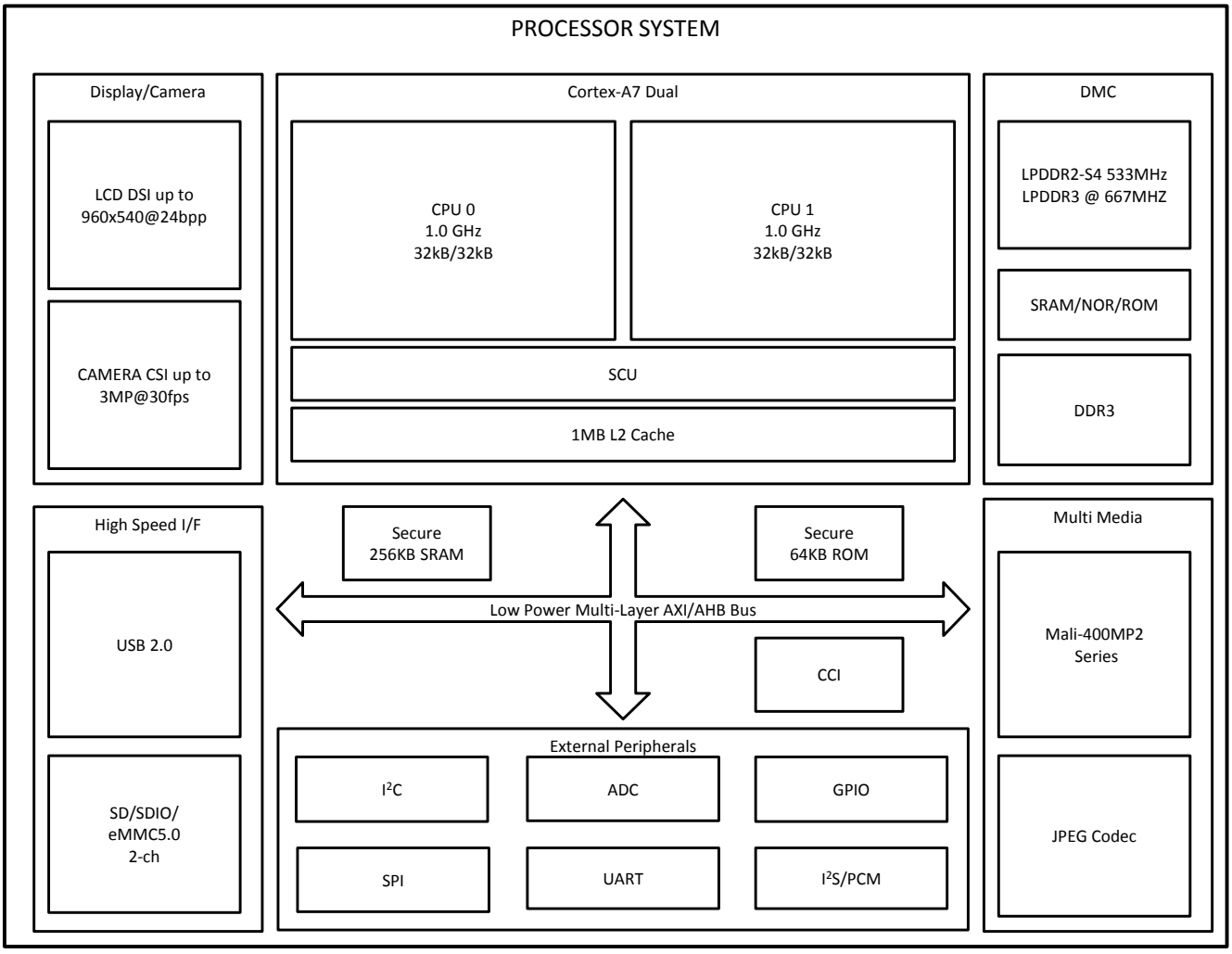

Figure 3. Processor System Block Schematic

MIPI DSI

The ARTIK 520 Module provides 1x 2-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are:

- Maximum resolution ranges up to qHD (960x540@24bpp)
- Supports 1 or 2 data lanes.
- Supported interfaces are:
  - Protocol-to-PHY Interface (PPI) in MIPI D-PHY specification V0.90
  - RGB Interface for video image input from display controller
  - An I80 interface for Command Mode Image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Pre-scaler to generate escape clock from byte clock

MIPI CSI

The ARTIK 520 Module provides 1x 2-lane MIPI interface that complies with the MIPI CSI standard specification V1.01r06. The key features of the MIPI CSI sub-system are:

- Supports 1 or 2 data lanes

- Supports up to 3MP@30fps
- Supported image formats are:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - MJPEG

SPI

The ARTIK 520 Module provides 2x Serial Peripheral Interfaces (SPI) that transfers serial data. SPI support includes
8-bit/16-bit/32-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by National Semiconductor, Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full-duplex
- 8-bit/16-bit/32-bit shift register for Tx and Rx
- 8-bit/16-bit/32-bit bus interface
- Complies with the SPI protocol described by National Semiconductor, Microwire and Motorola
- Support for 2 independent 32-bit wide transmit and receive FIFOs:
  - Depth 64 in SPI port 0 and depth 16 in SPI port 1
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Support Tx/Rx up to 50 MHz

ADC

The ADC interface controls one 28nm low power CMOS 1.8V 12-bit ADC. It converts the analog input signal into 12-bit binary code at a conversion rate of 50kSPS-1MSPS with a 1MHz-20MHz main clock. The ADCIF includes a 12-bit resolution that combines with an analog input multiplexer. The analog input multiplexer selects one from 2 input channels.

UART

The ARTIK 520 Module provides 2x full 4-pin UARTs plus 1x 2-pin UART with just RxD and TxD signals. The key features of the UART sub-system are:

- Both DMA and interrupt based mode of operation supported
- All independent channels support IrDA 1.0
- Each UART channel contains two FIFOs to receive and transmit data:
  - 256 bytes in ch0 and ch2
  - 64 bytes in ch1
  - 16 bytes in ch3
- Each UART channel contains:
  - Programmable baud-rates
  - One or two stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

I^2S

The ARTIK 520 Module provides one 3-line Inter-IC Sound (I^2S) channel. I^2S is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals, such as sub-coding and control.

It is possible to transmit data between two I^2S buses. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used. The key features of the I^2S sub-system are:

- Supports 1-port stereo (1 channel) I^2S-bus for audio with DMA based operation
- Supports serial data transfer of 8/16/24-bit per channel
- Supports I^2S, MSB-justified, and LSB-justified data formats
- Supports both master and slave modes

PCM

The ARTIK 520 Module provides 1x PCM channel. The PCM audio interface provides a bi-directional serial interface
to an external codec. The key features of the PCM sub-system are:

- A 16-bit PCM with 1 port audio interface
- Supports only Master mode
- All PCM serial timings and strobes are extracted from one master clock
- Supports 1x input (16-bit x 32depth) and 1x output (16-bit x 32 depth) FIFO to buffer data
- DMA interface for Tx or Rx or both

GPIO

The ARTIK 520 Module provides a GPIO system to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- Control for up to 91 external interrupts
  - Falling edge triggered
  - Rising edge triggered
  - Both edge triggered
- Control for up to 25 wake-up interrupts
  - Falling edge triggered
  - Rising edge triggered
  - Both edge triggered
- Control for up to 100 General Purpose I/Os
- Controls a variety of pin states in sleep mode

I^2C

The ARTIK 520 Module provides 6x generic 400kb/s I^2C channels + 1x dedicated 400kb/s camera I^2C channel. The key features of the I^2C sub-system are:

- Supporting master and slave mode
- 7-bit addressing mode only
- Supports serial, 8-bit oriented and bi-directional data transfer
- Supports up to 100 kb/s in the standard mode
- Supports up to 400 kb/s in the fast mode
- Supports master transmit, master receive, slave transmit, and slave receive operation
- Supports both interrupt and polling events

USB

The ARTIK 520 Module provides one USB2.0 interface. The key features of the USB2.0 sub-system are:

- In compliance with the USB 2.0 specification revision 1.0a
- In compliance with the UTMI+ Level3 revision 1.0
- Supports high-speed and full-speed transfers
- Supports up to 15 device-programmable endpoints:
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction

- Supports packet-based dynamic FIFO memory allocation up to 7936 depth

SDIO/xMMC

The ARTIK 520 Module provides one SDIO/xMMC interface. The Mobile Storage Host is an interface between the system and SD/MMC card. This host supports 8-bit DDR transfer with a 200 MHz clock rate. The key features of mobile storage host sub-system are:

- Support for Embedded Multimedia Cards (eMMC – version 5.0)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
- Support for Multimedia Cards (MMC – version 4.4)

Mali™-400 Series

The ARTIK 520 Module provides 1x instance of the Mali™-400 GPU series from ARM®. The Mali™-400 series adds graphics capabilities to the ARTIK 520 Module. The key features of the Mali™-400 sub-system are:

- Resolution of 4kx4k for the frame buffer as well as the texture buffer
- Tile-based pixel processing
- Scalable multi-core pixel processors (128 threads)

DMC

The ARTIK 520 Module provides a Dynamic Memory Controller (DMC) that is compatible with the JEDEC standard supporting LPDDR3/DDR3 and SDRAM devices. The following memory interfaces are supported:

- LPDDR2-S4 up to 533MHz
- LPDDR3 up to 667 MHz
- DDR3

Dual Cortex®-A7

The ARTIK 520 Module provides 2xCPU cores which consist of ARM® Cortex®-A7 core processors. For easier and faster CPU core switching, the ARTIK 520 Module supports a cache coherency interconnect (CCI) bus with L2 cache snooping capability. The ARM® Cortex®-A7 dual-core has the following common features:

- Common ARM®v7-A Cortex® architecture
- A core speed up to 1GHZ
- Security Extensions for implementation of enhanced security
- Virtualization Extensions for the development of virtualized systems that enable switching guest operation systems
- Program Trace Macrocell that is ARM CoreSight compatible
- Multi-core ARM TrustZone® technology

ARTIK 520 Module Connectors

The ARTIK 520 Module utilizes three 60-position connectors for all power, analog and digital I/O. Connectors J3, J4 and J5 are Panasonic ATX460124 with 60 pins and 0.4mm pitch. *Figure 4* shows the power/signal name assigned to each pin of each connector. *Table 1*, *Table 2* and *Table 3* describe the pinout in detail.

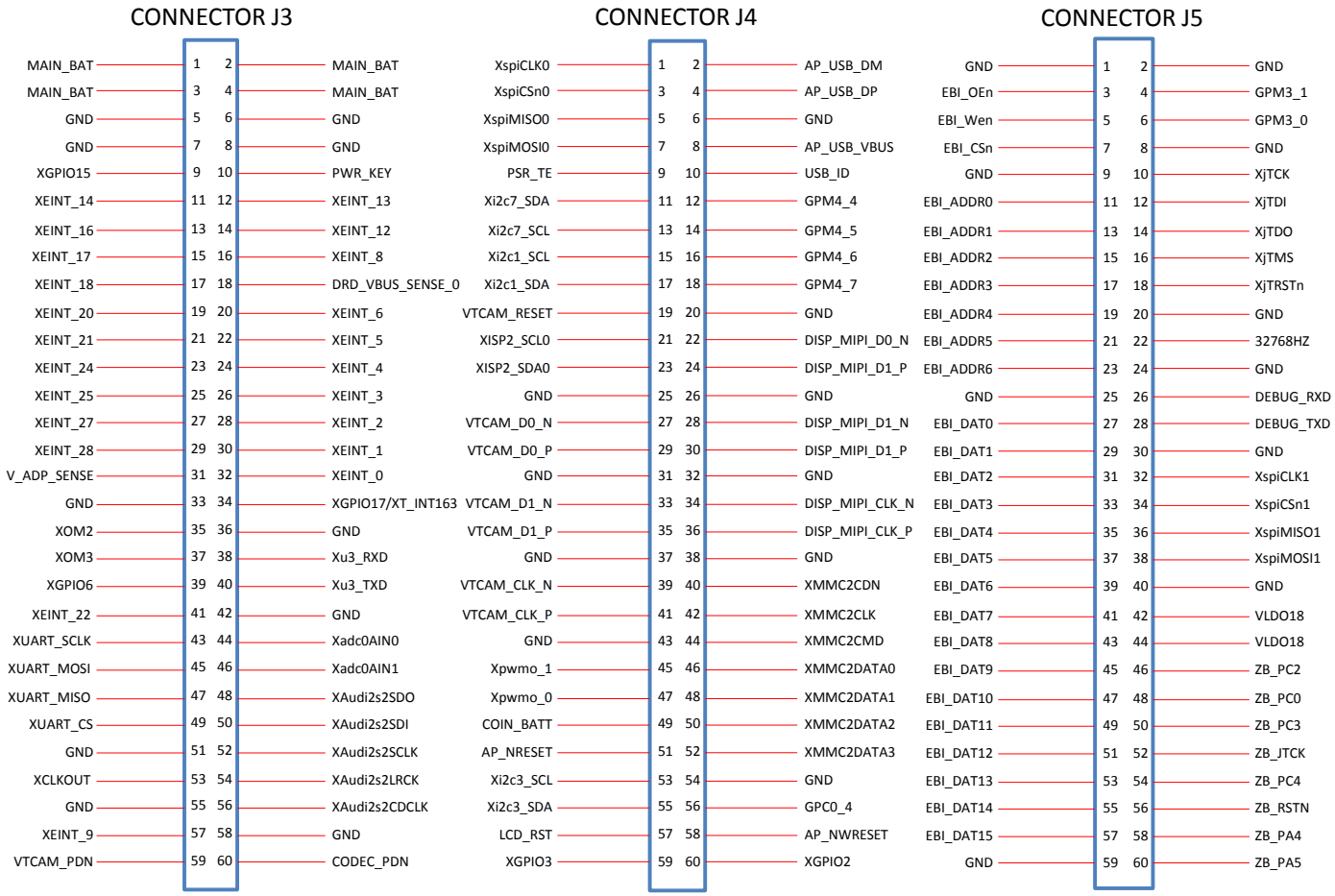

Figure 4. ARTIK 520 Module Connectors

CONNECTOR J3

Table 1. Connector J3

Connector J3									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD*	Group	Function
J3	1	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	3	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	5	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	7	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	9	XGPIO15	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip GPIO1
J3	11	XEINT_14	I	A	1V8	2	PUE	ARDUINO	General purpose interrupt or IO
J3	13	XEINT_16	I	A	1V8	2	PUD D	ETHERNET CONTROLLER	External chip IRQ
J3	15	XEINT_17	I	A	1V8	2	PUD D	POWER/RESET	Charge status interrupt
J3	17	XEINT_18	I	A	1V8	2	PUD D	UART	SPI-TO-UART IC for SPI bus emulation RESET
J3	19	XEINT_20	I	A	1V8	2	PUD D	UART	SPI-TO-UART IC for SPI bus emulation IRQ
J3	21	XEINT_21	O	A	1V8	2	PUD D	LCD	Backlight enable
J3	23	XEINT_24	I	A	1V8	2	PDE	POWER/RESET	Turn device on
J3	25	XEINT_25	I	A	1V8	2	PDE	POWER/RESET	Fuel gauge interrupt
J3	27	XEINT_27	I	A	1V8	2	PDE	AUDIO	Ear microphone detect
J3	29	XEINT_28	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip CS
J3	31	V_ADP_SENSE	I	A/SE	1V8	2	PDE	POWER/RESET	AC Power detect
J3	33	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	35	XOM2	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	37	XOM3	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	39	XGPIO6	I	A	1V8	2	PDE	ZWAVE	SD3503 ZWAVE reset
J3	41	XEINT_22	I	A	1V8	2	PUD D	CAMERA	27MHz osc enable
J3	43	XUART_SCLK	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation SCLK
J3	45	XUART_MOSI	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MOSI
J3	47	XUART_MISO	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MISO
J3	49	XUART_CS	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation CS
J3	51	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	53	XCLKOUT	O	PROCESSOR	1V8	NA	NA	AUDIO	Clock
J3	55	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	57	XEINT_9	I	A	1V8	2	PDE	ETHERNET CONTROLLER	General purpose interrupt or IO
J3	59	VTCAM_PDN	I	A	1V8	2	PDE	CAMERA	Power down
J3	2	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	4	MAIN_BAT	NA	NA	3V8	NA	NA	NA	Main battery
J3	6	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	8	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	10	PWR_KEY	I	PMIC	NA	NA	NA	POWER/RESET	PMIC power on key

Connector J3									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD*	Group	Function
J3	12	XEINT_13	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	14	XEINT_12	I	A	1V8	2	PDE	SIGFOX	Low power wireless transmitter reset
J3	16	XEINT_8	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	18	DRD_VBUS_SENSE_0	I	A	1V8	2	PDE	USB	Device detect
J3	20	XEINT_6	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	22	XEINT_5	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	24	XEINT_4	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	26	XEINT_3	I	A	1V8	2	PUE	ARDUINO	General purpose interrupt or IO
J3	28	XEINT_2	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	30	XEINT_1	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	32	XEINT_0	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO
J3	34	XGPIO17/XT_INT163	I	A	1V8	2	PDE	POWER/RESET	External IC interrupt
J3	36	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	38	Xu3_RXD	I	A	1V8	2	PUDD	ARDUINO	RxD
J3	40	Xu3_TXD	I	A	1V8	2	PUDD	ARDUINO	TxD
J3	42	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	44	Xadc0AIN0	I	ADC	1V8	NA	NA	ARDUINO	Input 0
J3	46	Xadc0AIN1	I	ADC	1V8	NA	NA	ARDUINO	Input 1
J3	48	XAudi2s2SDO	I	A	1V8	2	PDE	AUDIO	SDO
J3	50	XAudi2s2SDI	I	A	1V8	2	PDE	AUDIO	SDI
J3	52	XAudi2s2SCLK	I	A	1V8	2	PDE	AUDIO	SCLK
J3	54	XAudi2s2LRCK	I	A	1V8	2	PDE	AUDIO	LRCLK
J3	56	XAudi2s2CDCLK	I	A	1V8	2	PDE	AUDIO	CDCLK
J3	58	GND	NA	NA	0V0	NA	NA	NA	Ground
J3	60	CODEC_PDN	I	A	1V8	2	PDE	AUDIO	AK4953EQ audio codec IC power down

* The PUD variables have the following meaning: PUDD = Power Up Down Disabled, PDE = Power Down Enabled, PUE = Power Up Enabled, R = Reserved.

CONNECTOR J4

Table 2. Connector J4

Connector J4									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J4	1	XspiCLK0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI CLK
J4	3	XspiCSn0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI CSn
J4	5	XspiMISO0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI MISO
J4	7	XspiMOSI0	I	A	1V8	2	PDE	ETHERNET CONTROLLER/SIGFOX	SPI MOSI
J4	9	PSR_TE	I	A	1V8	2	PDE	LCD	CLK
J4	11	Xi2c7_SDA	I	A	1V8	2	PDE	ARDUINO	General purpose I2C SDA
J4	13	Xi2c7_SCL	I	A	1V8	2	PDE	ARDUINO	General purpose I2C SCL
J4	15	Xi2c1_SCL	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SCL
J4	17	Xi2c1_SDA	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SDA
J4	19	VTCAM_RESET	O	A	1V8	2	PDE	CAMERA	RESET Camera
J4	21	XISP2_SCL0	I	A	1V8	2	PDE	CAMERA	I2C SCL
J4	23	XISP2_SDA0	I	A	1V8	2	PDE	CAMERA	I2C SDA
J4	25	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	27	VTCAM_D0_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_N
J4	29	VTCAM_D0_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_P
J4	31	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	33	VTCAM_D1_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_N
J4	35	VTCAM_D1_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_P
J4	37	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	39	VTCAM_CLK_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_N
J4	41	VTCAM_CLK_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_P
J4	43	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	45	Xpwmo_1	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO or PWM
J4	47	Xpwmo_0	I	A	1V8	2	PDE	ARDUINO	General purpose interrupt or IO or PWM
J4	49	COIN_BAT	NA	PMIC	3V0	NA	NA	POWER/RESET	Backup battery
J4	51	AP_NRESET	I	PROCESSOR/PMIC	1V8	NA	NA	POWER/RESET/ ARDUINO/JTAG	ARTIK 520 Module reset
J4	53	Xi2c3_SCL	I	A	1V8	2	PUDD	TEST POINTS	I2C SCL
J4	55	Xi2c3_SDA	I	A	1V8	2	PUDD	TEST POINTS	I2C SDA
J4	57	LCD_RST	O	A	1V8	2	PDE	LCD	Reset
J4	59	XGPIO3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External Chip GPIO0
J4	2	AP_USB_DM	I/O	USB2.0	3V0	NA	NA	USB	USB DM
J4	4	AP_USB_DP	I/O	USB2.0	3V0	NA	NA	USB	USB DP
J4	6	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	8	AP_USB_VBUS	I/O	USB2.0	3V0	NA	NA	USB	USB VBUS
J4	10	USB_ID	I	USB2.0	3V0	NA	NA	USB	ID
J4	12	GPM4_4	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	14	GPM4_5	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	16	GPM4_6	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	18	GPM4_7	I	A	1V8	2	PDE	SIGFOX	ATA8520 SPI bus emulation
J4	20	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	22	DISP_MIPI_D0_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_N

Connector J4									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J4	24	DISP_MIPI_D0_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_P
J4	26	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	28	DISP_MIPI_D1_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_N
J4	30	DISP_MIPI_D1_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_P
J4	32	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	34	DISP_MIPI_CLK_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_N
J4	36	DISP_MIPI_CLK_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_P
J4	38	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	40	XMMC2CDN	I	B	1V8	4	PUE	SD CARD	XMMC2 CDN
J4	42	XMMC2CLK	O	B	1V8	12	PUDD	SD CARD	XMMC2 CLK
J4	44	XMMC2CMD	O	B	1V8	12	PUDD	SD CARD	XMMC2 CMD
J4	46	XMMC2DATA0	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA0
J4	48	XMMC2DATA1	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA1
J4	50	XMMC2DATA2	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA2
J4	52	XMMC2DATA3	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA3
J4	54	GND	NA	NA	0V0	NA	NA	NA	Ground
J4	56	GPC0_4	I	A	1V8	2	PDE	LCD	Identification (ID)
J4	58	AP_NWRESET	I	PROCESSOR/PMIC	1V8	NA	NA	PMIC	Warm reset from PMIC (development purposes)
J4	60	XGPIO2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip reset

CONNECTOR J5

Table 3. Connector J5

Connector J5									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J5	1	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	3	EBI_OEn	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip RDN
J5	5	EBI_Wen	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip WRN
J5	7	EBI_CSn	I	A	1V8	2	PDE	ETHERNET CONTROLLER	CS 1 default connect
J5	9	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	11	EBI_ADDR0	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR0
J5	13	EBI_ADDR1	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR1
J5	15	EBI_ADDR2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR2
J5	17	EBI_ADDR3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR3
J5	19	EBI_ADDR4	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR4
J5	21	EBI_ADDR5	I	A	1V8	2	PDE	ETHERNET CONTROLLER	External chip EBI_ADDR5
J5	23	EBI_ADDR6	I	A	1V8	2	PDE	NA	Not used
J5	25	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	27	EBI_DAT0	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 0
J5	29	EBI_DAT1	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 1
J5	31	EBI_DAT2	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 2
J5	33	EBI_DAT3	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 3
J5	35	EBI_DAT4	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 4
J5	37	EBI_DAT5	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 5
J5	39	EBI_DAT6	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 6
J5	41	EBI_DAT7	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 7
J5	43	EBI_DAT8	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 8
J5	45	EBI_DAT9	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 9
J5	47	EBI_DAT10	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 10
J5	49	EBI_DAT11	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 11
J5	51	EBI_DAT12	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 12
J5	53	EBI_DAT13	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 13
J5	55	EBI_DAT14	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 14
J5	57	EBI_DAT15	I	A	1V8	2	PDE	ETHERNET CONTROLLER	EBI BUS DATA 15
J5	59	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	2	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	4	GPM3_1	I	A	1V8	2	PDE	TEST POINTS	Not used
J5	6	GPM3_0	I	A	1V8	2	PDE	TEST POINTS	Not used
J5	8	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	10	XjTCK	I	JTAG	1V8	NA	NA	JTAG	JTAG CLK
J5	12	XjTDI	I	JTAG	1V8	NA	NA	JTAG	JTAG TDI
J5	14	XjTDO	O	JTAG	1V8	NA	NA	JTAG	JTAG TDO
J5	16	XjTMS	I	JTAG	1V8	NA	NA	JTAG	JTAG TMS
J5	18	XjTRSTn	I	JTAG	1V8	NA	NA	JTAG	JTAG RSTn
J5	20	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	22	32768HZ	O	PROCESSOR/PMIC/BT	1V8	NA	NA	TEST POINTS	32 KHz clock
J5	24	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	26	DEBUG_RXD	I	A	1V8	2	PUDD	DEBUG	AP debug UART RxD
J5	28	DEBUG_TXD	I	A	1V8	2	PUDD	DEBUG	AP debug UART TxD
J5	30	GND	NA	NA	0V0	NA	NA	NA	Ground

Connector J5									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J5	32	XspiCLK1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI CLK
J5	34	XspiCSn1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI CSn
J5	36	XspiMISO1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI MISO
J5	38	XspiMOSI1	O	A/SE	1V8	2	PDE	TEST POINTS	SPI MOSI
J5	40	GND	NA	NA	0V0	NA	NA	NA	Ground
J5	42	VLDO18	NA	NA	2V8	NA	NA	JTAG	2.8V/300mA
J5	44	VLDO18	NA	NA	2V8	NA	NA	JTAG	2.8V/300mA
J5	46	ZB_PC2	O	ZIGBEE	1V8	NA	NA	JTAG	JTAG data out
J5	48	ZB_PC0	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG reset
J5	50	ZB_PC3	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG data in
J5	52	ZB_JTCK	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG clock
J5	54	ZB_PC4	I	ZIGBEE	1V8	NA	NA	JTAG	JTAG mode select
J5	56	ZB_RSTn	O	ZIGBEE/LS	1V8	2	PDE	JTAG	JTAG reset
J5	58	ZB_PA4	I/O	ZIGBEE	1V8	NA	NA	JTAG	JTAG GPIO
J5	60	ZB_PA5	I/O	ZIGBEE/LS	1V8	NA	NA	JTAG	JTAG GPIO

ARTIK 520 Module Functional Interfaces

This section shows the functional interfaces that are available at the connectors. Since some of the functionality is spread over multiple connectors, these tables will help provide better insight into what functionality is located where. The functions provided are related to the development environment used. Depending on your project you can always choose to reprogram some of the GPIOs that are currently assigned to the functional interfaces as described below.

USB

Table 4. USB

USB									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	18	DRD_VBUS_SENSE_0	I	A	1V8	2	PDE	USB	Device detect
J4	2	AP_USB_DM	I/O	USB2.0	3V0	NA	NA	USB	USB DM
J4	4	AP_USB_DP	I/O	USB2.0	3V0	NA	NA	USB	USB DP
J4	8	AP_USB_VBUS	I/O	USB2.0	3V0	NA	NA	USB	USB VBUS
J4	10	USB_ID	I	USB2.0	3V0	NA	NA	USB	ID

Audio Codec

Table 5. Audio Codec

Audio Codec									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	27	XEINT_27	I	A	1V8	2	PDE	AUDIO	Ear microphone detect
J3	53	XCLKOUT	O	PROCESSOR	1V8	NA	NA	AUDIO	Clock
J3	48	XAudi2s2SDO	I	A	1V8	2	PDE	AUDIO	SDO
J3	50	XAudi2s2SDI	I	A	1V8	2	PDE	AUDIO	SDI
J3	52	XAudi2s2SCLK	I	A	1V8	2	PDE	AUDIO	SCLK
J3	54	XAudi2s2LRCK	I	A	1V8	2	PDE	AUDIO	LRCLK
J3	56	XAudi2s2CDCLK	I	A	1V8	2	PDE	AUDIO	CDCLK
J3	60	CODEC_PDN	I	A	1V8	2	PDE	AUDIO	AK4953EQ audio codec IC power down
J4	15	Xi2c1_SCL	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SCL
J4	17	Xi2c1_SDA	I	A	1V8	2	PDE	AUDIO/POWER/RESET	I2C SDA

UARTS

Table 6. UARTS

UARTS									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	17	XEINT_18	I	A	1V8	2	PUDD	UARTS	SPI-TO-UART IC for SPI bus emulation RESET
J3	19	XEINT_20	I	A	1V8	2	PUDD	UARTS	SPI-TO-UART IC for SPI bus emulation IRQ
J3	43	XUART_SCLK	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation SCLK
J3	45	XUART_MOSI	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MOSI
J3	47	XUART_MISO	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation MISO
J3	49	XUART_CS	I	A	1V8	2	PDE	UARTS	SPI-TO-UART IC for SPI bus emulation CS

CAMERA

Table 7. Camera

Camera									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	41	XEINT_22	I	A	1V8	2	PUDD	CAMERA	27MHz osc enable
J3	59	VTCAM_PDN	I	A	1V8	2	PDE	CAMERA	Power down
J4	19	VTCAM_RESET	O	A	1V8	2	PDE	CAMERA	RESET Camera
J4	21	XISP2_SCL0	I	A	1V8	2	PDE	CAMERA	I2C SCL
J4	23	XISP2_SDA0	I	A	1V8	2	PDE	CAMERA	I2C SDA
J4	27	VTCAM_D0_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_N
J4	29	VTCAM_D0_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D0_P
J4	33	VTCAM_D1_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_N
J4	35	VTCAM_D1_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI D1_P
J4	39	VTCAM_CLK_N	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_N
J4	41	VTCAM_CLK_P	I/O	MIPI	1V0	NA	NA	CAMERA	MIPI CLK_P

SD CARD

Table 8. SD Card

SD Card									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J4	40	XMMC2CDN	I	B	1V8	4	PUE	SD CARD	XMMC2 CDN
J4	42	XMMC2CLK	O	B	1V8	12	PUDD	SD CARD	XMMC2 CLK
J4	44	XMMC2CMD	O	B	1V8	12	PUDD	SD CARD	XMMC2 CMD
J4	46	XMMC2DATA0	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA0
J4	48	XMMC2DATA1	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA1
J4	50	XMMC2DATA2	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA2
J4	52	XMMC2DATA3	I	B	1V8	12	PUE	SD CARD	XMMC2 DATA3

POWER/RESET

Table 9. Power/Reset

Power/Reset									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	15	XEINT_17	I	A	1V8	2	PUDD	POWER/RESET	Charge status interrupt
J3	23	XEINT_24	I	A	1V8	2	PDE	POWER/RESET	Turn device on
J3	25	XEINT_25	I	A	1V8	2	PDE	POWER/RESET	Fuel gauge interrupt
J3	31	V_ADP_SENSE	I	A/SE	1V8	2	PDE	POWER/RESET	AC Power detect
J3	35	XOM2	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	37	XOM3	I	NA	1V8	NA	NA	POWER/RESET	SD/MMC or eMMC boot
J3	10	PWR_KEY	I	PMIC	NA	NA	NA	POWER/RESET	PMIC power on key
J3	34	XGPIO17/XT_INT163	I	A	1V8	2	PDE	POWER/RESET	External IC interrupt
J4	49	COIN_BAT	NA	PMIC	3V0	NA	NA	POWER/RESET	Backup battery
J4	51	AP_NRESET	I	PROCESSOR/ PMIC	1V8	NA	NA	POWER/RESET/ ARDUINO/JTAG	ARTIK 520 Module reset

LCD

Table 10. LCD

LCD									
Conn#	Pin#	Name	I/O	I/O Type	Voltage	DS [mA]	PUD	Group	Function
J3	21	XEINT_21	O	A	1V8	2	PUDD	LCD	Backlight enable
J4	9	PSR_TE	I	A	1V8	2	PDE	LCD	CLK
J4	57	LCD_RST	O	A	1V8	2	PDE	LCD	Reset
J4	22	DISP_MIPI_D0_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_N
J4	24	DISP_MIPI_D0_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D0_P
J4	28	DISP_MIPI_D1_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_N
J4	30	DISP_MIPI_D1_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI D1_P
J4	34	DISP_MIPI_CLK_N	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_N
J4	36	DISP_MIPI_CLK_P	I/O	MIPI	1V0	NA	NA	LCD	MIPI CLK_P
J4	56	GPC0_4	I	A	1V8	2	PDE	LCD	Identification (ID)