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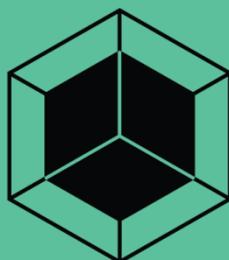
SAMSUNG
ARTIK™ Modules

7

710 Datasheet

ARTIK 710 Module Top View

Samsung's ARTIK[TM] 710 Module is a highly-integrated System-in-Module that utilizes an octa-core ARM® Cortex®-A53 processor packaged DRAM and Flash memory, a hardware Secure Element and a wide range of wireless communication options such as 802.11a/b/g/n/ac, Bluetooth® 4.1 (Classic+BLE), and 802.15.4 (ZigBee® or Thread) communications all into an extremely compact footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module's capabilities. With the combination of Wi-Fi, Bluetooth, ZigBee/Thread, the ARTIK 710 Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability with the camera and display support options. The hardware based Secure Element works with the ARM® TrustZone® and Trustware's Trusted Execution Environment (TEE) to provide enhanced end-to-end security.
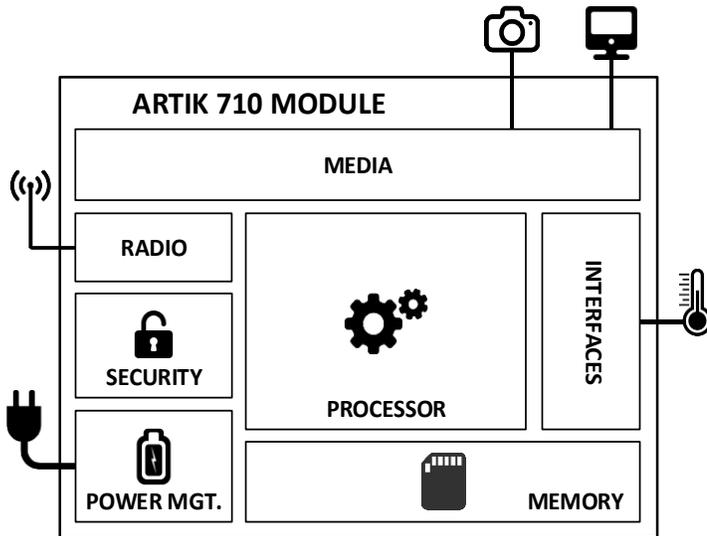
ARTIK 710 Module Block Diagram

Processor	
CPU	8x ARM® Cortex®-A53@1.4GHz
GPU	3D graphics accelerator
Media	
Camera I/F	4-Lane MIPI CSI
Display	4-Lane MIPI DSI up to FHD@24bpp
Audio	I^2S audio interface
Memory	
DRAM	1GB DDR3 @ 800MHz
FLASH	4GB eMMC
Security	
Secure Element	Secure point to point authentication and data transfer
Trusted Execution Environment	Trustware
Radio	
WLAN	IEEE 802.11a/b/g/n/ac
Bluetooth	4.1 (Classic+BLE)
802.15.4	ZigBee/Thread
Power Management	
PMIC	Provides all power of the ARTIK 710 Module using on board bucks and LDOs
Interfaces	
Analog and Digital I/O	GPIO, I^2C, SPI, UART, SDIO, USB 2.0, JTAG, Analog Input

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

VERSION HISTORY

Revision	Date	Description	Maturity
V1.0	October 17, 2016	ARTIK 710 datasheet.	Release
V1.01	November 15, 2016	Updated Page 1 ARTIK 710 Module Picture. Updated Figure 2, Figure 3. Updated Mechanical Specification section. Updated Front Page. Updated ARTIK 710 Module ZigBee or Thread section. Updated ARTIK 710 Module Wi-Fi/Bluetooth section.	Release Update

ARTIK 710 MODULE BLOCK DIAGRAM AND COMPONENT PLACEMENT

Figure 1 shows the functional block diagram of the ARTIK 710 Module. It consists of an octa-core ARM® Cortex®-A53 application processor with 1GB of DDR3 and 4GB eMMC Flash, PMIC power management SoC, Secure Element, Wi-Fi/BT chipset, ZigBee/Thread chipset and RF connectors.
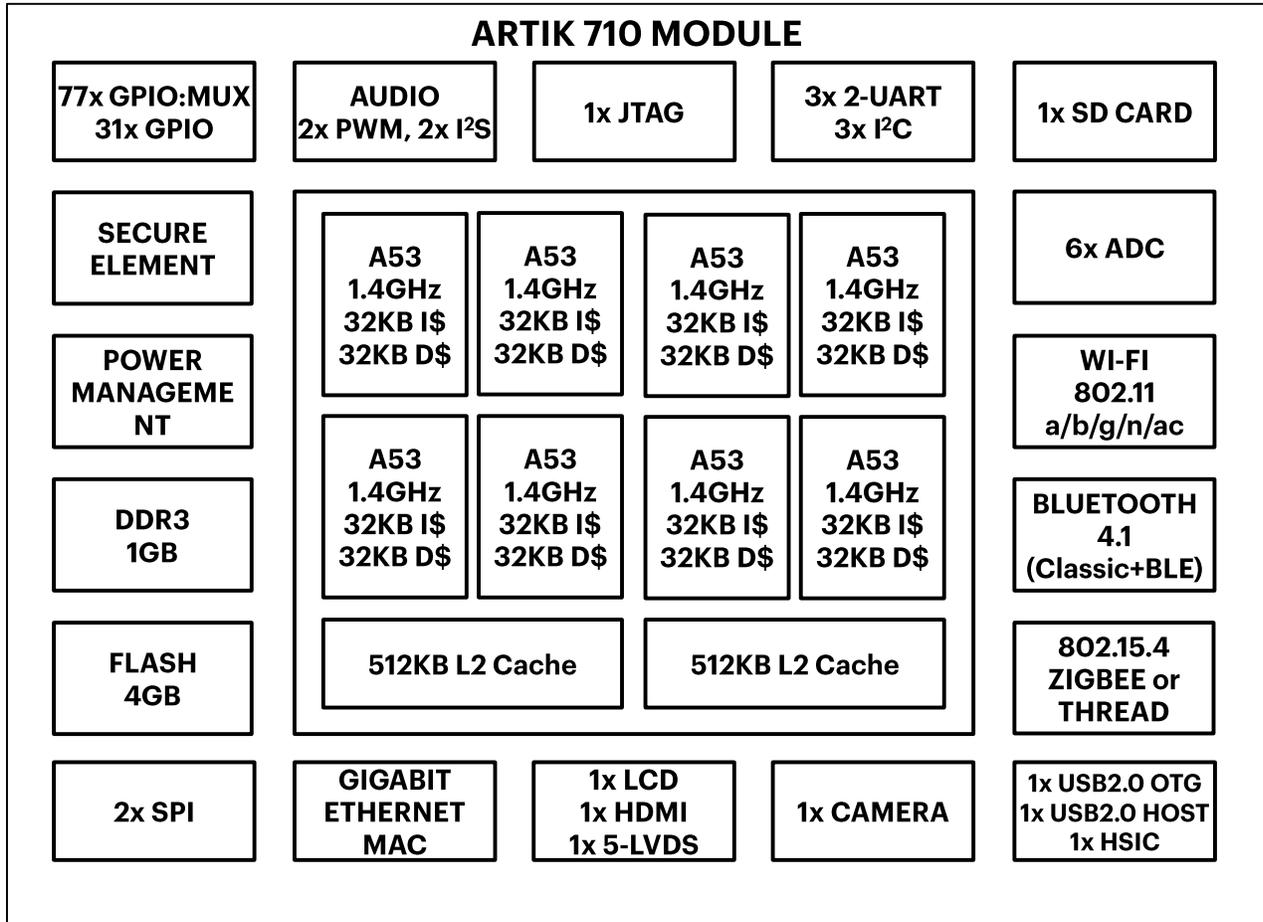
Figure 1. ARTIK 710 Module Functional Block Diagram

Figure 2 shows the Top View with component placement of the ARTIK 710 Module. The top side of the ARTIK 710 Module is populated with the octa-core ARM® A53 application processor, 2x 512MB of DDR3 memory chips, PMIC power manager, Wi-Fi/BT combo chipset, 4GB of Flash, 802.15.4 chipset to support ZigBee or Thread, PA and RF connectors for Wi-Fi/BT and 802.15.4 antennas. In addition _Figure 3_ shows the front and back of the certified ARTIK 710 Module.
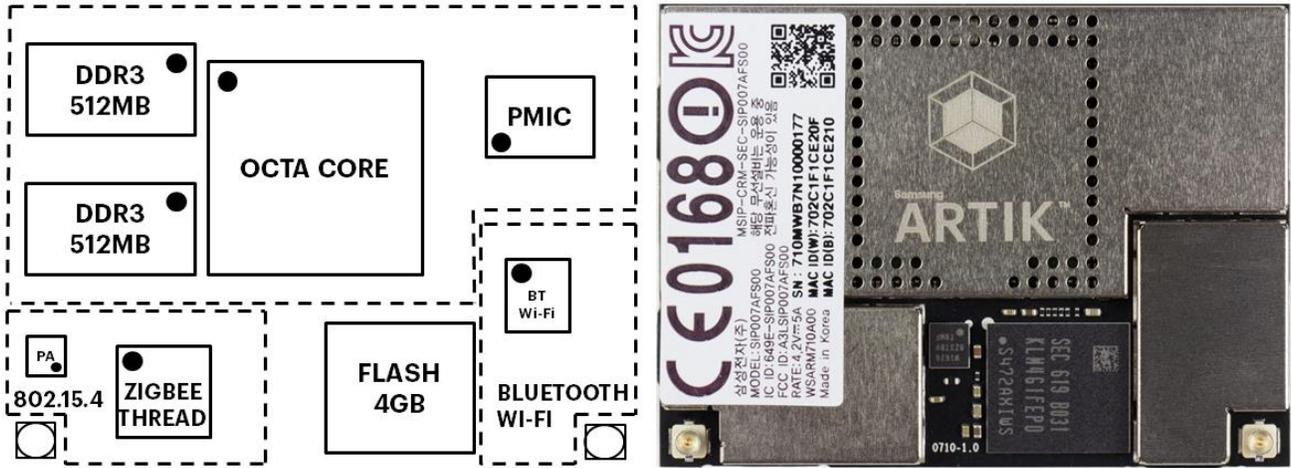
Figure 2. ARTIK 710 Module Component Placement - Top View
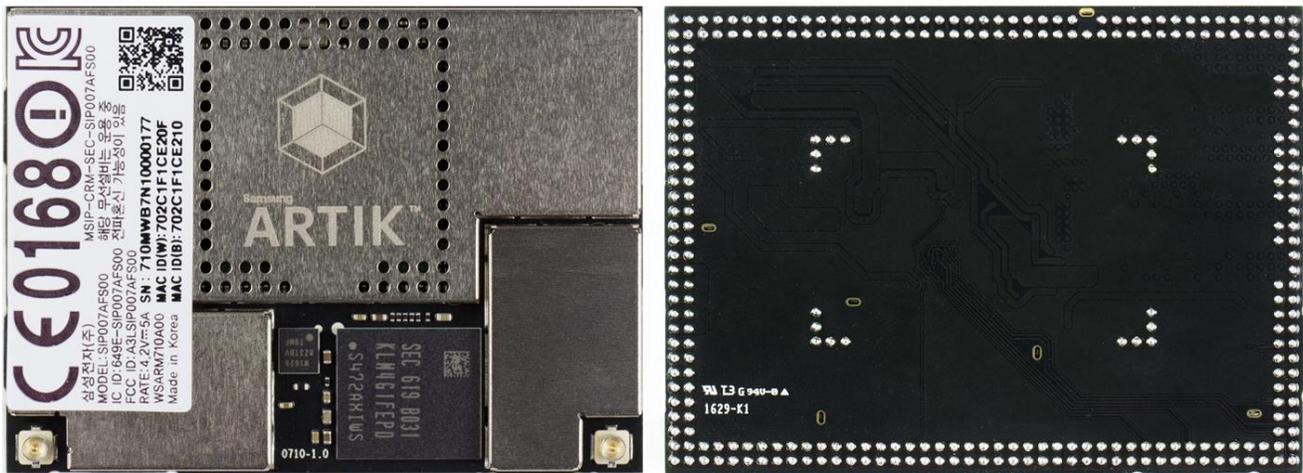
Figure 3. Front and Back of the certified ARTIK 710 Module

ARTIK 710 MODULE ZIGBEE OR THREAD

The ARTIK 710 Module carries a fully-integrated 802.15.4 device. It integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM® Cortex®-M3 microprocessor, flash and RAM memory and peripherals. The most important hardware features of the ZigBee or Thread module are:

- Complete system-on-chip using 32-bit ARM® Cortex®-M3 processor.
- Single-voltage operation

ARTIK 710 MODULE 802.15.4 FRONT END

The ARTIK 710 Module carries a fully integrated RF Front-End Module (FEM) designed specifically for low power sensitive IoT environments. The most important hardware features of the front-end are:

- Combined Tx/Rx transceiver port and single antenna port
- 2.4GHz high power amplifier with low pass harmonic filter
- Low noise amplifier
- Transmit/Receive switch
- Integrated power detector monitoring and controlling transmit power
- CMOS control logic
- 50Ω input output matching

ARTIK 710 MODULE MEMORY

The ARTIK 710 Module has 2x 512MB DDR3 memory chips running at 800MHz each. In addition the ARTIK 710 module has 1x 4GB eMMC Flash memory chip based on the JEDEC MMC 4.51/5.0 standard. The interface speed varies from 200MB/s using MMC4.51 to 400MB/s when using the MMC5.0 standard.

ARTIK 710 MODULE PMIC

The ARTIK 710 Module has a fully-integrated PMIC containing 5 High efficiency DC-DC converters and 10 LDOs. This unit provides all power requirements for the ARTIK 710 Module in one compact form factor. In addition, various stable power outputs are offered at the connectors, such that additional customer-defined use cases can be defined and efficiently implemented.

ARTIK 710 MODULE WI-FI/BLUETOOTH

The ARTIK 710 Module has a fully-integrated IEEE 802.11a/b/g/n/ac MAC baseband radio, Bluetooth 4.1 and an FM receiver. The most important hardware features of the Wireless LAN/Bluetooth combo SoC are:

- IEEE802.11 Features
  - WLAN 802.11ac compliant:
    - Single-stream spatial multiplexing up to 433Mbps
    - Support for 20, 40 and 80 MHz channels including 256 QAM
  - Supports explicit 802.11ac transmit beamforming
  - On chip PA for both bands
- Bluetooth Features
  - Support v4.1 with provisions to support future specifications
  - Bluetooth Class 1 or Class 2 transmitter operation
  - Support for Adaptive Frequency Hopping (reduce interference)
    - Using a 4-wire UART interface

ARTIK 710 MODULE SECURE ELEMENT

The ARTIK 710 Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The Secure Element provides an ISO/IEC 7816 14443 compliant interface. The most important hardware features of the Secure Element are:

- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 2080bits
  - ECC 512 bits
- Data security
  - Memory encryption for all memory
  - 256B read only and 256B non erasable flash area
  - Selective reset operation if abnormal voltages/frequencies are detected
- Embedded tamper-free memory
  - 32KB ROM
  - 264KB FLASH
  - 8.5KB Static RAM including 2.5KB crypto memory
- Serial interfaces:
  - ISO 7816-3 compliant interface
  - Asynchronous half-duplex character receive/transmit serial interface

ARTIK 710 MODULE SECURE JTAG

Our secure JTAG core that is part of the ARTIK 710 Module provides debug capabilities for the developer. The secure JTAG core has an authentication, authorization and an access provider module to assure that only authorized developers have access to the hardware. The main features of the secure JTAG core are:

- Dedicated authentication process through password mechanism
- Dedicated Hash engine with hash sequencer
- Industry standard JTAG capabilities

ARTIK 710 MODULE PROCESSOR SYSTEM

The processor system architecture that resides on the ARTIK 710 Module is a system-on-a-chip (SoC) based on a dual 32/64-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using an octa-core CORTEX®-A53 CPU. The ARTIK 710 Module contains 3D graphics hardware, image signal-processor hardware and a variety of high-speed interfaces such as eMMC5.0.

The ARTIK 710 Module allows for heavy traffic operations with a bandwidth up to 7.4GB/s such as 1080p video encoding and decoding, 3D graphics display and high resolution image signal processing with full HD display.

The application processor supports dynamic virtual-address mapping aiding software engineers to fully utilize the memory resources. The ARTIK 710 Module provides 3D graphics performance with a wide range of APIs such as OpenGL® ES1.1 and 2.0. The key features of the ARTIK 710 Module are:

- Octa-core ARM® Cortex®-A53 with 32KB I\$/32KB D\$ per core and shared 2x 512KB (per 4x cores) L2 Cache
- Memory subsystem:
  - DDR3 up to 800MHz
  - MLC/SLC NAND Flash support with hardwired ECC
- Supports 2D and 3D graphics hardware with OpenGL ES 1.1 and 2.0 software API
- Supports dual display up to 1920x1080 with TFT-LCD, LVDS, HDMI 1.4a and MIPI-DSI output
- Supports 10/100/1000M Ethernet MAC
- Supports a wide variety of interfaces such as S/PDIF, SPI, I^{2}S, I^{2}C, UART, USB, GPIOs, GMAC, PWM
- Supports up to 6 channels of ADC
- Supports MPEG-TS HW Parser
- Supports 1x USB Host, 1x USB OTG and 1x HSIC Host
- Supports secure JTAG
- Supports ARM TrustZone Technology
- Supports a variety of Power Modes (Normal, Sleep, Stop Modes)
- Supports a variety of Booting Options
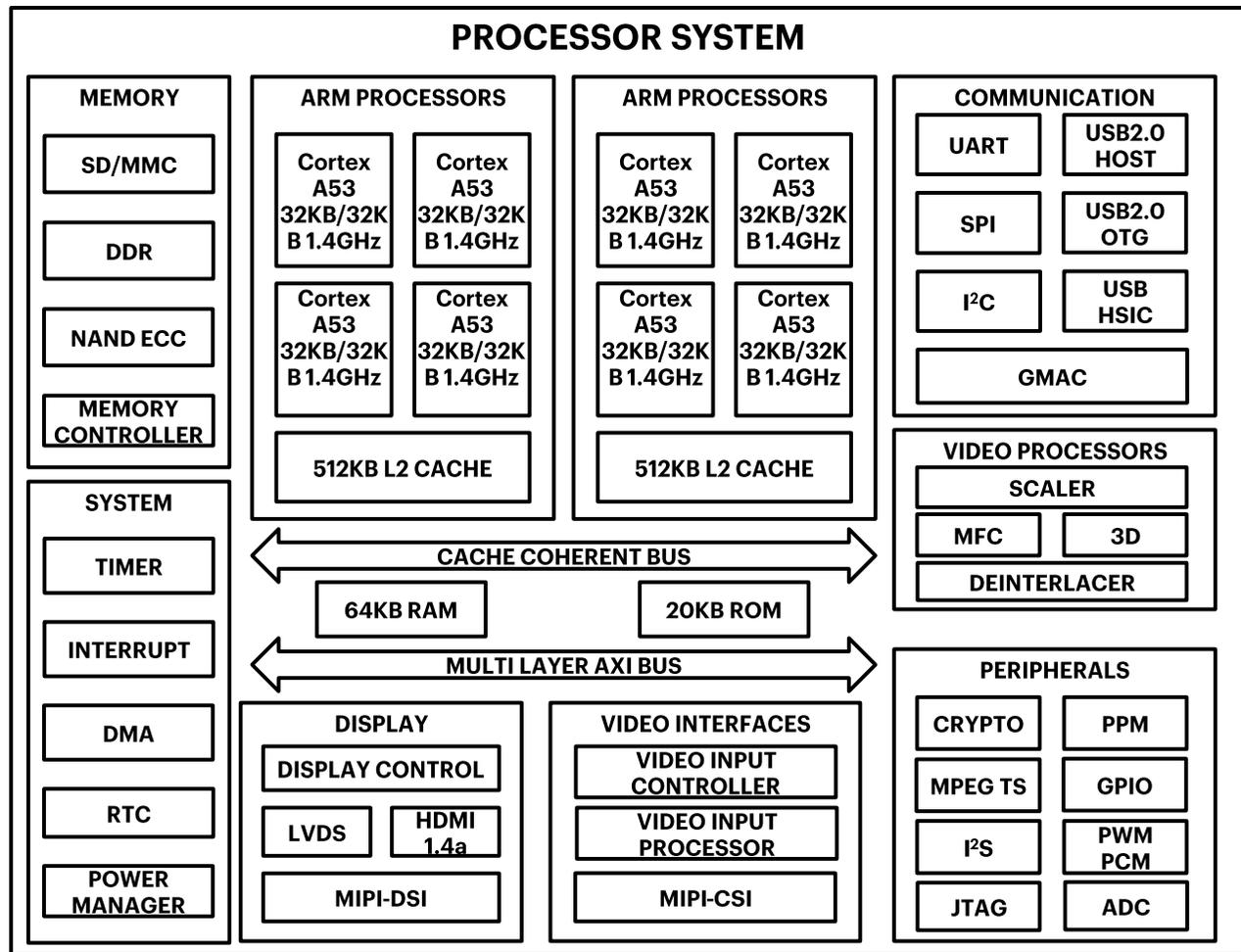
Figure 4. Processor System Block Schematic

SD/MMC

The ARTIK 710 Module provides 1x SD/MMC interface. The Mobile Storage Host is an interface between the system and SD/MMC card. The key features of mobile storage host sub-system are:

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support for Embedded Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support 8-bit DDR mode up to 50MHz
- Supports PIO and DMA mode data transfer
- Supports ¼- bit data bus width

MEMORY CONTROLLER

The most important features of the Memory module are:

- System Memory Controller
  - Support for 1GB DDR3 SDRAM
  - Maximum operating frequency of 800MHz
  - 32-bit data bus
- Static Memory Controller

- Multiplexed address up to 24-bit
- Support for SRAM, ROM and NAND flash
- Support for burst read/write
- NAND Flash Controller
  - Support for SLC/MLC Nand flash
  - ECC algorithm support

TIMER/WATCHDOG TIMER

The most important features of the Timer/Watchdog module are:

- 4x dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

INTERRUPT CONTROLLER

The most important features of the Interrupt Controller module are:

- Vectored Interrupt Controller
- Support for 4x interrupt types
  - 16x software generated interrupts
  - 6x External Private Peripheral Interrupt (PPI) per processor
  - 1x Internal PPI for each processor
  - 128x Shared peripheral interrupts
- For each interrupt source the following properties are available:
  - Fixed hardware interrupt priority level
  - Programmable interrupt priority level
  - Hardware interrupt priority level masking
  - IRQ and FIQ generation
  - Software interrupt generation
  - Test registers
  - Raw interrupt status
  - Interrupt request status

DMA

The most important features of the Scatter-Gather DMA module are:

- 16x channels of dedicated DMA
- 16x DMA request lines
- Various operating modes
  - Single DMA mode
  - Burst DMA mode
  - Memory 2 memory transfer
  - Memory to peripheral transfer
  - Peripheral to memory transfer
- Support for 8/16/32 bit wide transactions
- Big-Endian and Little-Endian (default) support

REAL TIME CLOCK (RTC) & POWER MANAGER

The most important features of the RTC and Power Manager module are:

- 4x spread spectrum PLLs
- 2x external crystals : 1x 24MHz crystal for PLL, 1x 32.768KHz crystal for RTC
- 32-bit RTC counter
- Support for alarm interrupt using RTC
- Support for various power modes
  - Normal, Idle, Stop, Sleep (Suspend to RAM)

ARM PROCESSORS

The most important features of the CPU module are:

- 8x Cortex A53 cores running at 1.4GHz
- Each core has 32KB of I-Cache (I$) and 32KB of D-Cache (D$)
- 2x 512KB of L2 Cache is shared between 2x4 cores
- Dedicated Vector Floating Point Processor (VFPP), Neon processor

LVDS

The ARTIK 710 Module provides 5x LVDS output channels with 1x clock channel. The key features of the LVDS channel system are:

- Output clock range 30-160MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

MIPI DSI

The ARTIK 710 Module provides 1x 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are:

- Maximum resolution ranges up to WUXGA 1920x1200
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
  - 16bpp, 18bpp packed, 18bpp loosely-packed (3 byte), 24bpp
- Supported interfaces are:
  - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
  - RGB Interface for video image input from display controller
  - An I80 interface for Command Mode Image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Pre-scaler to generate escape clock from byte clock

HDMI CONTROLLER

The ARTIK 710 Module provides 1x HDMI v1.4a interface. The key features of the HDMI sub-system are:

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
  - 480p@59.94/60Hz
  - 576p@50Hz
  - 720p@50/59.94/60Hz
  - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color
- HDMI-CEC compliant
- Integrated HDCP 1.4 compliant

MIPI CSI

The ARTIK 710 Module provides 1x 4-lane MIPI interface that complies with the MIPI CSI standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are:

- Supports 1, 2, 3 or 4 data lanes
- Supported image formats are:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - RGB565, RGB666, RGB888

- RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Compressed format : 10-6-10, 10-7-10, 10-8-10
- User defined Byte based data packet
- Compatible to PPI (Protocol to PHY interface)

VIDEO INPUT PROCESSOR

The ARTIK 710 Module provides 1x Video Input Processor (VIP). The key features of the VIP sub-system are:

- Support for external 8-bit and 16-bit MIPI
- Support for internal MIPI CSI
- Support of images up to 8192x8192
- Support for clipping and scale-down
- Support for YUV420, YUV422 and YUV444 memory format and linear YUV422 memory format

UART

The ARTIK 710 Module provides 3x2-pin UART with just RxD and TxD signals. The key features of the UART sub-system are:

- Separate 32x8 Tx and 32x12 Rx FIFO memory buffers
- Support for DMA and interrupt based mode of operation
- All independent channels support IrDA 1.0
- Support for modem control functions CTS, DCD, DSR, RTS, DTR and RI
- Each UART channel contains:
    - Programmable baud-rates
    - 1 or 2 stop bit insertion
    - 5-bit, 6-bit, 7-bit, or 8-bit data width
    - Parity checking

SPI

The ARTIK 710 Module provides 2x Serial Peripheral Interfaces (SPI) that transfers serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial, National Semiconductor's Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Complies with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Max operating frequency :
    - Master Mode : Support Tx up to 50MHz, Rx up to 20MHz
    - Slave Mode : Support Tx up to 8MHz, Rx up to 8MHz

I^{2}C

The ARTIK 710 Module provides 3x generic I^{2}C blocks supporting both 100kb/s and 400kb/s speed modes. The key features of the I^{2}C sub-system are:

- Supporting multi-master and slave mode
- 7-bit addressing mode only
- Supports serial, 8-bit oriented and bi-directional data transfer
- Supports up to 100 kb/s in the standard mode
- Supports up to 400 kb/s in the fast mode
- Supports master transmit, master receive, slave transmit, and slave receive operation
- Supports both interrupt and polling events

USB OTG

The ARTIK 710 Module provides 1x USB2.0 OTG interface supporting both device and host functionality. The key features of the USB2.0 OTG sub-system are:

- In compliance with the USB 2.0 On-The-Go specification revision 1.3a
- Operates in High Speed (480Mbps) Mode
- Operates in Full Speed (12Mbps) Mode
- Operates in Low Speed (1.5Mbps, host only) Mode
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- 1 control endpoint 0 for control transfer
- Supports up to 15 device-programmable endpoints:
    - Programmable endpoint type: Bulk, Isochronous, Interrupt
    - Programmable In/Out direction
- Supports 16 host channels

USB HOST/HSIC

The ARTIK 710 Module provides 1x USB2.0 Host controller that is fully compliant with the USB 2.0 specifications, and the Enhanced Host Controller Interface (EHCI) specification. The controller also provides a High Speed Inter Chip (HSIC) version 1.0 module. The key features of the USB2.0 OTG sub-system are:

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices
- In compliance with the UTMI+ Level3 revision 1.0
- Controlling the association to either the Open Host Controller Interface or the EHCI via a port router
- Root Hub functionality to support up/down stream port
- Support for HSIC version 1.0

ETHERNET MAC CONTROLLER

The most important features of the Ethernet MAC module are:

- Standard compliance
    - IEEE 802.3az-2010 (Energy Efficient Ethernet EEE)
    - RGMII v2.6
- MAC supports the following features:
    - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external gigabit PHY
    - Full duplex operation
    - Half duplex operation
    - Flexible address filtering
    - Additional frame filtering

SCALER

The ARTIK 710 Module provides a universal scaler. The key features of the scaler are:

- Support for different input formats
    - YUV420, YUV422, YUV444, interleaved UV
- Flexible size, from 8x8 up to 4096x4096 with a granularity of 8
- Upscale ratio from 8x8 to 4096x4096
- Downscale ratio from 4096x4096 to 8x8
- Low-pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

DE-INTERLACER

The ARTIK 710 Module provides a de-interlacer. The key features of the de-interlacer are:

- Support a maximum image width of 1920, image height is not limited

- Y, Cb and Cr are executed separately
- Separated YUV420, YUV422 and YUV444 format support

MULTI FORMAT CODEC

The ARTIK 710 Module provides an integrated Multi Format Codec (MFC) module. The key features of the MFC sub-system are:

- Decoder
  - H.264 : BP, MP, HP Level 4.2 up to 1920x1080, up to 50MBps
  - MPEG4 : Advanced Simple Profile (ASP) up to 1920x1080, up to 40Mbps
  - H.263 : Profile 3 up to 1920x1080, up to 20Mbps
  - VC-1 : SP, MP, AP profile, Level 3 up to 1920x1080, Level 3 up to 2048x1024, up to 45Mbps
  - MPEG 1,2 : Main Profile, High Level up to 1920x1080, up to 80MBps
  - VP8 : up to 1920x1080, up to 20Mbps
  - Theora : up to 1920x1080, up to 20Mbps
  - AVS : Jizhun profile, Level 6.2 up to 1920x1080, up to 40Mbps
  - RV8/9/10 : up to 1920x1080, up to 40Mbps
  - MJPEG : Baseline profile up to 8192x8292
- Encoder
  - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
  - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
  - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps
  - MJPEG : Baseline profile up to 8192x8192

GRAPHICS CONTROLLER

The ARTIK 710 Module provides 1x 2D and 1x 3D graphics accelerator. The key features of the graphics subsystem are:

- 2x pixel processors
  - Tile oriented processing
  - Alpha blending
  - Texture support, non-power-of-2
  - Cube mapping
  - Fast dynamic branching
  - Trigonometric acceleration
  - Full floating point arithmetic
  - Line, quad, triangle and point sprites
  - Perspective correct texturing
  - Point sampling, bilinear and trilinear filtering
  - 8-bit stencil buffering
  - 4-level hierarchical Z and stencil operation
- 1x geometry processor
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads
- Support for OpenGL ES 1.0 and 2.0
- Support for OpenVG 1.1

SECURITY IP

In addition to the Secure Element that is part of the ARTIK 710 Module, the main processor on the module provides additional security features:

- Secure 128-bit die ID
- On chip secure JTAG
  - Secure 128-bit JTAG ID
- On chip secure boot

- Secure 128-bit boot ID
- ARM TrustZone
  - TZPC (TrustZone Platform Controller)
  - TZASC (TrustZone Address Space Controller)
  - TZMA (TrustZone Memory Adapter)
- Hardware crypto accelerators
  - DES, Tripple DES
  - AES
  - SHA-1
  - MD5
  - PRNG

PPM PULSE PERIOD MEASUREMENT

The ARTIK 710 Module has a Pulse Period Measurement (PPM) IP-block that can measure the duration of a high level or low level from a GPIO pin. The PPM has a 16-bit counter that is tied to a clock that can vary between 843.750kHz-13.5MHz. For more details on how to relate a PPM to a GPIO please refer to the ARTIK 710 software developer's guide.

MPEG TS

The ARTIK 710 Module provides 1x MPEG Transport Stream de-multiplexer. The most important features of the MPEG-TS are:

- Support for 8-bit parallel mode
- Support for internal and external DMA
- Support for encoding and decoding of AES and CAS based streams
- Support for 2x channel MPEG-TS input with simultaneous 1x channel MPEG-TS output

I²S

The ARTIK 710 Module provides 2x 5-line Inter-IC Sound (I^{2}S) channel. I^{2}S is one of the most popular digital audio interfaces. The I^{2}S bus handles audio data and other signals, such as sub-coding and control. It is possible to transmit data between two I^{2}S buses. The key features of the I^{2}S sub-system are:

- Supports 1-port stereo (1 channel) I^{2}S-bus for audio with DMA based operation
- Supports serial data transfer of 16/24-bit per channel in Master and Slave mode
- Supports a variety of interface modes
  - I^{2}S, Left justified, Right justified, DSP mode

PCM

The ARTIK 710 Module provides 1x PCM channel. The PCM interface provides a bi-directional serial interface that can be connected to an external audio codec. The key features of the PCM sub-system are:

- Supports both Master and Slave mode external audio codecs
- Supports both short and long frame synchronization
- Supports a variety of data formats with a default format of 13-bit 2s complement, left justified, clock MSB first

PWM

The ARTIK 710 Module provides 2x PWM instances. The key features of the PWM sub-system are:

- 2x individual PWM channels with independent duty control and polarity
- 2x 32-bit PWM timers, 1x per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one-shot pulse mode
- Dead zone generator
- Level interrupt generation

GPIO

The ARTIK 710 Module provides a GPIO system with up to 108 GPIOs (77 multiplexed, 31 dedicated) to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- All GPIOs have programmable pull-up control
- All GPIOs have edge detect and level detect
- All GPIOs support programmable pull-up resistance
- All GPIOs can be set for Fast Slew or Normal Slew operation
- All GPIOs can be set for Default Drive Strength or High Drive Strength set by
- All GPIOs support individual interrupt generation and can be triggered on:
    - Rising edge
    - Falling edge
    - High level detection
    - Low level detection
    - GPIO data is clocked in at 50MHz

ADC

The ADC interface controls one 28nm low power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are:

- Up to 6-channels of analog input can be selected
- Converts analog input into 12-bit binary code up to 1MSPS
- Power consumption 1.0mW when running 1MSPS
- Input frequency up to 100kHz

ARTIK 710 MODULE PADS

The ARTIK 710 Module utilizes 271 signal and ground BALLs providing all the relevant signaling. _Figure 5_ shows how the BALLs are oriented and how signal coordinates are assigned to the PADs of the ARTIK 710 Module. _Table 1_, _Table 2_, _Table 3_ and _Table 4_ describe the relation between the BALL coordinates and the BALL signal names. _Table 1_, _Table 2_, _Table 3_ and _Table 4_ also provide detailed characteristics for each BALL signal name.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43
PA1	PA2	PA3	PA4	PA5	PA6	PA7	PA8	PA9	PA10	PA11	PA12	PA13	PA14	No Ball	PA16	PA17	PA18	PA19	PA20	PA21	PA22	PA23	PA24	PA25	PA26	PA27	PA28	PA29	PA30	PA31	PA32	PA33	PA34	PA35	PA36	PA37	PA38	PA39	PA40	PA41	PA42	PA43
PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8	PB9	PB10	PB11	PB12	PB13	PB14	PB15	PB16	PB17	PB18	PB19	PB20	PB21	PB22	PB23	PB24	PB25	PB26	PB27	PB28	PB29	PB30	PB31	PB32	PB33	PB34	PB35	PB36	PB37	PB38	PB39	PB40	PB41	PB42	PB43
PC1	No Ball																																								PC42	PC43
PD1	No Ball																																								PD42	PD43
PE1	PE2																																								PE42	PE43
PF1	PF2																																								PF42	PF43
PG1	No Ball																																								PG42	PG43
PH1	No Ball																																								PH42	PH43
PJ1	PJ2									TP282	TP283	TP284																		TP285	TP286	TP287									PJ42	PJ43
PK1	PK2									TP301																					TP288										PK42	PK43
PL1	PL2									TP300																					TP289										PL42	PL43
PM1	PM2																																								PM42	PM43
PN1	PN2																																								PN42	PN43
PP1	No Ball																																								PP42	PP43
PR1	PR2																																								PR42	PR43
PT1	PT2																																								PT42	PT43
PU1	No Ball																																								PU42	PU43
PV1	No Ball																																								PV42	PV43
PW1	PW2																																								PW42	PW43
PY1	PY2																																								PY42	PY43
PAA1	PAA2									TP299																					TP290										PAA42	PAA43
PAB1	PAB2									TP298																					TP291										PAB42	PAB43
PAC1	PAC2									TP297	TP296	TP295																		TP294	TP293	TP292									PAC42	PAC43
PAD1	PAD2																																								PAD42	PAD43
PAE1	PAE2																																								PAE42	PAE43
PAF1	PAF2																																								PAF42	PAF43
PAG1	PAG2																																								PAG42	PAG43
PAH1	PAH2																																								PAH42	PAH43
PAJ1	PAJ2																																								PAJ42	PAJ43
PAK1	PAK2	PAK3	PAK4	PAK5	PAK6	PAK7	PAK8	PAK9	PAK10	PAK11	PAK12	PAK13	PAK14	PAK15	PAK16	PAK17	PAK18	PAK19	PAK20	PAK21	PAK22	PAK23	PAK24	PAK25	PAK26	PAK27	PAK28	PAK29	PAK30	PAK31	PAK32	PAK33	PAK34	PAK35	PAK36	PAK37	PAK38	PAK39	PAK40	PAK41	PAK42	PAK43
PAL1	PAL2	PAL3	PAL4	PAL5	PAL6	PAL7	PAL8	PAL9	PAL10	PAL11	PAL12	PAL13	PAL14	PAL15	PAL16	PAL17	PAL18	PAL19	PAL20	PAL21	PAL22	PAL23	PAL24	PAL25	PAL26	PAL27	PAL28	PAL29	PAL30	PAL31	PAL32	PAL33	PAL34	PAL35	PAL36	PAL37	PAL38	PAL39	PAL40	PAL41	PAL42	PAL43

Figure 5. ARTIK 710 Module Top View BALL Organization

TOP BALL ARRAY

Table 1. TOP BALL ARRAY

BAL LOC	BALL Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PA1	GMAC_TXEN	3V3	GMAC_TXEN	S	GPIO	N	GMAC	GMAC Transmit Enable
PA2	GMAC_TXD1	3V3	GMAC_TXD1	S	GPIO	N	GMAC	GMAC Transmit Data 1
PA3	GMAC_TXD3	3V3	GMAC_TXD3	S	GPIO	N	GMAC	GMAC Transmit Data 3
PA4	GND	0V0	GND	NA	0V0	-	GND	Ground
PA5	GMAC_GTXCLK	3V3	GMAC_GTXCLK	S	GPIO	N	GMAC	GMAC Transmit Clock
PA6	GMAC_RXDV	3V3	GMAC_RXDV	S	GPIO	N	GMAC	GMAC Receive Enable
PA7	GMAC_RXD2	3V3	GMAC_RXD2	S	GPIO	N	GMAC	GMAC Receive Data 2
PA8	GMAC_RXD0	3V3	GMAC_RXD0	S	GPIO	N	GMAC	GMAC Receive Data 0
PA9	GND	0V0	GND	NA	0V0	-	GND	Ground
PA10	AP_MIPICSI_DNCLK	1V8	MIPICSI_DNCLK	S	IO	N	CSI	MIPI CSI Data Negative Clock
PA11	AP_MIPICSI_DN0	1V8	MIPICSI_DN0	S	IO	N	CSI	MIPI CSI Data Negative 0
PA12	AP_MIPICSI_DN1	1V8	MIPICSI_DN1	S	IO	N	CSI	MIPI CSI Data Negative 1
PA13	AP_MIPICSI_DN2	1V8	MIPICSI_DN2	S	IO	N	CSI	MIPI CSI Data Negative 2
PA14	AP_MIPICSI_DN3	1V8	MIPICSI_DN3	S	IO	N	CSI	MIPI CSI Data Negative 3
PA15	NO BALL	-	-	-	-	-	NO BALL	NA
PA16	AP_MIPIDSI_DNCLK	1V8	MIPIDSI_DNCLK	S	IO	N	DSI	MIPI DSI Data Negative Clock
PA17	AP_MIPIDSI_DN0	1V8	MIPIDSI_DN0	S	IO	N	DSI	MIPI DSI Data Negative 0
PA18	AP_MIPIDSI_DN1	1V8	MIPIDSI_DN1	S	IO	N	DSI	MIPI DSI Data Negative 1
PA19	AP_MIPIDSI_DN2	1V8	MIPIDSI_DN2	S	IO	N	DSI	MIPI DSI Data Negative 2
PA20	AP_MIPIDSI_DN3	1V8	MIPIDSI_DN3	S	IO	N	DSI	MIPI DSI Data Negative 3
PA21	GND	0V0	GND	NA	0V0	-	GND	Ground
PA22	AP_LVDS_TN0	1V8	LVDS_TN0	S	IO	N	LVDS	LVDS Transmit Channel 0 Negative
PA23	AP_LVDS_TN1	1V8	LVDS_TN1	S	IO	N	LVDS	LVDS Transmit Channel 1 Negative
PA24	AP_LVDS_TN2	1V8	LVDS_TN2	S	IO	N	LVDS	LVDS Transmit Channel 2 Negative
PA25	AP_LVDS_TNCLK	1V8	LVDS_TNCLK	S	IO	N	LVDS	LVDS Transmit Negative Clock
PA26	AP_LVDS_TN3	1V8	LVDS_TN3	S	IO	N	LVDS	LVDS Transmit Channel 3 Negative
PA27	AP_LVDS_TN4	1V8	LVDS_TN4	S	IO	N	LVDS	LVDS Transmit Channel 4 Negative
PA28	GND	0V0	GND	NA	0V0	-	GND	Ground
PA29	AP_HDMI_CEC	3V3	SA3	S	GPIO	N	HDMI	HDMI Consumer Electronics Control
PA30	AP_HDMI_TX2N	1V8	HDMI_TXN2	S	O	N	HDMI	HDMI Transmit Channel 1 Negative
PA31	AP_HDMI_TX1N	1V8	HDMI_TXN1	S	O	N	HDMI	HDMI Transmit Channel 0 Negative
PA32	AP_HDMI_TX0N	1V8	HDMI_TXN0	S	O	N	HDMI	HDMI Transmit Channel 2 Negative
PA33	AP_HDMI_TXCN	1V8	HDMI_TXNCLK	S	O	N	HDMI	HDMI Transmit Negative Clock
PA34	GND	0V0	GND	NA	0V0	-	GND	Ground
PA35	AP_OTG_DM	3V3	USB2.0OTG_DM	S	IO	N	USB OTG	USB OTG Data Minus
PA36	AP_USBH_DM	3V3	USB2.0HOST_DM	S	IO	N	USB HOST	USB HOST Data Plus
PA37	AP_GPA13	3V3	DISD12	S	GPIO	N	GPIO	Generic GPIO
PA38	AP_HSIC_STROBE	1V2	USBHSIC_STROBE	S	IO	N	HSIC	HSIC Strobe
PA39	AP_GPA14	3V3	DISD13	S	GPIO	N	GPIO	Generic GPIO
PA40	AP_GPA9	3V3	DISD8	S	GPIO	N	GPIO	Generic GPIO
PA41	AP_GPA15	3V3	DISD14	S	GPIO	N	GPIO	Generic GPIO
PA42	AP_GPA12	3V3	DISD11	S	GPIO	N	GPIO	Generic GPIO
PA43	GND	0V0	GND	NA	0V0	-	GND	Ground
PB1	GND	0V0	GND	NA	0V0	-	GND	Ground
PB2	GMAC_TXD0	3V3	GMAC_TXD0	S	GPIO	N	GMAC	GMAC Transmit Data 0
PB3	GMAC_TXD2	3V3	GMAC_TXD2	S	GPIO	N	GMAC	GMAC Transmit Data 2

BAL LOC	BALL Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PB4	GMAC_MDC	3V3	GMAC_MDC	S	GPIO	N	GMAC	GMAC MDC
PB5	GMAC_RXCLK	3V3	GMAC_RXCLK	S	GPIO	N	GMAC	GMAX Receive Clock
PB6	GMAC_RXD3	3V3	GMAC_RXD3	S	GPIO	N	GMAC	GMAC Receive Data 3
PB7	GMAC_RXD1	3V3	GMAC_RXD1	S	GPIO	N	GMAC	GMAC Receive Data 1
PB8	GMAC_MDIO	3V3	GMAC_MDIO	S	GPIO	N	GMAC	GMAC MDIO
PB9	GND	0V0	GND	NA	0V0	-	GND	Ground
PB10	AP_MIPICSI_DPCLK	1V8	MIPICSI_DPCLK	S	IO	N	CSI	MIPI CSI Data Positive Clock
PB11	AP_MIPICSI_DP0	1V8	MIPICSI_DP0	S	IO	N	CSI	MIPI CSI Data Positive 0
PB12	AP_MIPICSI_DP1	1V8	MIPICSI_DP1	S	IO	N	CSI	MIPI CSI Data Positive 1
PB13	AP_MIPICSI_DP2	1V8	MIPICSI_DP2	S	IO	N	CSI	MIPI CSI Data Positive 2
PB14	AP_MIPICSI_DP3	1V8	MIPICSI_DP3	S	IO	N	CSI	MIPI CSI Data Positive 3
PB15	GND	0V0	GND	NA	0V0	-	GND	Ground
PB16	AP_MIPIDSI_DPCLK	1V8	MIPIDSI_DPCLK	S	IO	N	DSI	MIPI DSI Data Positive Clock
PB17	AP_MIPIDSI_DP0	1V8	MIPIDSI_DP0	S	IO	N	DSI	MIPI DSI Data Positive 0
PB18	AP_MIPIDSI_DP1	1V8	MIPIDSI_DP1	S	IO	N	DSI	MIPI DSI Data Positive 1
PB19	AP_MIPIDSI_DP2	1V8	MIPIDSI_DP2	S	IO	N	DSI	MIPI DSI Data Positive 2
PB20	AP_MIPIDSI_DP3	1V8	MIPIDSI_DP3	S	IO	N	DSI	MIPI DSI Data Positive 3
PB21	GND	0V0	GND	NA	0V0	-	GND	Ground
PB22	AP_LVDS_TP0	1V8	LVDS_TP0	S	IO	N	LVDS	LVDS Transmit Channel 0 Positive
PB23	AP_LVDS_TP1	1V8	LVDS_TP1	S	IO	N	LVDS	LVDS Transmit Channel 1 Positive
PB24	AP_LVDS_TP2	1V8	LVDS_TP2	S	IO	N	LVDS	LVDS Transmit Channel 2 Positive
PB25	AP_LVDS_TPCLK	1V8	LVDS_TPCLK	S	IO	N	LVDS	LVDS Transmit Positive Clock
PB26	AP_LVDS_TP3	1V8	LVDS_TP3	S	IO	N	LVDS	LVDS Transmit Channel 3 Positive
PB27	AP_LVDS_TP4	1V8	LVDS_TP4	S	IO	N	LVDS	LVDS Transmit Channel 4 Positive
PB28	GND	0V0	GND	NA	0V0	-	GND	Ground
PB29	AP_HDMI_HPD	3V3	HDMI_HOT5V	S	I	N	HDMI	HDMI Hot 5V
PB30	AP_HDMI_TX2P	1V8	HDMI_TXP2	S	O	N	HDMI	HDMI Transmit Channel 1 Positive
PB31	AP_HDMI_TX1P	1V8	HDMI_TXP1	S	O	N	HDMI	HDMI Transmit Channel 0 Positive
PB32	AP_HDMI_TX0P	1V8	HDMI_TXP0	S	O	N	HDMI	HDMI Transmit Channel 2 Positive
PB33	AP_HDMI_TXCP	1V8	HDMI_TXPCLK	S	O	N	HDMI	HDMI Transmit Positive Clock
PB34	GND	0V0	GND	NA	0V0	-	GND	Ground
PB35	AP_OTG_DP	3V3	USB2.0OTG_DP	S	IO	N	USB OTG	USB OTG Data Plus
PB36	AP_USBH_DP	3V3	USB2.0HOST_DP	S	IO	N	USB HOST	USB HOST Data Minus
PB37	AP_OTG_ID	-	USB2.0OTG_ID	S	IO	N	USB HOST	USB HOST ID
PB38	AP_HSIC_DATA	1V2	USBHSIC_DATA	S	IO	N	HSIC	HSIC Data
PB39	AP_GPA4	3V3	DISD3	S	GPIO	N	GPIO	Generic GPIO
PB40	AP_GPA5	3V3	DISD4	S	GPIO	N	GPIO	Generic GPIO
PB41	AP_GPA16	3V3	DISD15	S	GPIO	N	GPIO	Generic GPIO
PB42	AP_GPA11	3V3	DISD10	S	GPIO	N	GPIO	Generic GPIO
PB43	GND	0V0	GND	NA	0V0	-	GND	Ground

BOTTOM BALL ARRAY

Table 2. BOTTOM BALL ARRAY

BALL LOC	BALL Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PAK1	AP_I2S0_DOUT	3V3	I2SDOUT0	S	GPIO	N	I2S0	I2S 0 Data Out
PAK2	AP_I2S0_BCLK	3V3	I2SBCLK0	S	GPIO	N	I2S0	I2S 0 Bit Clock
PAK3	AP_GPC11_SPI2_MISO	3V3	SA11	S	GPIO	N	SPI2	SPI 2 Receive Data
PAK4	AP_GPC9_SPI2_CLK	3V3	SA9	S	GPIO	N	SPI2	SPI 2 Clock
PAK5	AP_SPI0_MISO	3V3	SPIRXD0	S	GPIO	N	SPI0	SPI 0 Receive Data
PAK6	AP_SPI0_CLK	3V3	SPICLK0	S	GPIO	N	SPI0	SPI 0 Clock
PAK7	AP_GPC14_PWM2	3V3	SA14	S	GPIO	N	PWM	PWM 2
PAK8	AP_GPD6_SCL	3V3	SCL2	S	GPIO	N	I2C	I2C SCL
PAK9	AP_GPD4_SCL1	3V3	SCL1	S	GPIO	N	I2C	I2C SCL 1
PAK10	AP_GPD2_SCL0	3V3	SCL0	S	GPIO	N	I2C	I2C SCL 0
PAK11	AP_GPA23_HDMI_I2C_SCL	3V3	DISD22	S	GPIO	N	I2C	HDMI I2C SCL
PAK12	ZB_JTMS	3V3	-	-	-	-	ZIGBEE	ZIGBEE JTAG TMS
PAK13	ZB_JTCK	3V3	-	-	-	-	ZIGBEE	ZIGBEE JTAG TCK
PAK14	ZB_PC0	3V3	-	-	-	-	ZIGBEE	ZIGBEE Control
PAK15	ZB_PA4	3V3	-	-	-	-	ZIGBEE	ZIGBEE Control
PAK16	GND	0V0	GND	NA	0V0	-	GND	Ground
PAK17	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	DCDC3, VCC 3V3 Power
PAK18	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	DCDC3, VCC 3V3 Power
PAK19	AP_NBATTF	3V3	AP_NBATTF	-	NA	-	MISC	Battery
PAK20	AP_GPE2	3V3	VID0_6	S	GPIO	N	MISC	Miscellaneous
PAK21	AP_GPE1	3V3	VID0_5	S	GPIO	N	MISC	Miscellaneous
PAK22	AP_UARTTX3	3V3	UARTTXD3	S	GPIO	N	UART	UART Transmit Data 3
PAK23	AP_UARTTX4	3V3	SD13	S	GPIO	N	UART	UART Transmit Data 4
PAK24	AP_UARTTX5	3V3	SD15	S	GPIO	N	UART	UART Transmit Data 5
PAK25	AP_GPB0_VID1_1_I2SLRCK1	3V3	VID1_1	S	GPIO	N	I2S1	I2S 1 Left Right Clock
PAK26	AP_GPA28_I2SMCLK1	3V3	VICLK1	S	GPIO	N	I2S1	I2S 1 Master Clock
PAK27	AP_GPA30_VID1_0_I2SBCLK1	3V3	VID1_0	S	GPIO	N	I2S1	I2S 1 Bit Clock
PAK28	AP_SD0_CMD	3V3	SDCMD0	S	GPIO	N	SD/MMC	SD Command
PAK29	AP_SD0_D1	3V3	SDDAT0_1	S	GPIO	N	SD/MMC	SD Data 1
PAK30	AP_SD0_CLK	3V3	SDCLK0	S	GPIO	N	SD/MMC	SD Clock
PAK31	NO BALL	-	-	-	-	-	NO BALL	NA
PAK32	AP_GPB13_SD0_BOOT	3V3	SD0	S	GPIO	N	BOOTING	Select Booting Scenario
PAK33	AP_GPC17	3V3	SA17	S	GPIO	N	GPIO	Generic GPIO
PAK34	AP_GPC0	3V3	SA0	S	GPIO	N	GPIO	Generic GPIO
PAK35	AP_GPC26	3V3	RDNWR	S	GPIO	PU	GPIO	Generic GPIO
PAK36	AP_GPB8	3V3	VID1_5	S	GPIO	N	GPIO	Generic GPIO
PAK37	AP_GPB14	3V3	RNB0	S	GPIO	N	MISC	Miscellaneous
PAK38	AP_GPA20	3V3	DISD19	S	GPIO	N	GPIO	Generic GPIO
PAK39	AP_GPA18	3V3	DISD17	S	GPIO	N	GPIO	Generic GPIO
PAK40	AP_GPA21	3V3	DISD20	S	GPIO	N	GPIO	Generic GPIO
PAK41	AP_GPA10	3V3	DISD9	S	GPIO	N	GPIO	Generic GPIO
PAK42	AP_GPA6	3V3	DISD5	S	GPIO	N	GPIO	Generic GPIO
PAK43	BT_PCM_D_IN	3V3	-	-	-	-	BT PCM	PCM Data In
PAL1	AP_I2S0_DIN	3V3	I2SDIN0	S	GPIO	N	I2S0	I2S 0 Data In
PAL2	AP_I2S0_MCLK	3V3	I2SMCLK0	S	GPIO	N	I2S0	I2S 0 Master Clock
PAL3	AP_GPC12_SPI2_MOSI	3V3	SA12	S	GPIO	N	SPI2	SPI 2 Transmit Data
PAL4	AP_GPC10_SPI2_CS	3V3	SA10	S	GPIO	PU	SPI2	SPI 2 Frame
PAL5	AP_SPI0_MOSI	3V3	SPITXD0	S	GPIO	N	SPI0	SPI 0 Transmit Data
PAL6	AP_SPI0_CS	3V3	SPIFRM0	S	GPIO	N	SPI0	SPI 0 Frame

BALL LOC	BALL Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PAL7	AP_GPD1_PWM0	3V3	PWM0	S	GPIO	N	PWM	PWM 0
PAL8	AP_GPD7_SDA	3V3	SDA2	S	GPIO	N	I2C	I2C SDA
PAL9	AP_GPD5_SDA1	3V3	SDA1	S	GPIO	N	I2C	I2C SDA 1
PAL10	AP_GPD3_SDA0	3V3	SDA0	S	GPIO	N	I2C	I2C SDA 0
PAL11	AP_GPA24_HDMI_I2C_SDA	3V3	DISD23	S	GPIO	N	I2C	HDMI I2C SDA
PAL12	ZB_JTDI	3V3	-	-	-	-	ZIGBEE	ZIGBEE JTAG TDI
PAL13	ZB_JTDO	3V3	-	-	-	-	ZIGBEE	ZIGBEE JTAG TDO
PAL14	ZB_RSTN	3V3	SA8	S	GPIO	N	ZIGBEE	ZIGBEE Reset
PAL15	ZB_PA5	3V3	NSCS1	S	GPIO	PU	ZIGBEE	ZIGBEE Control
PAL16	GND	0V0	GND	NA	0V0	-	GND	Ground
PAL17	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	DCDC3, VCC 3V3 Power
PAL18	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	DCDC3, VCC 3V3 Power
PAL19	AP_VDDPWRON	3V3	VDDPWRON	S	O	N	MISC	VDD Power On
PAL20	AP_GPE3	3V3	VID0_7	S	GPIO	N	MISC	Miscellaneous
PAL21	AP_GPE0	3V3	VID0_4	S	GPIO	N	MISC	Miscellaneous
PAL22	AP_UARTRX3	3V3	UARTRXD3	S	GPIO	N	UART	UART Receive Data 3
PAL23	AP_UARTRX4	3V3	SD12	S	GPIO	N	UART	UART Receive Data 4
PAL24	AP_UARTRX5	3V3	SD14	S	GPIO	N	UART	UART Receive Data 5
PAL25	AP_GPD31	3V3	VID0_3	S	GPIO	N	MISC	Miscellaneous
PAL26	AP_GPB9_I2SDIN1	3V3	VID1_6	S	GPIO	N	I2S1	I2S 1 Data In
PAL27	AP_GPB6_VID1_4_I2SDOUT1	3V3	VID1_4	S	GPIO	N	I2S1	I2S 1 Data Out
PAL28	AP_SD0_D3	3V3	SDDAT0_3	S	GPIO	N	SD/MMC	SD Data 3
PAL29	AP_SD0_D2	3V3	SDDAT0_2	S	GPIO	N	SD/MMC	SD Data 2
PAL30	AP_SD0_D0	3V3	SDDAT0_0	S	GPIO	N	SD/MMC	SD Data 0
PAL31	AP_GPB4_VID1_3_BOOT	3V3	VID1_3	S	GPIO	N	BOOTING	Select Booting Scenario
PAL32	AP_GPB15_SD1_BOOT	3V3	SD1	S	GPIO	N	BOOTING	Select Booting Scenario
PAL33	AP_GPD8	3V3	SD8	S	GPIO	N	GPIO	Generic GPIO
PAL34	AP_GPE30	3V3	NSOE	S	GPIO	PU	GPIO	Generic GPIO
PAL35	AP_GPC27	3V3	NSDQM	S	GPIO	PU	GPIO	Generic GPIO
PAL36	AP_GPB22	3V3	SD6	S	GPIO	N	GPIO	Generic GPIO
PAL37	AP_GPB16	3V3	NNFOE0	S	GPIO	N	MISC	Miscellaneous
PAL38	AP_GPB23	3V3	SD7	S	GPIO	N	GPIO	Generic GPIO
PAL39	AP_GPA22	3V3	DISD21	S	GPIO	N	GPIO	Generic GPIO
PAL40	AP_GPA19	3V3	DISD18	S	GPIO	N	GPIO	Generic GPIO
PAL41	AP_GPA17	3V3	DISD16	S	GPIO	N	GPIO	Generic GPIO
PAL42	AP_GPA3	3V3	DISD2	S	GPIO	N	GPIO	Generic GPIO
PAL43	BT_PCM_CLK	3V3	-	-	-	-	BT PCM	PCM Clock