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Hexagon Application Kit

For XMC4000 Family

CPU_42A-V1

CPU Board XMC4200 Actuator

Board User's Manual

Revision 1.0, 2013-02-19

Microcontroller

Edition 2013-02-19

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2013-02-19	Initial release

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Introduction

This document describes the features and hardware details of the CPU Board XMC4200 Actuator (CPU_42A-V1) designed to work with Infineon's XMC4200 Microcontroller. This board is part of Infineon's Hexagon Application Kits.

1 Overview

The CPU board CPU_42A-V1 houses the XMC4200 Microcontroller and the ACT satellite connector for application expansion. The board along with satellite cards (e.g. AUT_ISO-V1, MOT_GPDLV-V2 boards) demonstrates the capabilities of XMC4200. The main use case for this board is to demonstrate motor control and power conversion features of the XMC4200 device including tool chain. The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

1.1 Key Features

The CPU_42A-V1 board is equipped with the following features

- XMC4200 (ARM® Cortex™-M4-based) Microcontroller, 256 kByte on-chip Flash, QFN-48
- Connection to satellite cards via the ACT satellite connector
- USB Device support via micro USB connector
- CAN Transceiver with CAN Connector (SUB-D, DE-9 male)
- Debug options
  - On-board Debugger via the Debug USB connector
  - Cortex Debug connector 10-pin (0.05")
  - Cortex Debug+ETM connector 20-pin (0.05")
- Reset push button
- Boot from Embedded Flash or CAN
- PowerScale Connector: Ready for power consumption analysis
- 6 LED's
  - 3 Power indicating LEDs
  - 1 User LED (P2.1)
  - 1 RESET LED
  - 1 Debug LED
- User button connected to P14.7
- Potentiometer, connected to analog input P14.4
- Power supply
  - Via Micro-USB connector
  - Via satellite connector pins (ACT satellite cards can supply power to CPU board)
  - Via Debug USB connector (Micro USB)
  - RTC backup battery

1.2 Block Diagram

Figure 1 shows the functional block diagram of the CPU_42A-V1 board. For more information about the power supply please refer to chapter 2.1.

The CPU board has got the following building blocks:

- Satellite Connector (ACT)
- CAN transceiver and CAN Connector
- Variable resistor (POTI) connected to GPIO P14.4
- USB Connector (Micro-USB)
- On-board Debugger via Debug USB connector (Micro-USB)
- 2 Cortex Debug Connectors
- User LED connected to GPIO P2.1
- User Button connected to P14.7

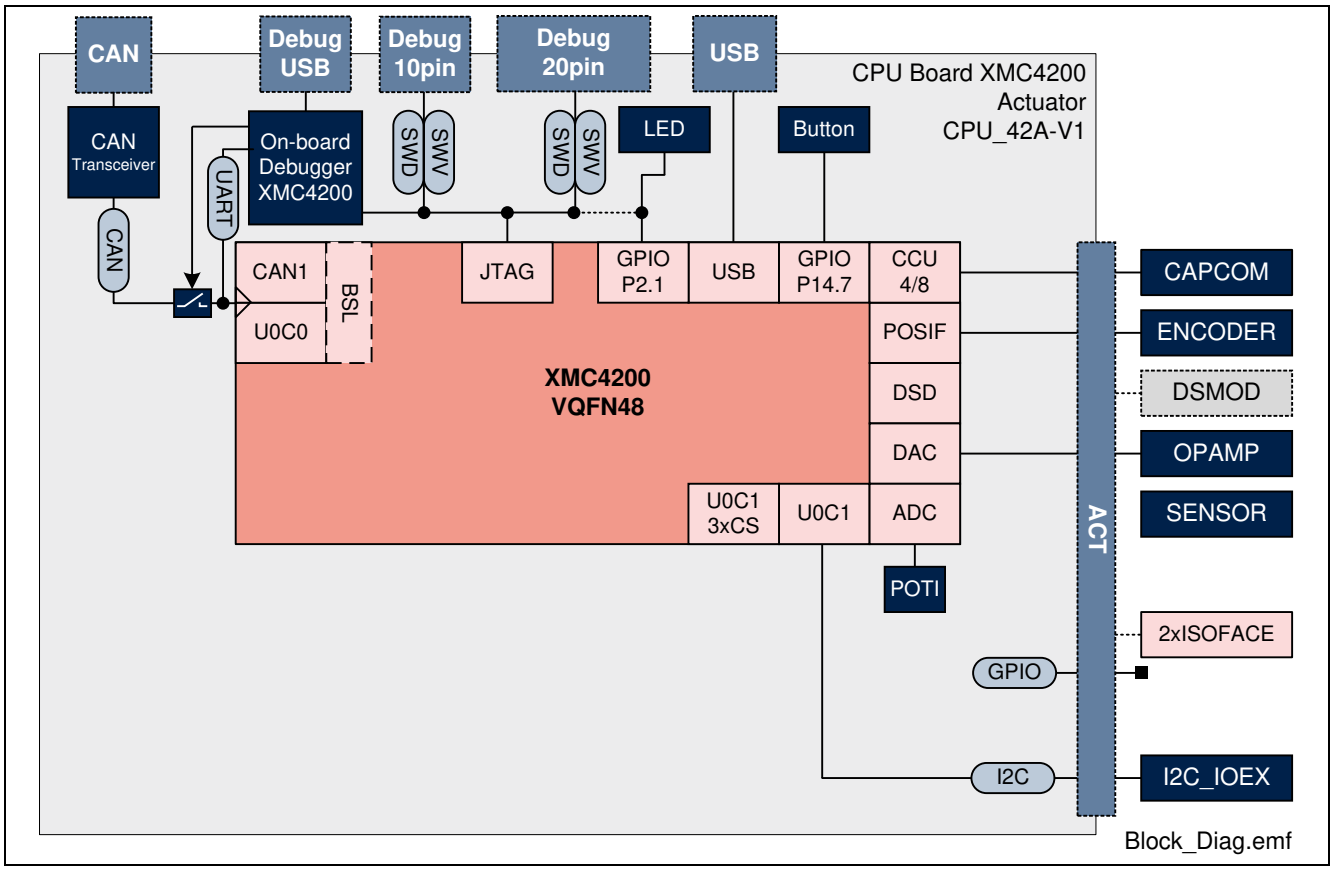

Figure 1 Block Diagram of the CPU Board CPU_42A-V1

2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

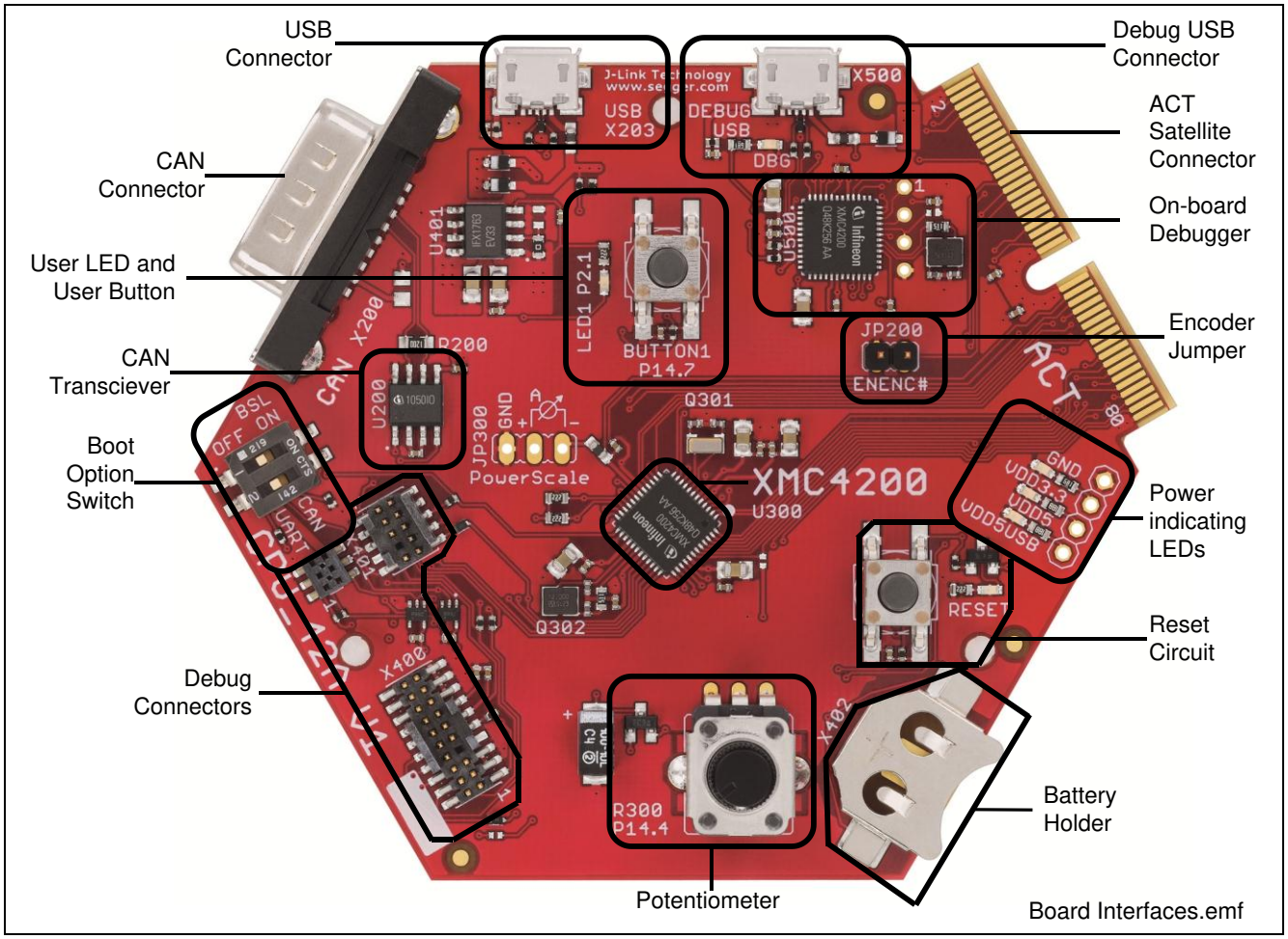

Figure 2 CPU Board XMC4200 Actuator(CPU_42A-V1)

2.1 Power Supply

The CPU_42A-V1 board can be powered via either of the USB plugs (5 V); however, there is a current limit that can be drawn from the host PC through USB. If the CPU_42A-V1 board is used to drive other satellite cards e.g. MOT_GPDLV-V2 and the total system current required exceeds 500 mA, then the CPU_42A-V1 board needs to be powered by the satellite cards. These satellite cards support external power supply.

The typical current drawn by the CPU board without any satellite cards connected is about 170 mA (@5 V).

For powering the board through an USB interface, connect the USB cable provided with the kit to either of the Micro-USB connector on board as shown in Figure 3.

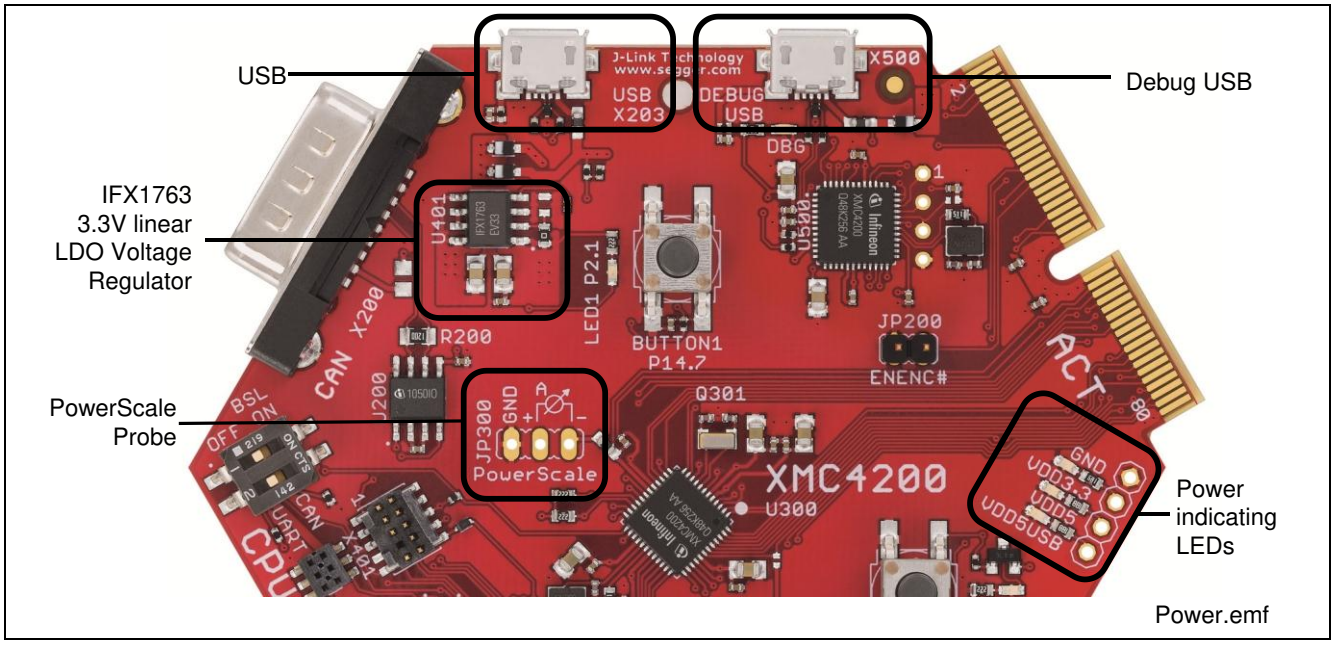

Figure 3 Powering Options

To indicate the power status of the CPU_42A-V1 board three power indication LED's are provided on board (see Figure 3). The LED will be "ON" when the corresponding power rail is powered.

Table 1 Power status LED's

LED Reference	Power Rail	Voltage	Note
V401	VDD5	5 V	Must always be "ON"
V402	VDD5USB	5 V	"ON" if powered by USB connector X203 "OFF" in all other supply cases
V403	VDD3.3	3.3 V	Must always be "ON"

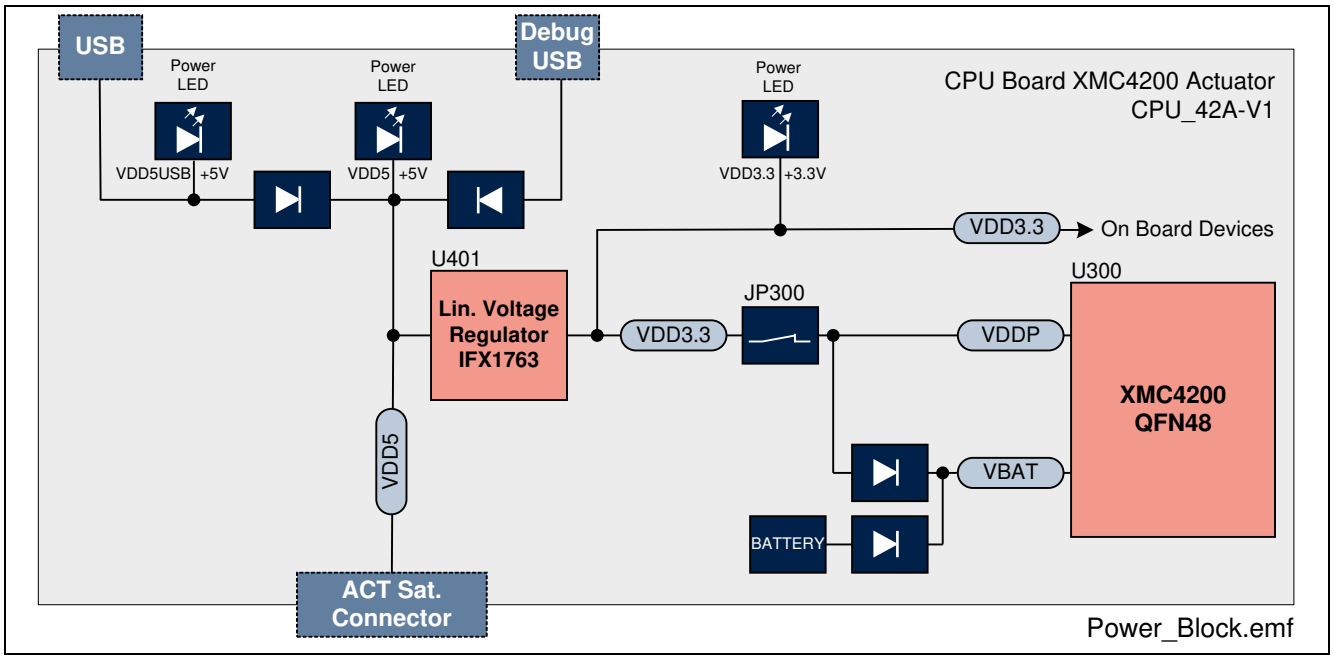

Figure 4 Block Diagram Of Power Supply

Hitex PowerScale probe is provided on the CPU_42A-V1 board to measure the power consumption of the XMC4200.

Table 2 Power Measurement

Jumper	Function	Description
JP300	PowerScale	A Hitex PowerScale probe can be connected for current sensing the VDD3.3 (CPU power source). Default: pos. 1-2 (closed) *Note: On the PCB there is a shorting trace between pin 1-2. This trace has to be cut first, before using PowerScale. Pin 3 is GND.*

2.2 Encoder Jumper

The jumper JP200 “ENENC#” on the CPU_42A-V1 board is used to enabled/disable an external unit connected to the ACT satellite connector, e.g.an encoder line receiver on the Motor Drive Card MOT_GPLV-V2.

The signal on the encoder jumper is not connected to the XMC4200. It’s connected to pin 30 of the ACT satellite connector only. If the jumper JP200 is shorted, a ground level is driven at pin 30 of the ACT satellite connector. If the jumper is open the line is floating. In this case a pull-up resistor on the ACT satellite card must ensure a high level.

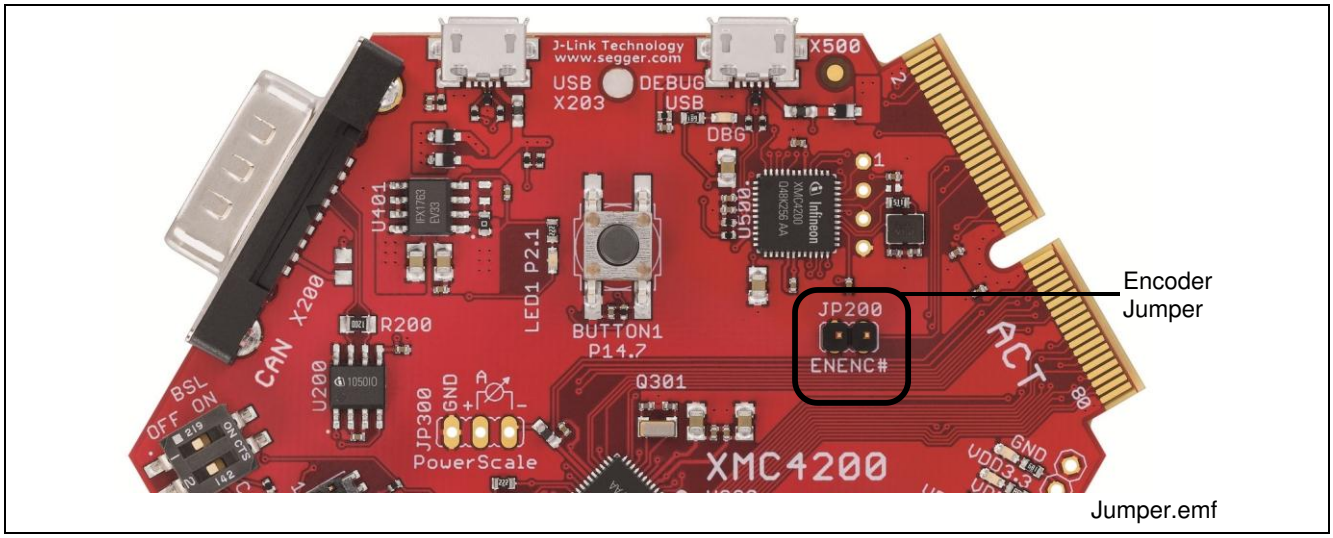

Figure 5 Encoder Jumper

2.3 CAN

The CPU_42A-V1 board provides a CAN interface via a Sub-D DE-9 connector (X200). Infineon's high speed CAN transceiver IFX1050GVIO for industrial application supports 3.3V I/O logic and is suitable for 12V and 24V bus systems with an excellent EMC performance. The CAN bus is terminated on-board with 120 Ohm.

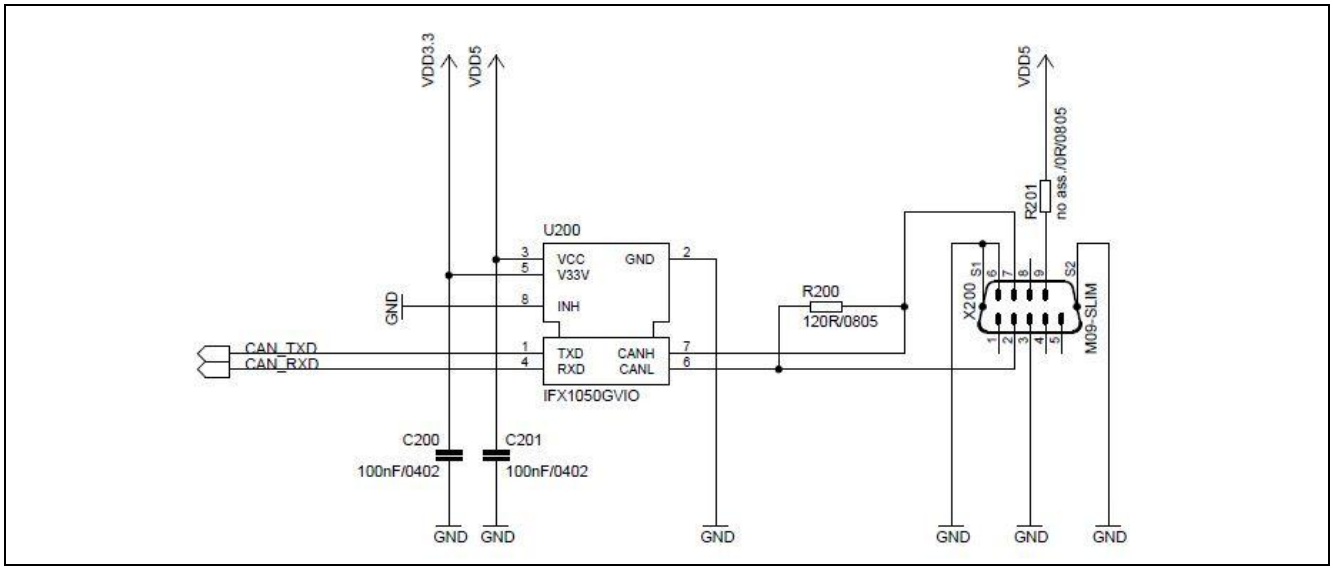

Figure 6 CAN Interface

Table 3 shows the signals available at the CAN connector X200.

Table 3 CAN Connector Pinout (X200)

Pin No.	Signal Name	Description
1	NC	No Connection
2	CANL	CAN Low
3	GND	Ground
4	NC	No Connection
5	NC	No Connection
6	GND	Ground
7	CANH	CAN High
8	NC	No Connection
9	VDD	5 Volt (not connected, use R201 to apply power to the connector)

The CAN signals CAN_TXD and CAN_RXD are routed to XMC4200 port pins P1.5 and P1.4 respectively via the switches U301 and U303.These switches will disconnect the CAN transceiver from the port pins P1.5 and P1.4 in case a UART function is required. On these pins of the XMC4200 the UART function is overlaid with the CAN function. The UART function can be used for external communication via a USB virtual COM port, which is supported by the on-board debugger.

2.4 Reset

A reset signal connected to the low-active PORST# pin of XMC4200 (U300) can be issued by

- an on-board Reset Button (SW400, RESET)
- an on-board debugger (U500)
- an external debugger connected to either of the Cortex Debug connector X400 or X401

The RESET signal is routed to all satellite connectors. The reset circuit includes a red LED (V407) to indicate the reset status: The Reset LED (V407) will be “ON” during active reset state and will be “OFF” if reset is not active.

Be aware that PORST# is a bidirectional reset pin of the XMC4000 family which can also be pulled low by the XMC4000 device itself.

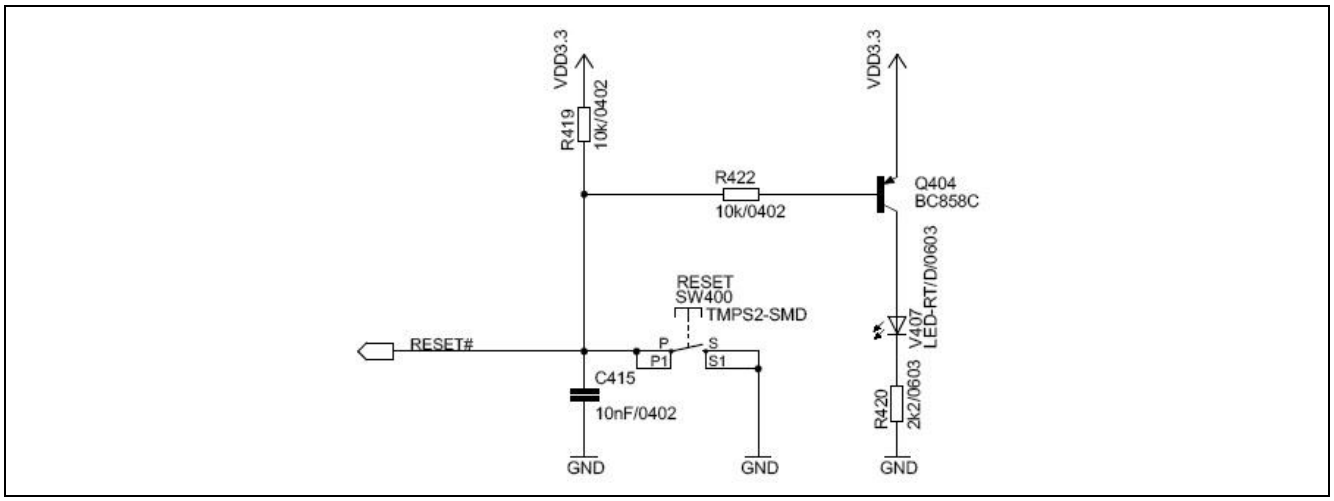

Figure 7 Reset

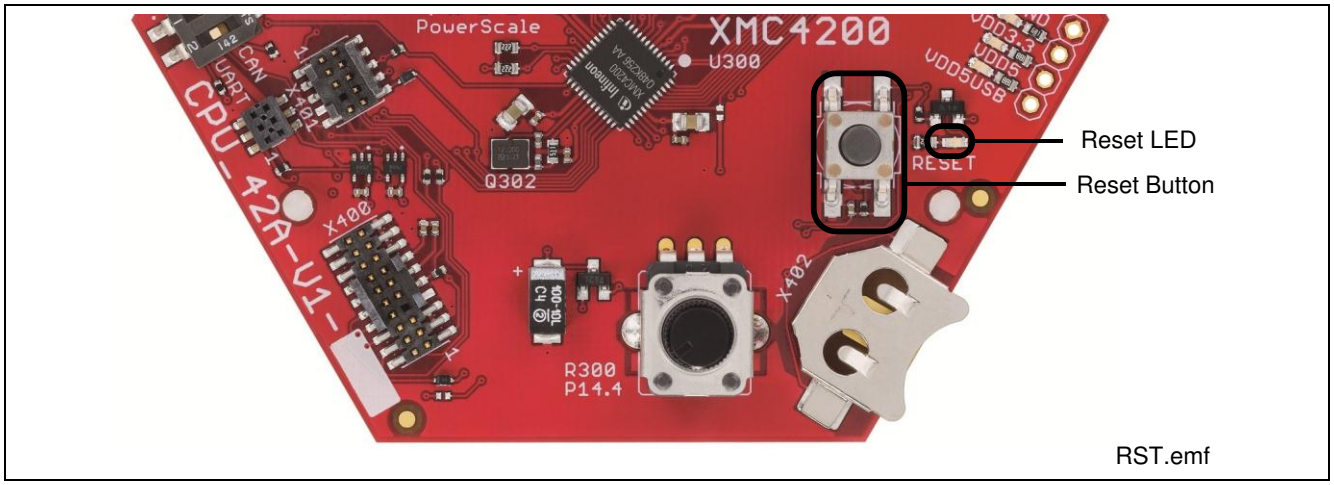

Figure 8 Reset LED and Reset Button

2.5 Clock Generation

An external 12 MHz crystal provides the clock signal to the XMC4200 microcontroller. The drive strength of the oscillator is set to maximum by software, in order to ensure a safe start-up of the oscillator even under worst case conditions. A serial 510 Ohm resistor will attenuate the oscillations during operations.

For the RTC clock a separate external 32.768 kHz crystal is used on board.

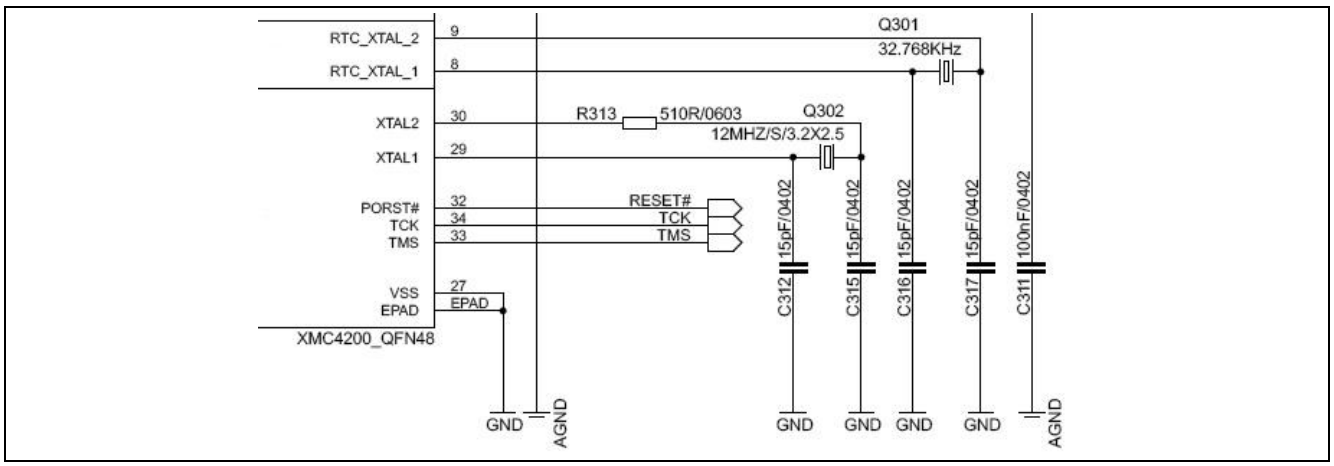

Figure 9 Clock Generation

2.6 Boot Option

During power-on-reset the XMC4200 latches the dip switch SW300 settings via the TCK and the TMS pin. Based on the values latched different boot options are possible.

Table 4 Boot Options Settings

BSL (TMS)	CAN/UART (TCK)	Boot Option
OFF (1)	UART (0)	Normal Mode (Boot from flash)
ON (0)	UART (0)	ASC BSL Enabled (Boot from UART)
OFF (1)	CAN (1)	BMI Customized Boot Enabled
ON (0)	CAN (1)	CAN BSL Enabled (Boot from CAN)

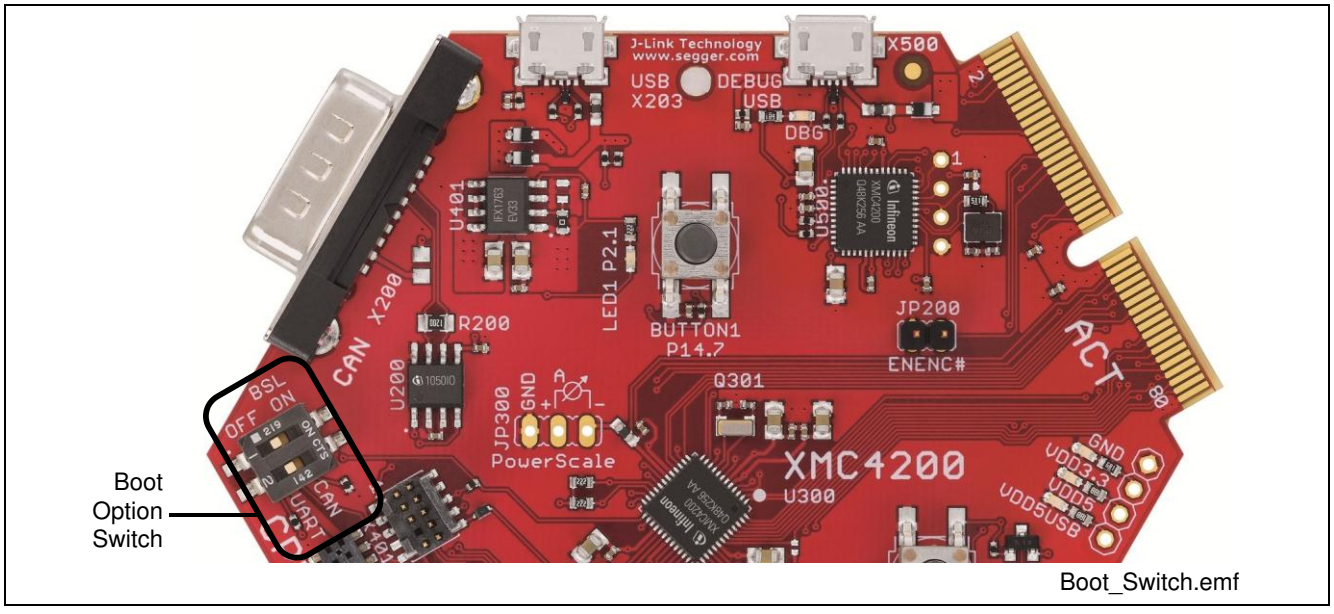

Figure 10 Boot Options Switch

2.7 Debug Interface

The CPU_42A-V1 board supports debugging via 3 different channels:

- On-board debugger
- Cortex Debug Connector (10-pin)
- Cortex Debug+ETM Connector (20-pin)

The Hexagon Application Boards are designed to use “Serial Wire Debug” as debug interface. JTAG debug is not supported by default because the GPIO P0.7, where the required TDI function is mapped to also, is used by various Actuator boards connected to the ACT satellite connector.

Note: It is strongly recommended not to use JTAG debug mode, especially if satellites boards are connected, which uses the GPIO P0.7. For the same reason also do not use the on-board debugger in JTAG debug mode.

If you want to use the JTAG debug mode through the cortex debug connectors (X400, X401) anyway, enable the JTAG interface of the XMC device by assembling the pull-up resistor R427 (4k7 Ohm) and the resistor R410 (0 - 33 Ohm).

2.7.1 On-board Debugger

The on-board debugger [1] supports

- Serial Wire Debug
- Serial Wire Viewer [2]
- Full Duplex UART communication via a USB Virtual COM

[1] Attention: Newer firmware versions of the on-board debugger require the latest J-Link driver (V4.62 or higher) and a Serial Port Driver (CDC driver) installed on your computer. Please check “Install J-Link Serial Port Driver” when installing the latest J-Link driver (see Figure 11)

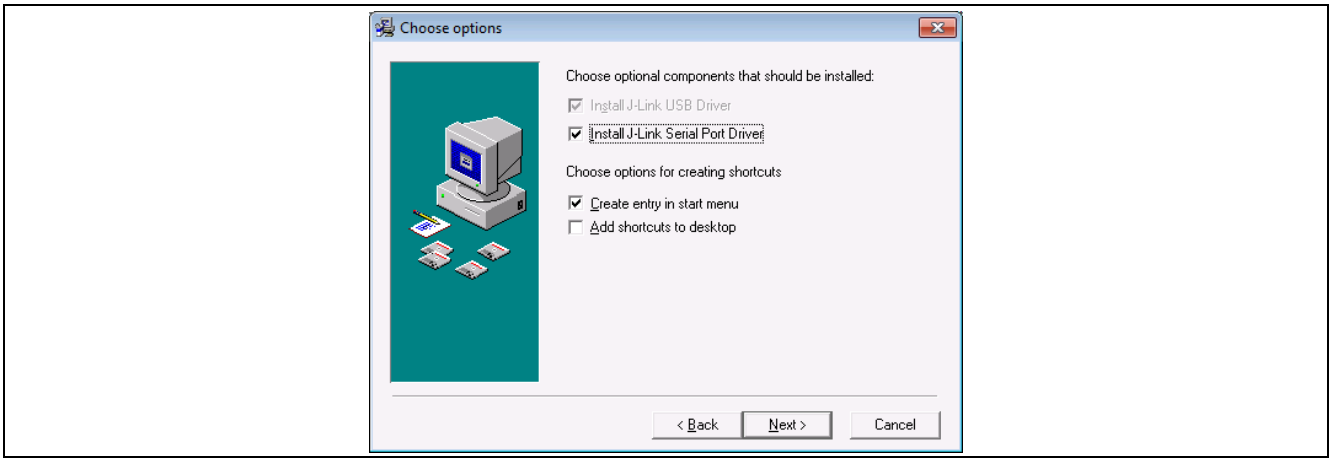

Figure 11 Installation of Serial Port Driver

[2] If Serial Wire Viewer is used, the User LED cannot freely be programmed and starts flickering, because the Serial Wire Viewer function is overlaid with the GPIO function connected to the User LED.

The on-board debugger can be accessed through the Debug USB connector shown in Figure 12. The Debug LED V502 shows the status during debugging.

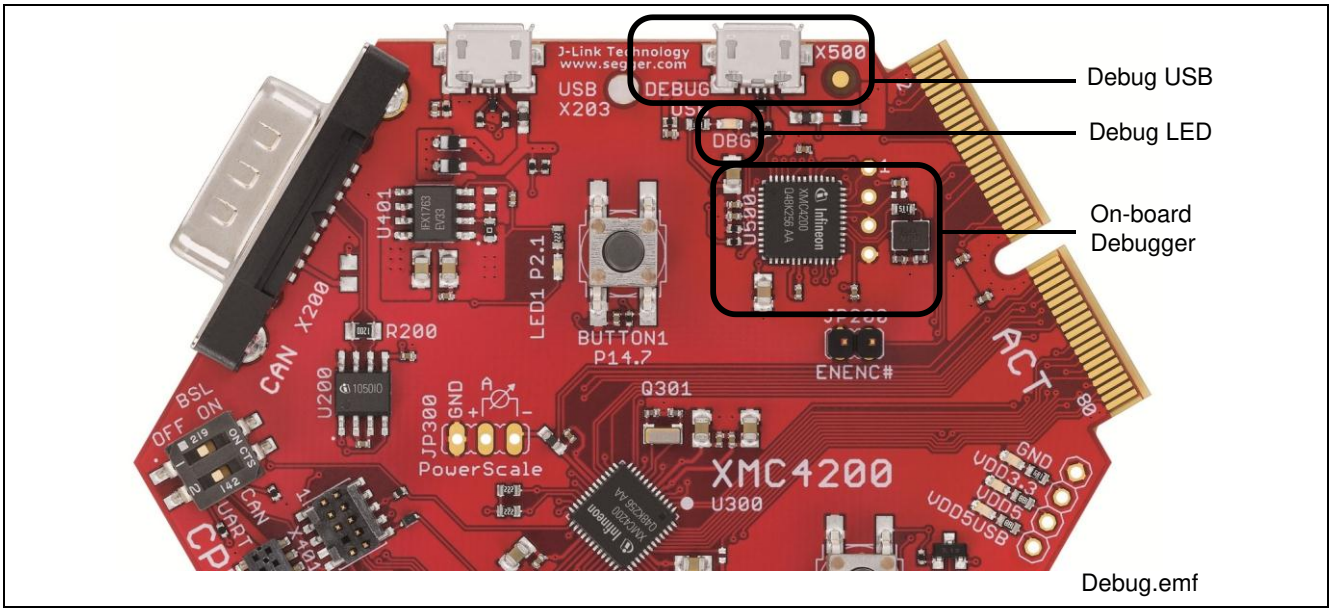

Figure 12 On-board Debugger

When using an external debugger connected to the 10pin/20pin Cortex Debug Connector, the on-board debugger is switched off.

When using the USB virtual COM port function of the on-board debugger the on-board CAN interface is disabled through the switches U301 and U303.

2.7.2 Cortex Debug Connector (10-pin)

The CPU_42A-V1 board supports Serial Wire Debug operation and Serial Wire Viewer operation (via the SWO signal when Serial Wire Debug mode is used) through the 10-pin Cortex Debug Connector.

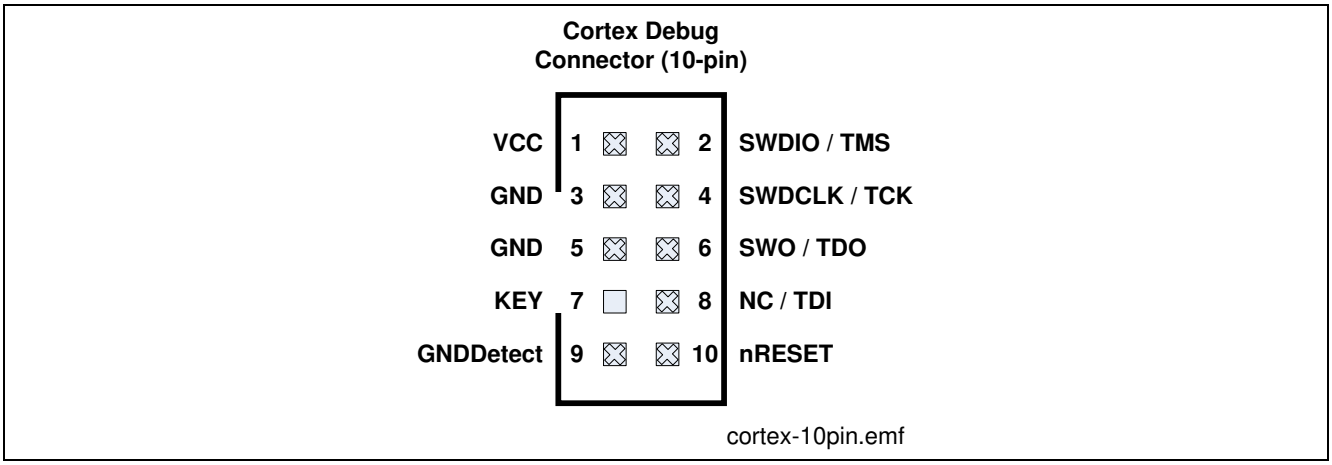

Figure 13 Cortex Debug Connector (10-pin)

Table 5 Cortex Debug Connector (10 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)

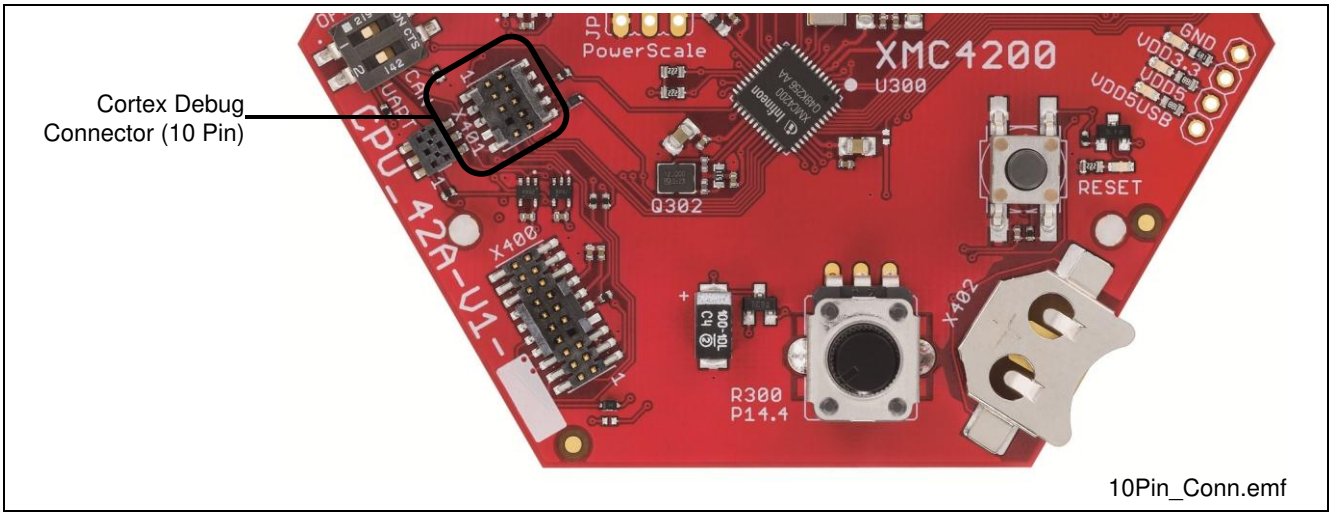

Figure 14 Cortex Debug Connector (10-pin) Layout

2.7.3 Cortex Debug+ ETM Connector (20-pin)

The CPU_42A-V1 board supports Serial Wire Debug operation, Serial Wire viewer operation (via SWO connection when Serial Wire Debug mode is used) through the 20-pin Cortex Debug+ ETM Connector. The board does not support the Instruction Trace operation.

JTAG Debug operation additionally would require the TDI (P0.7) signal. By default the TDI signal is disconnected from the Cortex Debug Connectors by a not assembled resistor R410, because the port pin P0.7 is used by the Actuator boards connected to the ACT satellite connector.

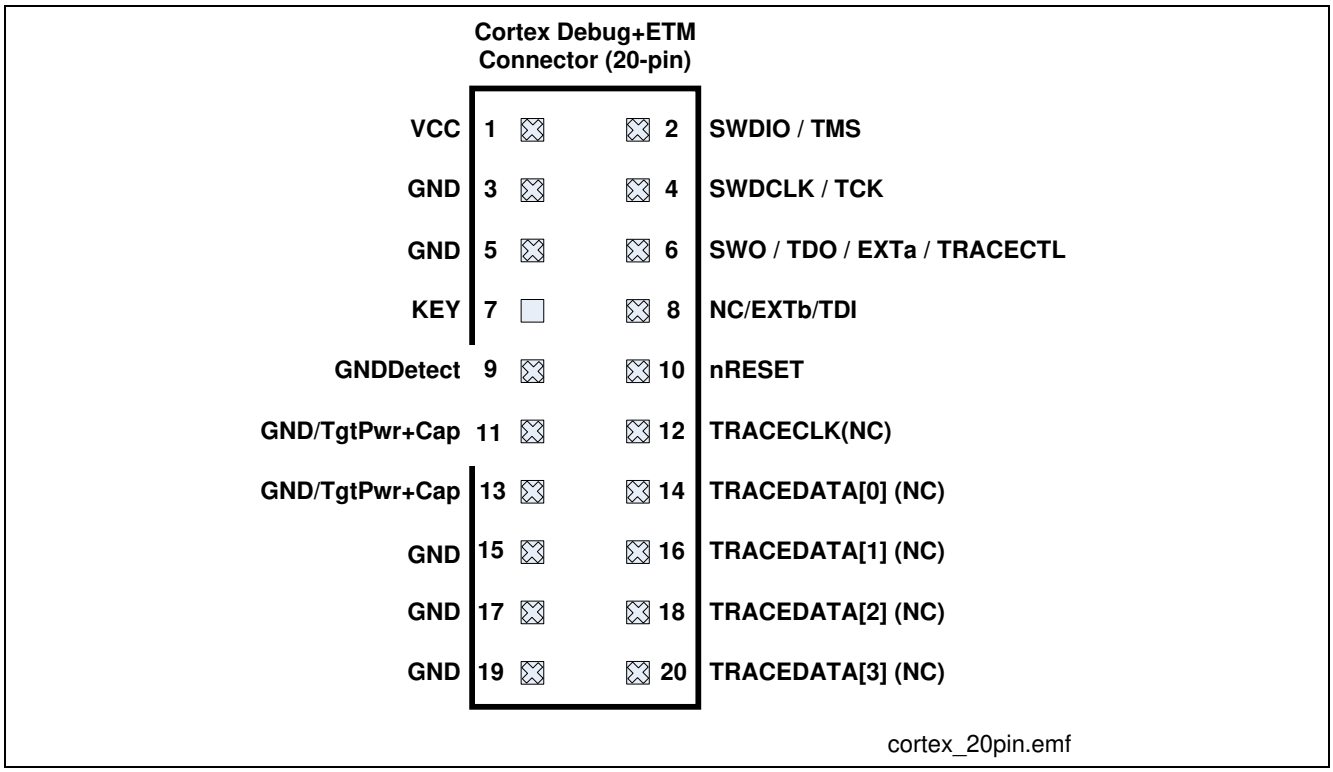

Figure 15 Cortex Debug+ETM Connector (20-pin)

Table 6 Cortex Debug+ ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)
11	GND/TgtPwr+Cap	Ground	Ground
12	TRACECLK	TRACECLK	TRACECLK
13	GND/TgtPwr+Cap	Ground	Ground
14	TRACEDATA[0]*	TRACEDATA[0]	TRACEDATA[0]
15	GND	Ground	Ground

Table 6 Cortex Debug+ ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
16	TRACEDATA[1]*	TRACEDATA[1]	TRACEDATA[1]
17	GND	Ground	Ground
18	TRACEDATA[2]*	TRACEDATA[2]	TRACEDATA[2]
19	GND	Ground	Ground
20	TRACEDATA[3]*	TRACEDATA[3]	TRACEDATA[3]

*Note: * Not connected on board*

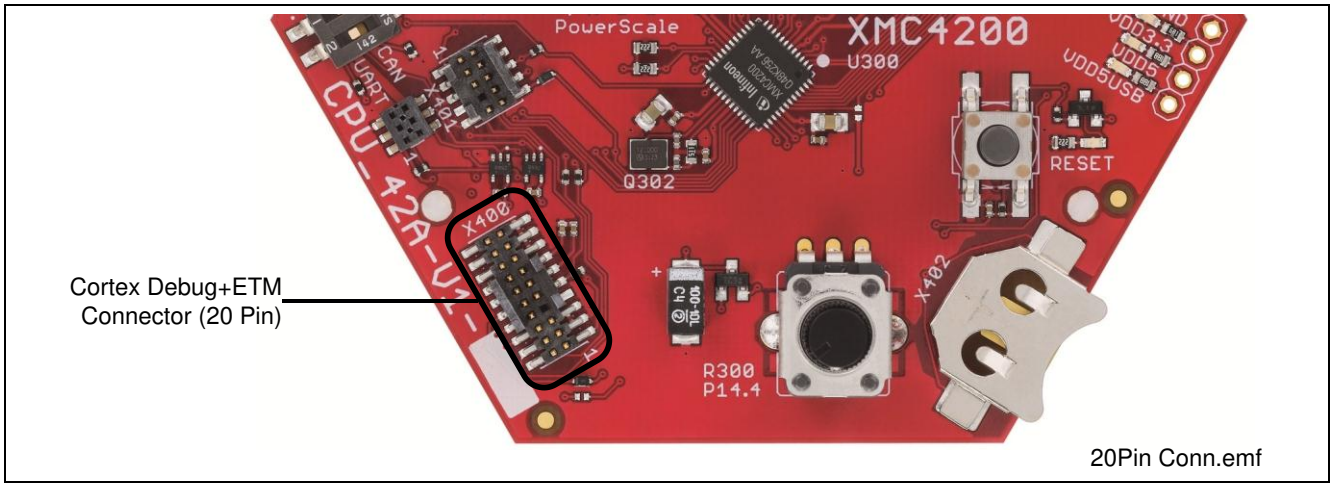

Figure 16 Cortex Debug+ ETM Connector (20-pin) Layout

2.8 USB

The XMC4200 supports USB interface in device mode. The power is expected through VBUS (pin 1) from an external host (e.g. PC). When the current consumption of the application running on the Hexagon Application system is higher than 500 mA, power from an external source through satellite cards shall be used.

Note: Some PCs, notebooks or hubs have a weak USB supply which is not sufficient for proper supply. In this case use an external 5 Volt power supply or a powered USB hub.

The VBUS function can be mapped to the HIB_IO_0 pin. A voltage divider (R205/R206) limits the voltage level at the HIB_IO_0 to maximum 3.3V.

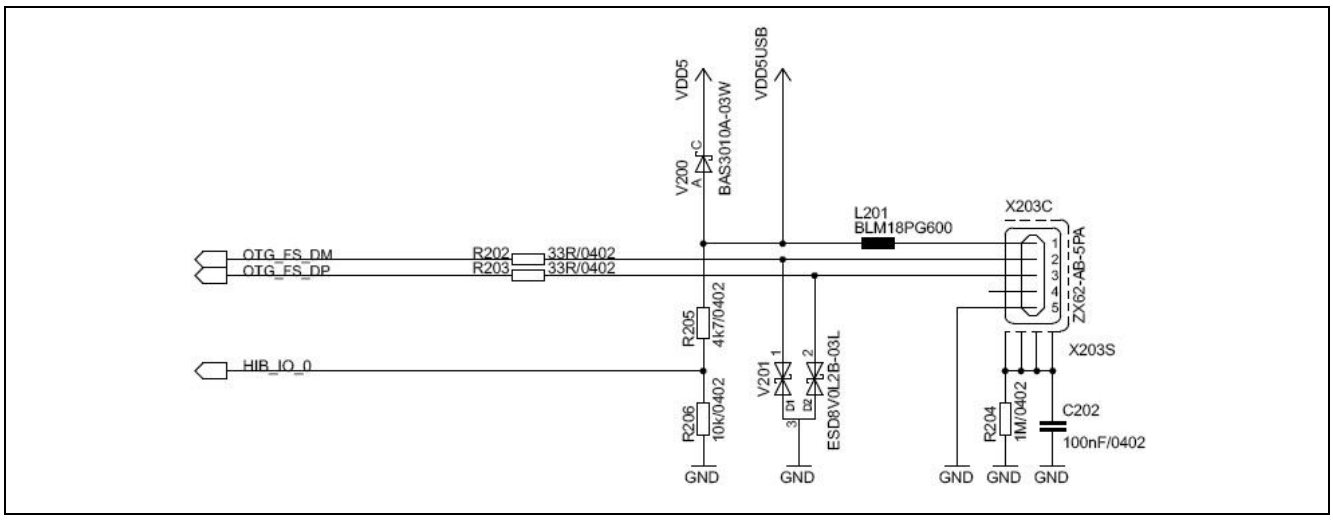

Figure 17 USB Connector

Table 7 USB micro AB connector Pinout

Pin No.	Pin Name	Pin Description
1	VBUS	5 V
2	D-	Data Minus
3	D+	Data Plus
4	ID	Identification
5	GND	Ground

2.9 RTC

The XMC4200 CPU has two power domains, the Core Domain and the Hibernate Domain.

The Core Domain (VDDP pins) is connected to the VDD3.3 rail. An on-board LDO voltage regulator generates VDD3.3 (3.3 V) out of VDD5 (5 V).

The Hibernate Domain is powered via the auxiliary supply pin VBAT, which is supplied by either a 3 V coin cell (size 1216, 1220 or 1225) plugged into the battery holder or 3.3 V (VDD3.3) generated by the on-board voltage regulator.

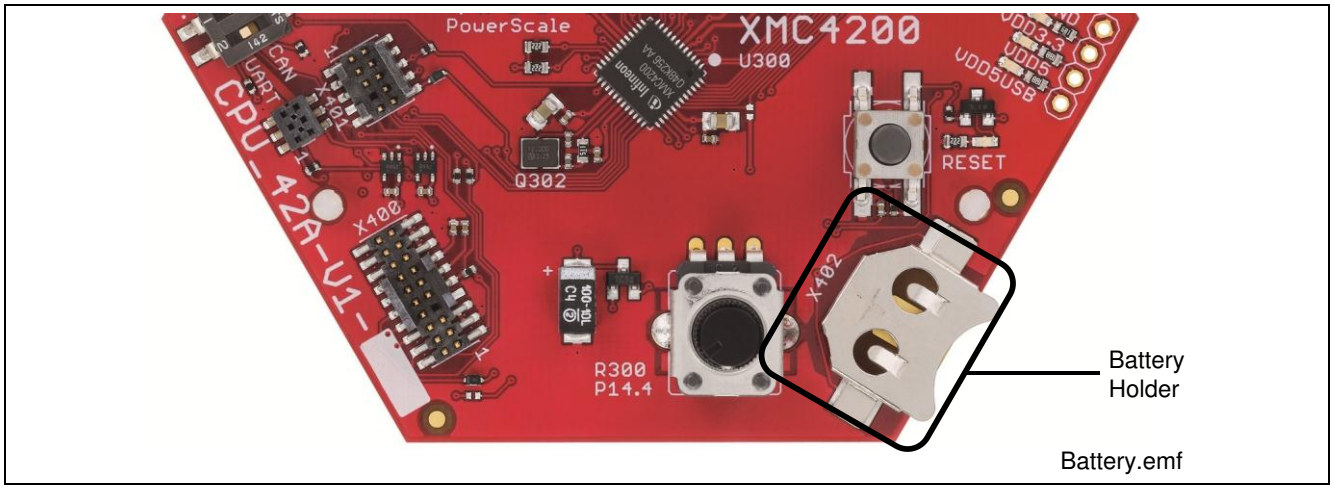

Figure 18 Battery Holder for Coin Cells

The Real Time Clock (RTC) is located in the hibernate domain. Even if the Core Domain is not powered the Hibernate Domain will operate if VBAT is supplied. The RTC keeps running as long as the Hibernate Domain is powered via the auxiliary supply VBAT.

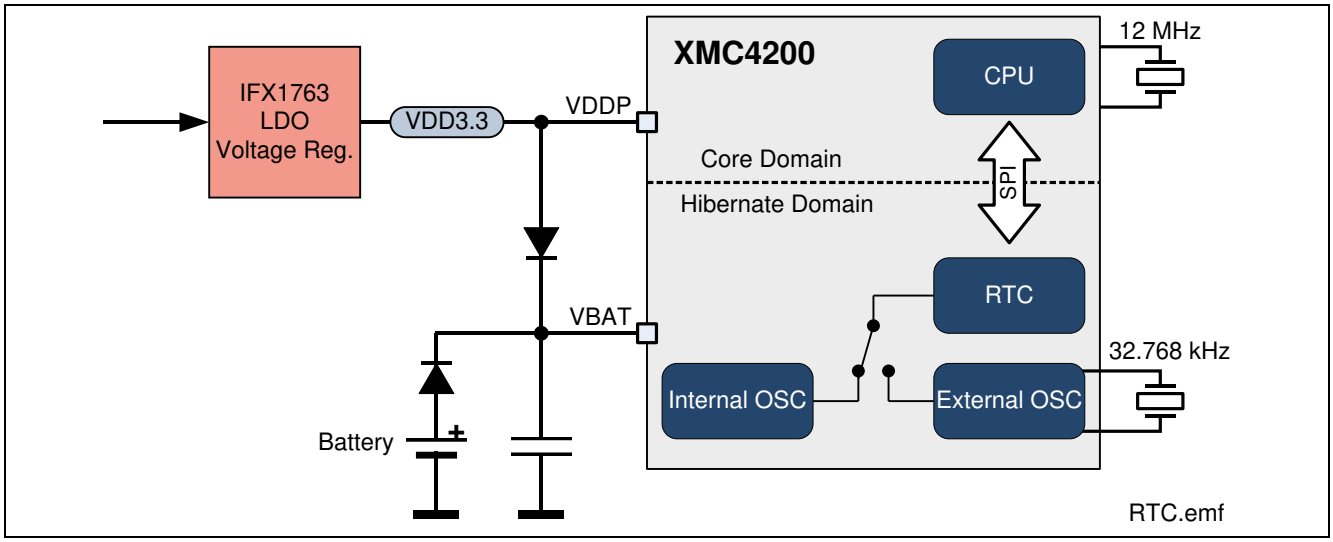

Figure 19 XMC4200 Power Domains and Real Time Clock

2.10 User LEDs and User Button

The port pin P2.1 of the XMC4200 is connected to LED V300. More User LED's are available through the I2C GPIO expander on most of the satellite cards.

Table 8 User LEDs

LED	Connected to Port Pin
V300	GPIO P2.1 [1]

[1] If Serial Wire Viewer is used, the User LED at P2.1 is flickering and cannot freely be programmed, because the Serial Wire Viewer function is overlaid with the GPIO function at P2.1.

One User Buttons SW301 is available at GPIO P14.7 of the XMC4200.

Table 9 User Buttons

Button	Connected to Pin
BUTTON1 / SW301	GPIO P14.7

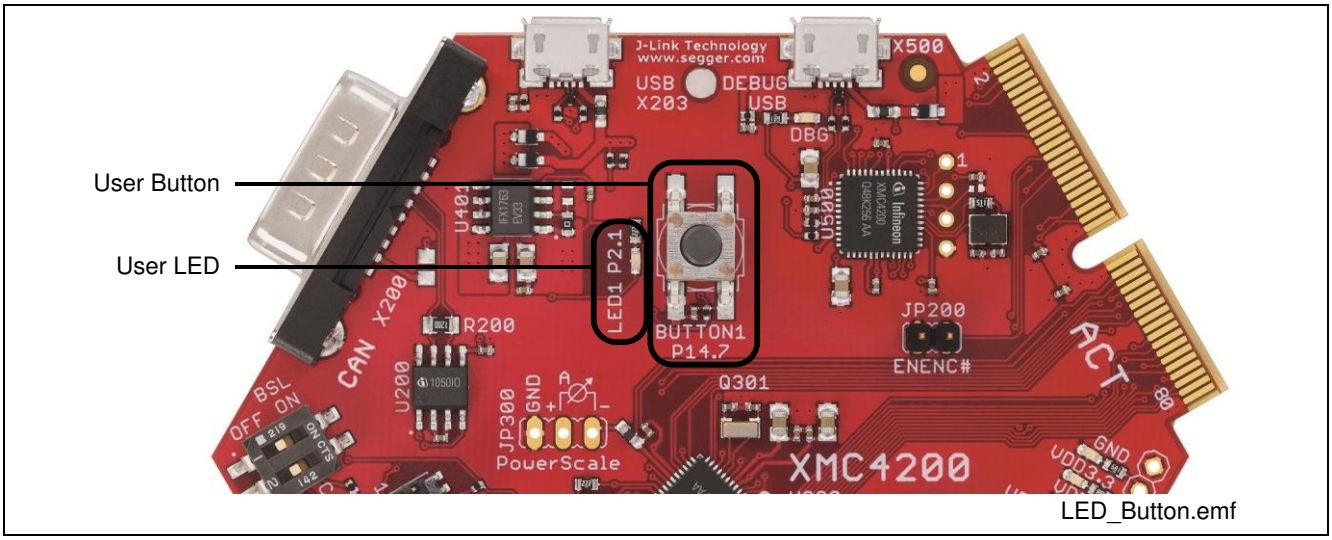

Figure 20 User LED and User Button

2.11 Potentiometer

The CPU_42A-V1 board provides a potentiometer POT1 for ease of use and testing of the on-chip analog to digital converter. The potentiometer is connected to the analog input G0_CH4 (P14.4). The analog output voltage of the potentiometer ranges from 0 V to 3.3 V.

Table 10 Potentiometer

Potentiometer	Connected to Port Pin
P300	P14.4 / G0_CH4 (Group 0, channel 4)

2.12 Satellite Connector

The CPU_42A-V1 board provides an ACT (Actuator) satellite connector for application extension by satellite cards.

Note: Satellite cards shall be connected to their matching satellite connectors only. (For e.g. ACT satellite cards shall be connected to ACT satellite connector only)

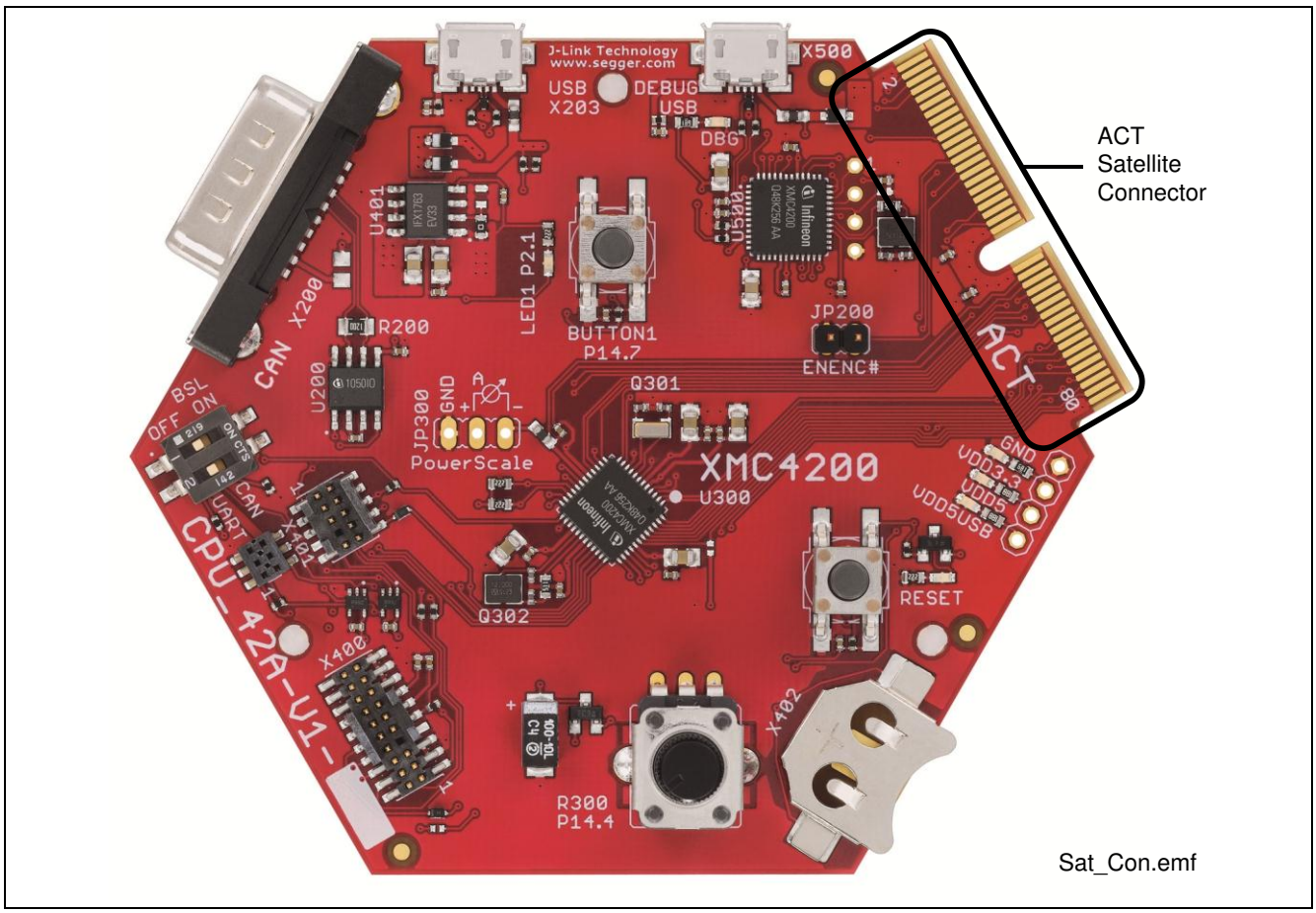

Figure 21 Satellite Connector

2.12.1 ACT Satellite Connector

The ACT satellite connector on the CPU_42A-V1 board allows interface expansion through ACT satellite cards.

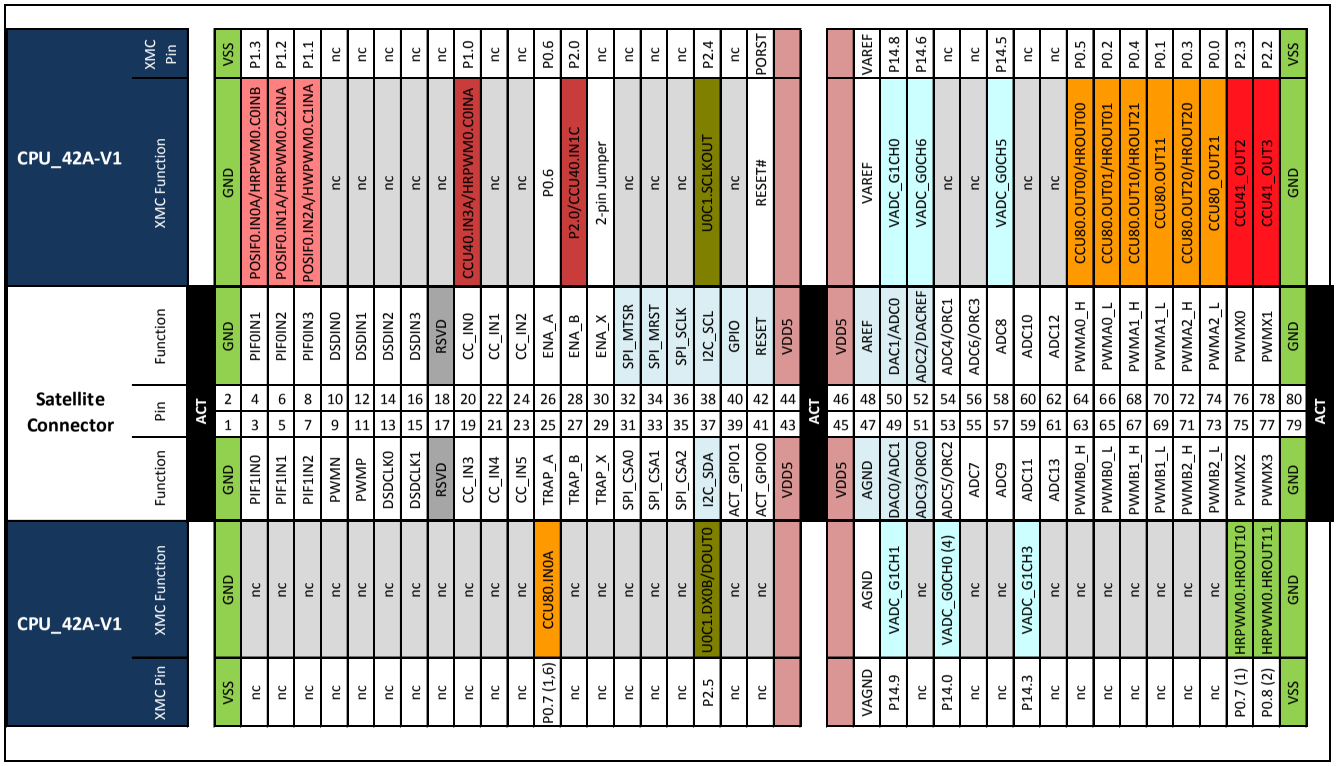

Figure 22 Satellite Connector Type ACT

(1) P0.7 can also be used for JTAG Debugging (TDI)
(2) P0.8 is used as TRST in order to enable JTAG Debug
(3) This pin is connected with the satellite connector via an analog switch
(4) This ADC input does not support “Out of Range Detection”
(5) This pin must be “enabled” by a solder jump.
(6) Support High Resolution PWM

3 Production Data

3.1 Schematics

This chapter contains the schematics for the CPU board:

- Satellite Connector, USB, CAN
- XMC4200
- Power and Debug
- On-board Debugger

The board has been designed with Eagle. The full PCB design data of this board can also be downloaded from www.infineon.com/xmc-dev.

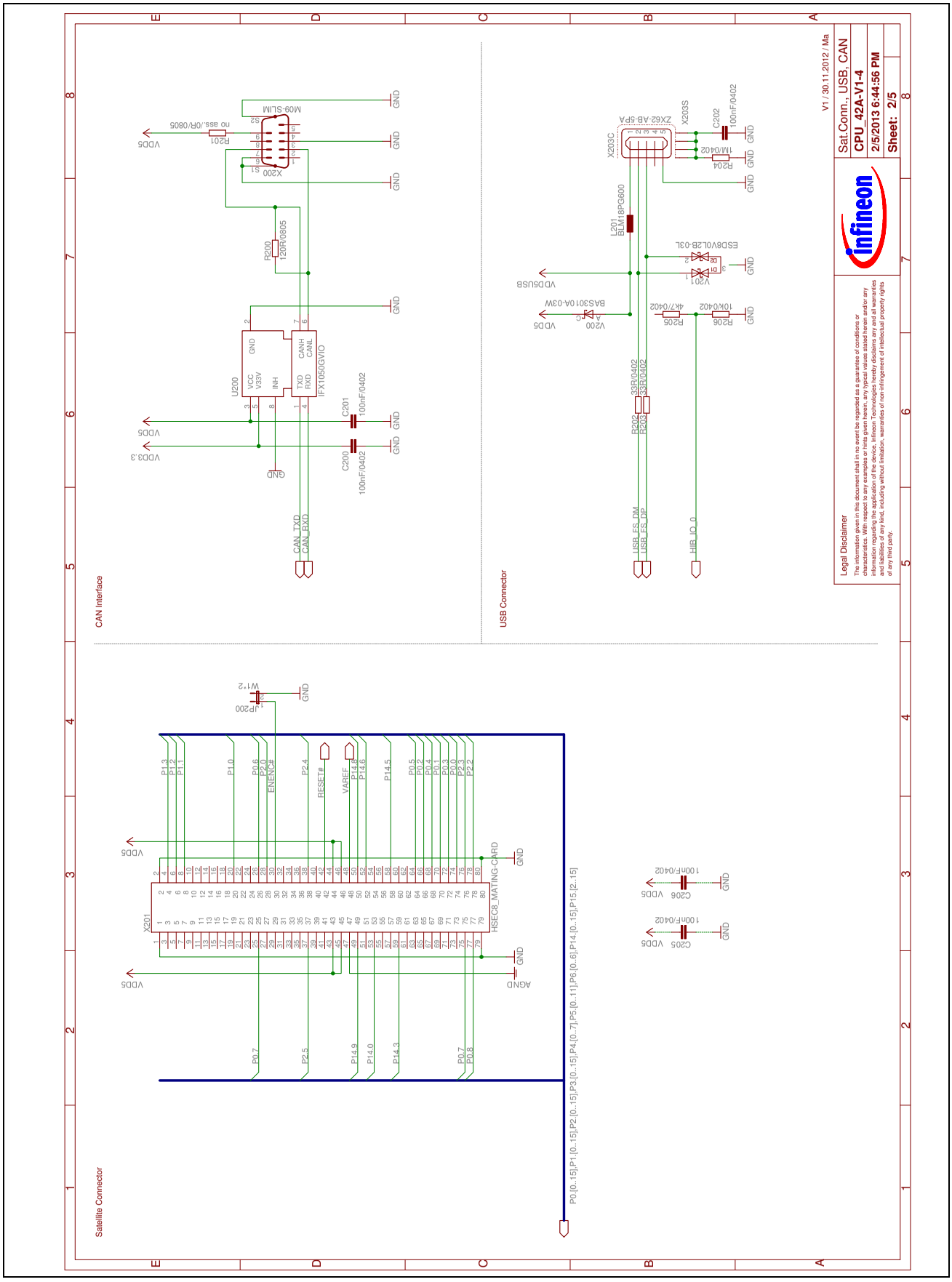

Figure 23 Satellite Connector, USB, CAN