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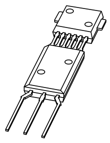


KMA210

Programmable angle sensor

Rev. 2 — 7 December 2011 **Product data sheet**

1. Product profile

1.1 General description

The KMA210 is a magnetic angle sensor module. The MagnetoResistive (MR) sensor bridges, the mixed signal Integrated Circuit (IC) and the required capacitances are integrated into a single package.

This angular measurement module KMA210 is pre-programmed, pre-calibrated and therefore, ready to use.

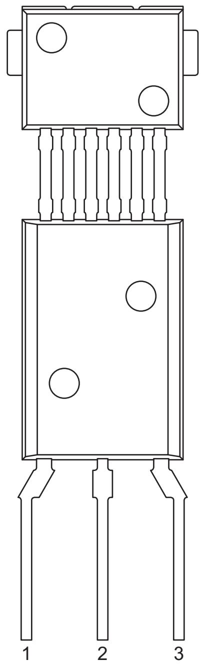
The KMA210 allows user-specific adjustments of angular range, zero angle and clamping voltages. The settings are stored permanently in a non-volatile memory.

1.2 Features and benefits

- High precision sensor for magnetic angular measurement
- Single package sensor module with integrated filters for improved ElectroMagnetic Compatibility (EMC)
- Automotive qualified in accordance with AEC-Q100 Rev-G
- Programmable user adjustments, including zero angle and angular range
- Fail-safe non-volatile memory with write protection using lock bit
- Independent from magnetic field strength above 35 kA/m
- Ready to use without external components
- High temperature range up to 160 °C
- Ratiometric analog output voltage
- Overvoltage protection up to 16 V
- Programming via One-Wire Interface (OWI)
- User-programmable 32-bit identifier
- Magnet-loss, power-loss and broken bond wire detection
- Factory calibrated

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline
1	V_{DD}	supply voltage	
2	GND	ground	
3	OUT/DATA	analog output or data interface	

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
KMA210	-	plastic single-ended multi-chip package; 6 interconnections; 3 in-line leads	SOT1288

4. Functional diagram

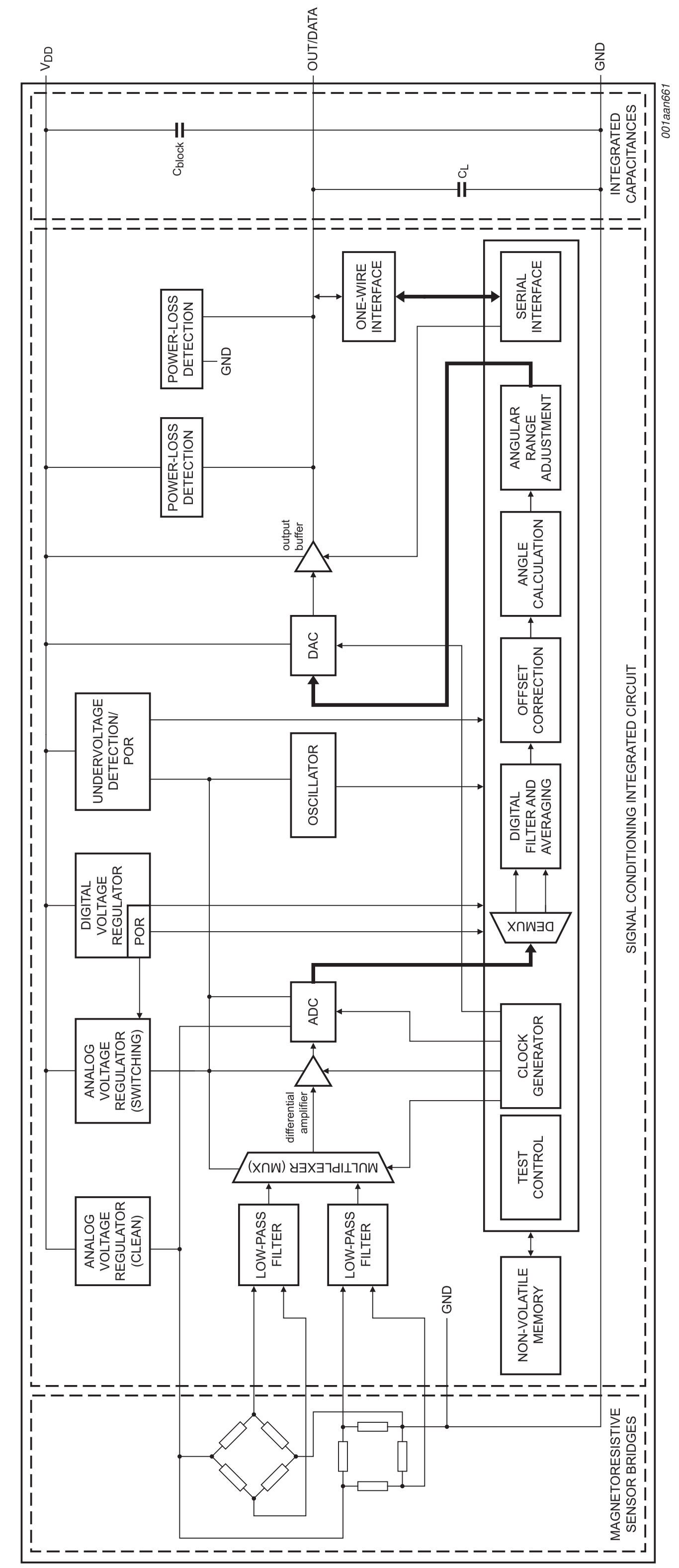


Fig 1. Functional diagram of KMA210

5. Functional description

The KMA210 amplifies two orthogonal differential signals from MR sensor bridges and converts them into the digital domain. The angle is calculated using the COordinate Rotation DIgital Computer (CORDIC) algorithm. After a digital-to-analog conversion the analog signal is provided to the output as a linear representation of the angular value. Zero angle, clamping voltages and angular range are programmable. In addition, two 16-bit registers are available for customer purposes, such as sample identification.

The KMA210 comprises a Cyclic Redundancy Check (CRC) and an Error Detection and Correction (EDC), as well as magnet-loss and broken bond wire detection to ensure a fail-safe operation. A power-loss detection circuit pulls the analog output to the remaining connection, if either the supply voltage or the ground line of the mixed signal IC is interrupted.

After multiplexing the two MR Wheatstone bridge signals and their successive amplification, the signal is converted into the digital domain by an Analog-to-Digital Converter (ADC). Further processing is done within an on-chip state machine. This includes offset cancellation, calculation of the mechanical angle using the CORDIC algorithm, as well as zero angle and angular range adjustment. The internal Digital-to-Analog Converter (DAC) and the analog output stage are used for conversion of the angle information into an analog output voltage, which is ratiometric to the supply voltage.

The configuration parameters are stored in a user-programmable non-volatile memory. The OWI (accessible using pin OUT/DATA) is used for accessing the memory. In order to protect the memory content a lock bit can be set. After locking the non-volatile memory, its content cannot be changed anymore.

5.1 Angular measurement directions

The differential signals of the MR sensor bridges depend only on the direction of the external magnetic field strength H_{ext}, which is applied parallel to the plane of the sensor. In order to obtain a correct output signal, the minimum saturation field strength has to be exceeded.

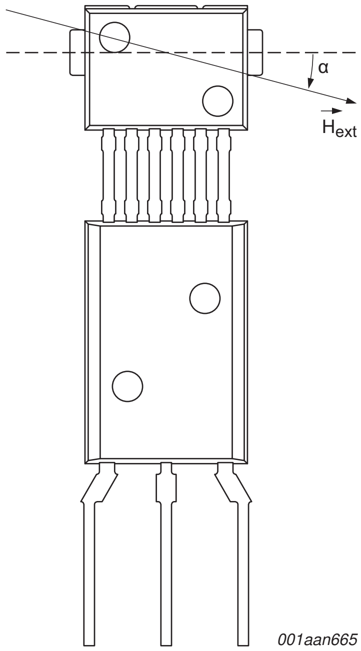


Fig 2. Angular measurement directions

Since the Anisotropic MR (AMR) effect is periodic over 180°, the sensor output is also 180°-periodic, where the angle is calculated relative to a freely programmable zero angle. The dashed line indicates the mechanical zero degree position.

6. Analog output

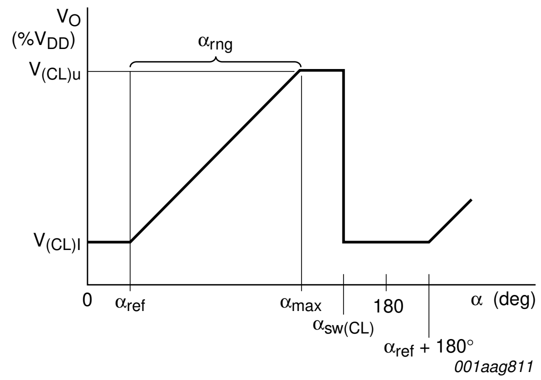
The KMA210 provides one analog output signal on pin OUT/DATA. The measured angle α is converted linearly into a value, which is ratiometric to the supply voltage V_{DD}. Either a positive or a negative slope is provided for this purpose.

Table 3 describes the analog output behavior for a positive slope. If for example, a magnetic field angle, above the programmed maximum angle α_{max}, but below the clamp switch angle $\alpha_{sw(CL)}$ is applied to the sensor, then analog output is set to the upper clamping voltage. If the magnetic field angle is larger than the clamp switch angle, the analog output switches from upper to lower clamping voltage. In the case of a negative slope, the clamping voltages are changed.

Table 3. Analog output behavior for a positive slope

Magnetic field angle	Analog output
$\alpha_{max} < \alpha < \alpha_{sw(CL)}$	$V_{(CL)u}$
$\alpha_{sw(CL)} < \alpha < \alpha_{ref} + 180°$	$V_{(CL)l}$

The analog output voltage range encodes both angular and diagnostic information. A valid angle value is between the upper and lower clamping voltage. If the analog output is in the diagnostic range, that is below 4 %V_{DD} or above 96 %V_{DD}, an error condition has been detected. The analog output repeats every 180°.



$\alpha_{max} = \alpha_{ref} + \alpha_{rng}$

Fig 3. Characteristic of the analog output

7. Diagnostic features

The KMA210 provides several diagnostic features:

7.1 CRC and EDC supervision

The KMA210 includes a supervision of the programmed data. At power-on, a CRC of the non-volatile memory is performed. Furthermore the memory is protected against bit errors. Every 16-bit data word is saved internally as a 22-bit word for this purpose. The protection logic corrects any single-bit error in a data word, while the sensor continues in normal operation mode. Double-bit errors per word will be detected and switches the device into diagnostic mode.

7.2 Magnet-loss detection

If the applied magnetic field strength is not sufficient, the KMA210 can raise a diagnostic condition. In order to enter the diagnostic mode, due to magnet-loss, the detection has to be enabled first. The device can be programmed into active diagnostic mode, where the output is driven below 4 $\%V_{DD}$ or above 96 $\%V_{DD}$.

7.3 Power-loss detection

The power-loss detection circuit enables the detection of an interrupted supply or ground line of the mixed signal IC in normal operation mode up to the maximum operating supply voltage. In the case of a power-loss condition, two internal switches in the sensor are closed, connecting the pin of the analog output to the supply voltage and the ground pins.

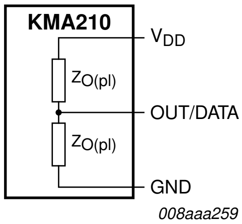


Fig 4. Equivalent output circuit in case of a power-loss condition

Table 4 describes the power-loss behavior and gives the resulting output voltage depending on the interrupted supply or ground line and the load resistance.

Table 4. Power-loss behavior

Load resistance	Interrupted supply line	Interrupted ground line
$R_{L(ext)} > 5\ k\Omega$	$V_O \leq 4\ \%V_{DD}$	$V_O \geq 96\ \%V_{DD}$

7.4 Broken bond wire detection

The broken bond wire detection circuit enables the detection of an interrupted supply or ground line of the MR sensor bridge. In the case of a broken bond wire the device goes into diagnostic mode and a status bit is set.

7.5 Low supply voltage detection and overvoltage protection

If the supply voltage is below the switch-off threshold voltage, a status bit is set and the device goes into diagnostic mode. If the supply voltage is above the overvoltage switch-on threshold voltage, the device enters diagnostic mode. Table 5 describes the system behavior depending on the voltage range of the supply voltage.

Table 5. System behavior

Supply voltage	State	Description
0 V to ≅ 1.8 V	start-up power	The output buffer drives an active LOW or is powered down, but the switches of the power-loss detection circuit are not fully opened and set the output to a level between ground and half the supply voltage.
≅ 1.8 V to V_{POR}	power-on reset	The power-loss charge pump is fully operational and turns the switches of the detection circuit off. The output buffer drives an active LOW and sets the output to the lower diagnostic level. During the reset phase all circuits are in reset and/or Power-down mode.
V_{POR} to $V_{th(on)}$ or $V_{th(off)}$	initialization	The digital core and the oscillator are active. After reset the content of the non-volatile memory is copied into the shadow registers. The output buffer drives an active LOW and sets the output to the lower diagnostic level.
$V_{th(on)}$ or $V_{th(off)}$ to minimum V_{DD}	functional operation	All analog circuits are active and the measured angle is available at the analog output. Not all parameters are within the specified limits.

Table 5. System behavior *…continued*

Supply voltage	State	Description
Minimum V_{DD} to maximum V_{DD}	normal operation	All analog circuits are active and the measured angle is available at the analog output. All parameters are within the specified limits.
Maximum V_{DD} to $V_{th(ov)}$	functional operation	All analog circuits are active and the measured angle is available at the analog output. Not all parameters are within the specified limits.
$V_{th(ov)}$ to 16 V	overvoltage	The digital core and the oscillator are active but all other circuits are in Power-down mode. The output is set to the lower diagnostic level.

Table 6 describes the diagnostic behavior and the resulting output voltage depending on the error case. Furthermore the duration and termination condition to enter and leave the diagnostic mode are given, respectively.

Table 6. Diagnostic behavior

Diagnostic condition	Duration	Analog output	Termination condition
Low voltage	1 μs < t < 10 μs	≤ 4 %V_{DD}	functional or normal operation
Overvoltage	1 μs < t < 10 μs	≤ 4 %V_{DD}	functional or normal operation
Checksum error	n/a	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[2]	power-on reset[1]
Double-bit error	n/a	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[2]	power-on reset[1]
Magnet-loss	0.5 ms < t < 6 ms	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[2]	magnet present[1]
Power-loss	≤ 2 ms	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[2]	power-on reset
Broken bond wire	0.2 ms < t < 1 ms	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[2]	power-on reset[1]

[1] Status bit stays set in command register until power-on reset.

[2] Depending on the diagnostic level setting.

8. Limiting values

Table 7. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.3	+16	V
V_O	output voltage			−0.3	+16	V
$V_{O(ov)}$	overvoltage output voltage	T_{amb} < 140 °C at t < 1 h	[1]	$V_{th(ov)}$	16	V
I_r	reverse current	T_{amb} < 70 °C		-	150	mA
T_{amb}	ambient temperature			−40	+160	°C
$T_{amb(pr)}$	programming ambient temperature			10	70	°C
T_{stg}	storage temperature			−40	+125	°C
Non-volatile memory						
$t_{ret(D)}$	data retention time	T_{amb} = 50 °C		17	-	year
$N_{endu(W\_ER)}$	write or erase endurance	$T_{amb(pr)}$ = 70 °C		100	-	cycle

[1] Overvoltage on analog output and supply within the specified operating voltage range.

9. Recommended operating conditions

Table 8. Operating conditions

In a homogenous magnetic field.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage		[1]	4.5	5.0	5.5	V
T_{amb}	ambient temperature			–40	-	+160	°C
$T_{amb(pr)}$	programming ambient temperature			10	-	70	°C
$C_{L(ext)}$	external load capacitance		[1][2]	0	-	22	nF
			[2][3]	0	-	6.8	nF
$R_{L(ext)}$	external load resistance		[4]	5	-	∞	kΩ
H_{ext}	external magnetic field strength			35	-	-	kA/m

[1] Normal operation mode.

[2] Between ground and analog output.

[3] Command mode.

[4] Power-loss detection is only possible with a load resistance within the specified range connected to the supply or ground line.

10. Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		145	K/W

11. Characteristics

Table 10. Supply current

Characteristics are valid for the operating conditions, as specified in Section 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}	supply current		[1][2]	5	-	10.5	mA
			[3][4]	-	-	13	mA
$I_{off(ov)}$	overvoltage switch-off current		[5]	-	-	6	mA

[1] Normal operation and diagnostic mode excluding overvoltage and undervoltage within the specified operating supply voltage range.

[2] Without load current at the analog output.

[3] Normal operation and diagnostic mode over full voltage range up to limiting supply voltage at steady state.

[4] With minimum load resistance at the analog output.

[5] Diagnostic mode for a supply voltage above the overvoltage threshold voltage up to the limiting supply voltage.

Table 11. Power-on reset

Characteristics are valid for the operating conditions, as specified in Section 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(on)}$	switch-on threshold voltage	analog output switches on, if $V_{DD} > V_{th(on)}$	-	4.30	4.45	V
$V_{th(off)}$	switch-off threshold voltage	analog output switches off, if $V_{DD} < V_{th(off)}$	3.90	4.10	-	V
V_{hys}	hysteresis voltage	$V_{hys} = V_{th(on)} - V_{th(off)}$	0.1	0.2	-	V
V_{POR}	power-on reset voltage	IC is initialized	-	3.3	3.6	V
$V_{th(ov)}$	overvoltage threshold voltage	analog output switches off, if $V_{DD} > V_{th(ov)}$	6.5	7.5	8.0	V
$V_{hys(ov)}$	overvoltage hysteresis voltage		0.1	0.3	-	V

Table 12. Module performance

Characteristics are valid for the operating conditions, as specified in Section 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{res}	angle resolution		[1]	-	-	0.04	deg
α_{max}	maximum angle	programmable angular range for $V_{(CL)u} - V_{(CL)l} \geq 80\ \%V_{DD}$	[2]	5	-	180	deg
α_{ref}	reference angle	programmable zero angle	[2]	0	-	180	deg
$V_{O(nom)}$	nominal output voltage	at full supply operating range		5	-	95	$\%V_{DD}$
$V_{O(udr)}$	upper diagnostic range output voltage		[3][4][5]	96	-	100	$\%V_{DD}$
$V_{O(ldr)}$	lower diagnostic range output voltage		[3][4][5]	0	-	4	$\%V_{DD}$
$V_{(CL)u}$	upper clamping voltage		[4][5][6]	40	-	95	$\%V_{DD}$
$V_{(CL)l}$	lower clamping voltage		[4][5][6]	5	-	30.5	$\%V_{DD}$
$\Delta V_{(CL)}$	clamping voltage variation	deviation from programmed value	[4][5]	−0.3	-	+0.3	$\%V_{DD}$
$V_{n(o)(RMS)}$	RMS output noise voltage	equivalent power noise	[1][4]	-	0.4	2.5	mV
$\Delta\phi_{lin}$	linearity error	temperature range −40 °C to +160 °C	[4][7]	−1.2	-	+1.2	deg
		temperature range −40 °C to +140 °C	[4][7]	−1	-	+1	deg
$\Delta\phi_{temp}$	temperature drift error	temperature range −40 °C to +160 °C	[1][4][7][8]	-	-	0.8	deg
		temperature range −40 °C to +140 °C	[1][4][7][8]	-	-	0.65	deg
$\Delta\phi_{temp\vert RT}$	temperature drift error at room temperature	temperature range −40 °C to +160 °C	[7][8][9]	-	-	0.65	deg
		temperature range −40 °C to +140 °C	[7][8][9]	-	-	0.55	deg
$\Delta\phi_{hys}$	hysteresis error	referred to input	[4][7]	-	-	0.09	deg
$\Delta\phi_{\mu lin}$	microlinearity error	referred to input	[4][7]	−0.1	-	+0.1	deg

Table 12. Module performance *…continued*

Characteristics are valid for the operating conditions, as specified in Section 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta\phi_{ang}$	angular error	temperature range −40 °C to +160 °C	[4][7] [10]	−1.35	-	+1.35	deg
		temperature range −40 °C to +140 °C	[4][7] [10]	−1.1	-	+1.1	deg
m_{ang}	slope of angular error		[4][7] [10]	-	-	0.04	deg/deg
$Z_{O(pl)}$	power-loss output impedance	impedance to remaining supply line in case of lost supply voltage or lost ground		-	-	210	Ω

[1] At a nominal output voltage between 5 %V_{DD} and 95 %V_{DD} and a maximum angle of α_{max} = 180°.

[2] In steps of resolution < 0.022°.

[3] Activation is dependent on the programmed diagnostic mode.

[4] At a low-pass filtered analog output with a cut-off frequency of 0.7 kHz.

[5] Settling to these values is limited by 0.7 kHz low-pass filtering of analog output.

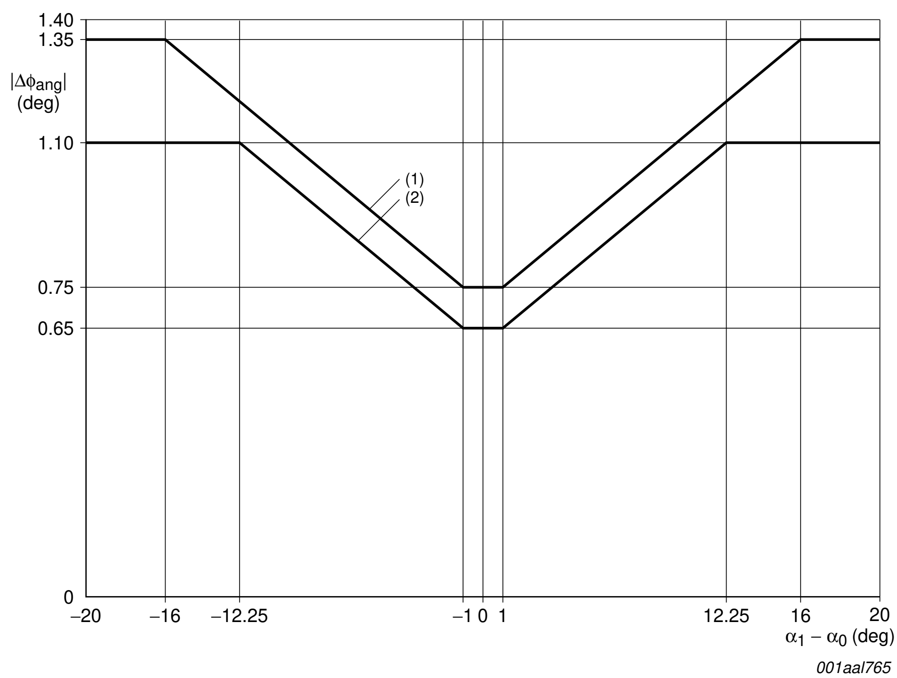
[6] In steps of 0.02 %V_{DD}.

[7] Definition of errors is given in Section 12.

[8] Based on a 3σ standard deviation.

[9] Room temperature is given for an ambient temperature of 25 °C.

[10] Graph of angular error is shown in Figure 5.



(1) −40 °C to +160 °C

(2) −40 °C to +140 °C

Fig 5. Envelope curve for the magnitude of angular error

Table 13. Dynamics

Characteristics are valid for the operating conditions, as specified in Section 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{on}	turn-on time	until first valid result	-	-	5	ms
f_{upd}	update frequency		2.4	3.125	-	kHz
t_s	settling time	after an ideal mechanical angle step of 45°, until 90 % of the final value is reached	-	-	1.8	ms
$t_{cmd(ent)}$	enter command mode time	after power on	20	-	30	ms
$t_{rec(ov)}$	overvoltage recovery time	after overvoltage	-	-	4	ms

Table 14. Digital interface

Characteristics are valid for the operating conditions, as specified in Section 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		80	-	-	$\%V_{DD}$
V_{IL}	LOW-level input voltage		-	-	20	$\%V_{DD}$
V_{OH}	HIGH-level output voltage	$I_O = 2$ mA	80	-	-	$\%V_{DD}$
V_{OL}	LOW-level output voltage	$I_O = 2$ mA	-	-	20	$\%V_{DD}$
I_{od}	overdrive current	absolute value for overdriving the output buffer	-	-	20	mA
t_{start}	start time	LOW level before rising edge	5	-	-	μs
t_{stop}	stop time	HIGH level before falling edge	5	-	-	μs
T_{bit}	bit period	minimum period may be limited by the load capacitance	10	-	100	μs
ΔT_{bit}	bit period deviation	deviation between received clock and sent clock	$0.8T_{bit}$	$1T_{bit}$	$1.2T_{bit}$	μs
t_{w0}	pulse width 0		$0.175T_{bit}$	$0.25T_{bit}$	$0.375T_{bit}$	μs
t_{w1}	pulse width 1		$0.625T_{bit}$	$0.75T_{bit}$	$0.825T_{bit}$	μs
t_{to}	time-out time	communication reset guaranteed after maximum t_{to}	-	-	220	μs
$t_{tko(slv)}$	slave takeover time	duration of LOW level for slave takeover	1	-	5	μs
$t_{tko(mas)}$	master takeover time	duration of LOW level for master takeover	$0T_{bit}$	-	$0.5T_{bit}$	μs
t_{prog}	programming time	for a single memory address	20	-	-	ms
t_{cp}	charge pump time	waiting time after enabling the non-volatile memory charge pump clock	1	-	-	ms

Table 15. Internal capacitances

Characteristics are valid for the operating conditions, as specified in Section 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{block}	blocking capacitance	[1]	25	47	75	nF
C_L	load capacitance	[1]	1.1	2.2	3.3	nF

[1] Measured at 1 MHz.

12. Definition of errors

12.1 General

Angular measurement errors by the KMA210 result from linearity errors, temperature drift errors and hysteresis errors. Figure 6 shows the output signal of an ideal sensor, where the measured angle ϕ_{meas} corresponds ideally to the magnetic field angle α. This curve will further be denoted as angle reference line $\phi_{ref}(\alpha)$ with a slope of 0.5 $\%V_{DD}$/degree.

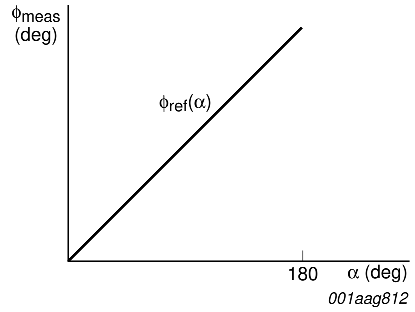


Fig 6. Definition of the reference line

The angular range is set to α_{max} = 180° and the clamping voltages are programmed to $V_{(CL)l}$ = 5 $\%V_{DD}$ and $V_{(CL)u}$ = 95 $\%V_{DD}$ for a valid definition of errors.

12.2 Hysteresis error

The hysteresis error $\Delta\phi_{hys}$ is defined as the maximum difference between the angles, given by the device output when performing a positive (clockwise) rotation and negative (counter clockwise) rotation over an angular range of 180°, measured at a constant temperature.

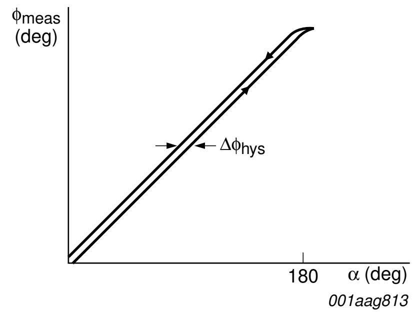


Fig 7. Definition of the hysteresis error

Equation 1 gives the mathematical description for the hysteresis value $\Delta\phi_{hys}$:

$$\Delta\phi_{hys}(\alpha) = \left|\phi_{meas}(\alpha \to 180^{\circ}) - \phi_{meas}(\alpha \to 0^{\circ})\right| \quad (1)$$

12.3 Linearity error

The KMA210 output signal deviation from a best straight line ϕ_{BSL}, with the same slope as the reference line, is defined as linearity error. The magnetic field angle is varied at fixed temperatures for measurement of this linearity error. The output signal deviation from the best straight line at the given temperature is the linearity error $\Delta\phi_{lin}$. It is a function of the magnetic field angle α and the temperature of the device T_{amb}.

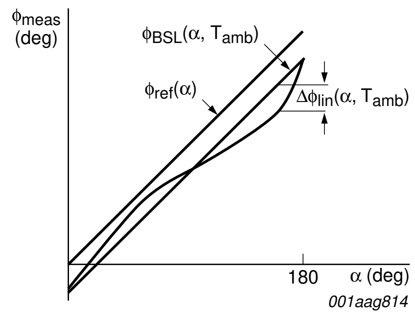


Fig 8. Definition of the linearity error

12.4 Microlinearity error

The microlinearity error $\Delta\phi_{\mu lin}$ is the device output deviation from 1°, if the magnetic field angle α is changed by $\Delta\alpha$ = 1°.

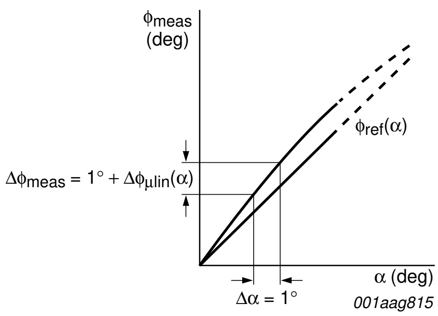


Fig 9. Definition of the microlinearity error

12.5 Temperature drift error

The temperature drift $\Delta\phi_{temp}$ is defined as the envelope over the deviation of the angle versus the temperature range. It is considered as the pure thermal effect.

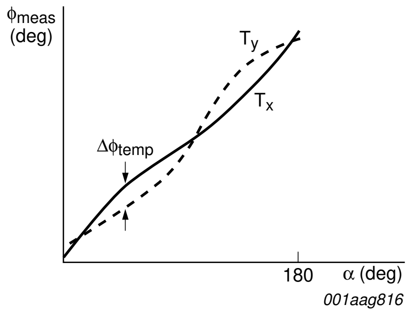


Fig 10. Definition of the temperature drift error

Equation 2 gives the mathematical description for temperature drift value $\Delta\phi_{temp}$:

$$\Delta\phi_{temp}(\alpha) = \left|\phi_{meas}(\alpha, T_x) - \phi_{meas}(\alpha, T_y)\right| \tag{2}$$

with:

T_x: temperature for maximum ϕ_{meas} at angle α

T_y: temperature for minimum ϕ_{meas} at angle α

The deviation from the value at room temperature $\Delta\phi_{temp|RT}$ describes the temperature drift of the angle, compared to the value, which the sensor provides at room temperature:

$$\Delta\phi_{temp|RT}(\alpha, T_{amb}) = \left|\phi_{meas}(\alpha, T_{amb}) - \phi_{meas}(\alpha, T_{RT})\right| \tag{3}$$

with:

T_{RT}: room temperature (25 °C)

12.6 Angular error

The angular error $\Delta\phi_{ang}$ is the error of angle difference measured by the sensor, if the mechanical angle deviates from α_0 to α_1. Here α_0 and α_1 are arbitrary angles within the angular range. The angle measurement at α_0 is the initially programmed reference angle, programmed by the customer at room temperature and zero hour upon production. The angle measurement at α_1 is made at any temperature within the ambient temperature range:

$$\Delta\phi_{ang} = (\phi_{meas}(\alpha_1, T_{amb}) - \phi_{meas}(\alpha_0, T_{RT})) - (\alpha_1 - \alpha_0) \tag{4}$$

with:

α_0, α_1: arbitrary mechanical angles within the angular range

$\phi_{meas}(\alpha_0, T_{RT})$: programmed angle at α_0, T_{RT} = 25 °C and zero hour upon production

$\phi_{meas}(\alpha_1, T_{amb})$: angle measured by the sensor at α_1 and any temperature within T_{amb}

This error comprises non-linearity and temperature drift related to the room temperature.

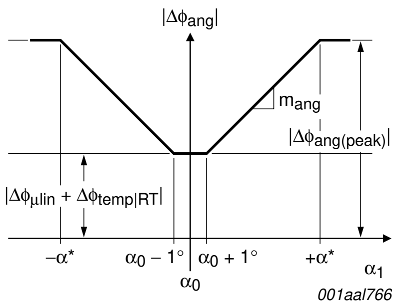


Fig 11. Envelope curve for the magnitude of angular error

Figure 11 shows the envelope curve for the magnitude of angular error $|\Delta\phi_{ang}|$ versus α_1 for all angles α_0 and all temperatures T_{amb} within the ambient temperature range. $|\Delta\phi_{ang}|$ has its minimum, if α_1 is in the range of $\pm 1°$ around α_0. Here only the microlinearity error $\Delta\phi_{\mu lin}$ and the temperature drift related to the room temperature $|\Delta\phi_{temp|RT}|$ occurs. If α_1 deviates from α_0 by more than 1° in either direction, $|\Delta\phi_{ang}|$ can increase with a gradient defined by slope m_{ang}.

Angular error can be expressed by Equation 5 to Equation 8:

for $|\alpha_1 - \alpha_0| \leq 1°$

$$|\Delta\phi_{ang}| = |\Delta\phi_{\mu lin} + \Delta\phi_{temp|RT}| \tag{5}$$

for $1° < |\alpha_1 - \alpha_0| < \alpha^*$

$$|\Delta\phi_{ang}| = |\Delta\phi_{\mu lin} + \Delta\phi_{temp|RT}| + m_{ang} \times (|\alpha_1 - \alpha_0| - 1°) \tag{6}$$

for $|\alpha_1 - \alpha_0| \geq \alpha^*$

$$|\Delta\phi_{ang}| = \sqrt{(\Delta\phi_{lin})^2 + (\Delta\phi_{temp|RT})^2} \tag{7}$$

with:

$$\alpha^* = \frac{|\Delta\phi_{\mathrm{ang(peak)}}| - |\Delta\phi_{\mu lin} + \Delta\phi_{temp|RT}|}{m_{ang}} + \alpha_0 + 1° \tag{8}$$

13. Programming

13.1 General description

The KMA210 provides an OWI to enable programming of the device which uses pin OUT/DATA bidirectionally.

In general the device runs in analog output mode, the normal operation mode. This mode is configured by the embedded programming data and is started after a power-on reset once time t_{on} has elapsed. In this mode, the magnetic field angle is converted into the corresponding output voltage.

Command mode has to be entered to enable programming. In this mode, the customer can adjust all required parameters (for example zero angle and angular range) to meet the application requirements. After enabling the internal charge pump and waiting for t_{cp} the data is stored in the non-volatile memory. After changing the contents of the memory, the checksum must be recalculated and written (see Section 13.4).

In order to enter the command mode, a specific command sequence must be sent after a power-on reset and during the time slot $t_{cmd(ent)}$. The external source used to send the command sequence must overdrive the output buffer of the KMA210. In doing so it provides current I_{od}.

During communication, the KMA210 is always the slave and the external programming hardware is the master. Figure 12 illustrates the structure of the OWI data format.

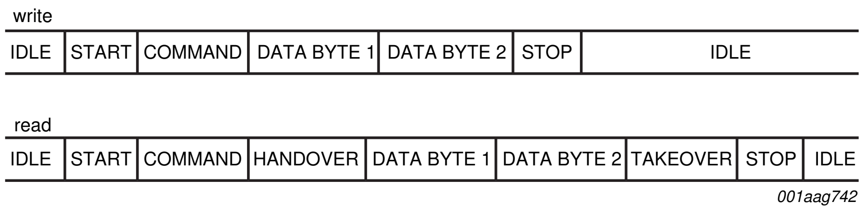


Fig 12. OWI data format

The master provides the start condition, which is a rising edge after a LOW level. Then a command byte which can be either a read or a write command is sent. Depending on the command, the master or the slave has to send the data immediately after the command sequence. In the case of a read command, an additional handover or takeover bit is inserted before and after the data bytes. Each communication must be closed with a stop condition driven by the master. If the slave does not receive a rising edge for a time longer than t_{to}, a time-out condition occurs. The bus is reset to the idle state and waits for a start condition and a new command. This can be used to synchronize the device regardless of the previous state.

All communication is based on this structure (see Figure 12), even for entering the command mode. In this case a special write command is required, followed by the command sequence (two data bytes). The customer can access the non-volatile memory, CTRL1, TESTCTRL0 and SIGNATURE registers (described in Section 13.5). Only a power-on reset will leave the command mode. A more detailed description of the programming is given in the next sections.

13.2 Timing characteristics

As described in the previous section, a start and stop condition is necessary for communication. The LOW-level duration before the rising edge of the start condition is defined as t_{start}. The HIGH-level duration after the rising edge of the stop condition is defined as t_{stop}. These parameters, together with all other timing characteristics are shown in Table 14.

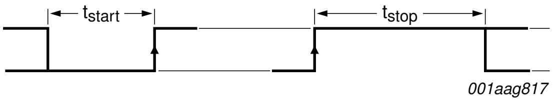


Fig 13. OWI start and stop condition

Figure 14 shows the coding of a single bit with a HIGH level of V_{IH} and a LOW level of V_{IL}. Here the pulse width t_{w1} or t_{w0} represents a logic 1 or a logic 0 of a full bit period T_{bit}, respectively.

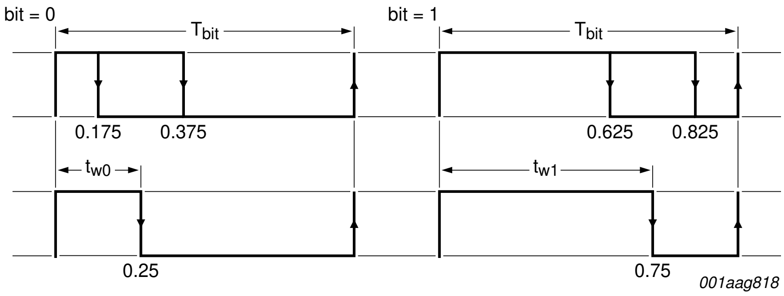


Fig 14. OWI timing

13.3 Sending and receiving data

The master has to control the communication during sending or receiving data. The command byte defines the region, address and type of command requested by the master. In case of a read command, an additional handover or takeover bit must be inserted before and after the two data bytes (see Figure 12). However the OWI is a serial data transmission, whereas the Most Significant Byte (MSB) must be sent at first.

Table 16. Format of a command byte

7	6	5	4	3	2	1	0
CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

Table 17. Command byte bit description

Bit	Symbol	Description
7 to 5	CMD[7:5]	region bits
		000 = 16-bit non-volatile memory
		001 to 011 = reserved
		100 = 16-bit register
		101 to 111 = reserved
4 to 1	CMD[4:1]	address bits
0	CMD0	read/write
		0 = write
		1 = read

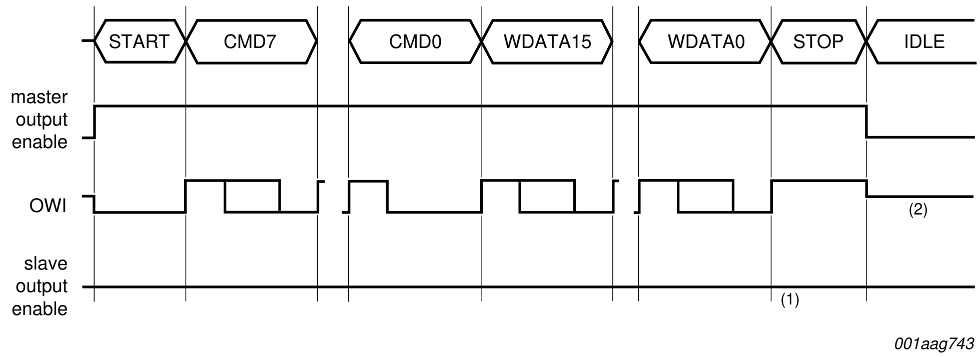
A more detailed description of all customer accessible registers is given in Section 13.5. Both default value and the complete command including the address and write or read request are also listed.

13.3.1 Write access

To write data to the non-volatile memory, the internal charge pump must be enabled by setting bits CP_CLOCK_EN and WRITE_EN and waiting for t_{cp}. The following procedure must be performed:

1. Start condition: The master drives a rising edge after a LOW level
2. Command: The master sends a write command (CMD0 = 0)
3. Data: The master sends two data bytes
4. Stop condition: The master drives a rising edge after a LOW level

Figure 15 shows the write access of the digital interface. The signal OWI represents the data on the bus from the master or slave. The signals: master output enable and slave output enable indicate when the master or the slave output is enabled or disabled, respectively.



(1) Missing rising edges generate a time-out condition and the written data is ignored.

(2) If the master does not drive the bus, the bus is defined by the bus-pull.

Fig 15. OWI write access

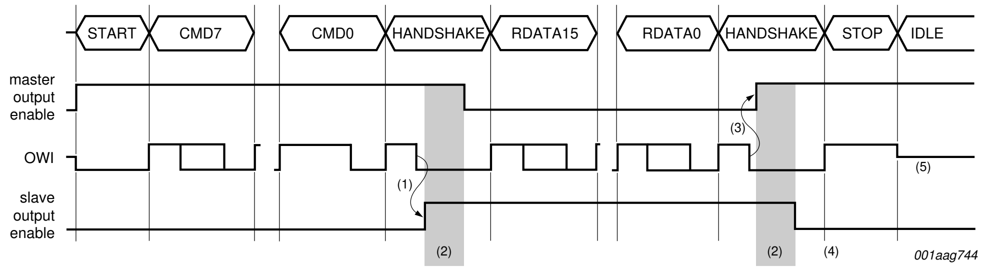
Note: As already mentioned in Section 13.1, the command mode has to be entered using the write procedure. If command mode is not entered, communication is not possible and the sensor operates in normal operation mode. After changing an address, the time t_{prog} must elapse before changing another address. Finally the checksum must be recalculated and written, because the contents of the non-volatile memory have been changed (see Section 13.4).

13.3.2 Read access

To read data from the sensor, the following procedure must be performed:

1. Start condition: The master drives a rising edge after a LOW level
2. Command: The master sends a read command (CMD0 = 1)
3. Handover: The master sends a handover bit, that is a logic 0 and disables the output after a three-quarter bit period
4. Takeover: The slave drives a LOW level after the falling edge for $t_{tko(slv)}$
5. Data: The slave sends two data bytes
6. Handover: The slave sends a handover bit, that is a logic 0 and disables the output after a three-quarter bit period
7. Takeover: The master drives a LOW level after the falling edge for $t_{tko(mas)}$
8. Stop condition: The master drives a rising edge after a LOW level

Figure 16 shows the read access of the digital interface. The signal OWI represents the data on the bus from the master or slave. The signals: master output enable and slave output enable indicate when the master or the slave output is enabled or disabled, respectively.



(1) Duration of LOW level for slave takeover $t_{tko(slv)}$.

(2) There is an overlap in the output enables of master and slave, because both drive a LOW level. However this ensures the independency from having a pull-up or pull-down on the bus. In addition it improves the EMC robustness, because all levels are actively driven.

(3) Duration of LOW level for master takeover $t_{tko(mas)}$.

(4) If the master does not take over and a pull-up exists, the stop condition is generated by the pull-up. Otherwise a time-out is generated if there is a pull-down and the slave waits for a rising edge as start condition.

(5) If the master does not drive the bus, the bus is defined by the bus-pull.

Fig 16. OWI read access

13.3.3 Entering the command mode

After a power-on reset, the sensor provides a time slot $t_{cmd(ent)}$ for entering the command mode. A specific command sequence has to be sent (see Figure 17). If command mode is not entered, the sensor starts in the normal operation mode. However the signature can be written by the master if the sensor switches to diagnostic mode.

During the command mode sequence, the analog output is enabled. The external programming hardware has to overdrive the output with current I_{od}. If command mode is activated, the analog output is disabled and pin OUT/DATA operates as a digital interface.

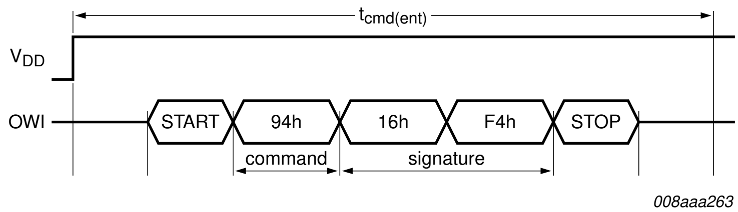


Fig 17. OWI command mode procedure

13.4 Cyclic redundancy check

As already mentioned in Section 7, there is an 8-bit checksum for the non-volatile memory data. To calculate this value, the CRC needs to be generated with the MSB of the memory data word at first over all corresponding addresses in increasing order.

All addresses from 8h to Fh must be read out for calculating the checksum. The Least Significant Byte (LSB) of address Fh which contains the previous checksum must be overwritten with 0h before the calculation can be started.

Finally, the internal charge pump has to be enabled for programming by setting bits CP_CLOCK_EN and WRITE_EN (see Section 13.5.1) and waiting for t_{cp}.

The generator polynomial for the calculation of the checksum is:

$$G(x) = x^8 + x^2 + x + 1 \tag{9}$$

With a start value of FFh and the data bits are XOR at the x^8 point.

13.4.1 Software example in C

```c
#include <stdio.h.>

// calc_crc accepts unsigned 16-bit data in data
int calc_crc(int crc, unsigned int data)
{
      const int gpoly = 0x107; // generator polynomial
      int i;                  //index variable
      for (i = 15; i >= 0; i--)
      {
            crc <<= 1;             //shift left
            crc |= (int) ((data & (1u<<i))>>i);
            // XOR of with generator polynomial when MSB(9) = HIGH
            if (crc & 0x100) crc ^= gpoly;
      }
      return crc;
}
int main(void)
{
      int crc, crc_res, i;
      // 8 LSB are CRC field filled with 0
      unsigned int data_seq[] = {0x0000, 0xFFC1, 0x0400, 0x0100,
                                 0x1300, 0x0000, 0x0000, 0x0000};
      // calculate checksum over all data
      crc = 0xFF;                // start value of crc register
      printf(“Address\tValue\n”);
      for (i = 0; i <= 7; i++)
            {
            printf(“0x%1X\t0x%04X\n”, i, data_seq[i]);
            crc = calc_crc(crc, data_seq[i]);
            }
      crc_res = crc;             // crc_res = 0xA9
      printf(“\nChecksum\n0x%02X\n”, crc_res);
      // check procedure for above data sequence
      crc = 0xFF;
      for (i = 0; i <= 6; i++)
            crc = calc_crc(crc, data_seq[i]);
      // last word gets crc inserted
      crc = calc_crc(crc, data_seq[i] | crc_res);
      printf(“\nCheck procedure for data sequence: must be 0x00 is 0x%02X.\n”,crc);
      return 1;
}
```

The checksum of this data sequence is A9h.

13.5 Registers

13.5.1 Command registers

To enter the command mode, the signature given in Table 18 must be written into the specific register using the OWI. This must be done as described in Section 13.3.3, with a write command, followed by the signature, but after a power-on reset and not later than $t_{cmd(ent)}$.

Table 18. Command registers

Command write/read	Register	Bit	Access	Field	Description
82h/83h	CTRL1	15	R	IN_DIAG_MODE	shows if there is a diagnostic condition present; this bit is not affected by the setting of register field FORCE_DIAG_OFF
		14	W	FORCE_DIAG_OFF	force diagnostic mode off; default: 0b
		13	-	-	reserved
		12	R	LOW_VOLTAGE_DET	low voltage condition detected
		11	R/W	CP_CLOCK_EN	charge pump clock enabled (must be set after setting write enable signal for writing to non-volatile memory); default: 0b
		10 and 9	-	-	reserved
		8	R	ERR_CORRECT	single-bit error of non-volatile memory has been detected and corrected; updated every memory readout; remains set until the diagnostic condition disappears and a power-on reset is done
		7	R	UNCORR_ERR	double-bit error of non-volatile memory has been detected; updated every memory readout; remains set until the diagnostic condition disappears and a power-on reset is done
		6	R	MAGNET_LOSS_DET	magnet-loss detected; bit remains set until the diagnostic condition disappears and a power-on reset is done; magnet-loss detection must be enabled for entering diagnostic mode
		5	R	BROKEN_BOND_DET	broken bond wire detected; bit remains set until the diagnostic condition disappears and a power-on reset is done
		4	R	CRC_BAD	checksum error detected; updated every start-up
		3 to 0	-	-	reserved
94h/-	SIGNATURE	15 to 0	W	SIGNATURE	write signature 16F4h within $t_{cmd(ent)}$ to enter command mode; see Section 13.3.3 for more details
96h/97h	TESTCTRL0	15 to 12	-	-	reserved
		11	W	WRITE_EN	write enable signal; must be set before writing to non-volatile memory; default: 0b
		10 to 0	-	-	reserved

13.5.2 Non-volatile memory registers

The device includes several internal registers which are used for customization and identification.

The initial signature allows read access to all areas but only write access to customer registers. Write accesses to reserved areas are ignored. Since these registers are implemented as non-volatile memory cells, writing to the registers needs a specific time t_{prog} after each write access to complete.

As there is no check for the programming time, the user must make sure no other accesses to the non-volatile memory are made during the programming cycle. The non-volatile memory must not be addressed during the time t_{prog}.

Note: Before data can be stored in the non-volatile memory, the internal charge pump has to be switched on for the programming duration by setting register CTRL1, bit 11 CP_CLOCK_EN and register TESTCTRL0, bit 11 WRITE_EN. Register addresses 8h to Fh have to be read out and consulted to calculate the checksum.

Table 19. Non-volatile memory registers

Address	Command write/read	Register	Bit	Description	Default MSB/LSB
0h	-/01h	reserved	-	addresses are reserved for calibration purposes	[1]
1h	-/03h				
2h	-/05h				
3h	-/07h				
4h	-/09h				
5h	-/0Bh				
6h	-/0Dh				
7h	-/0Fh				
8h	10h/11h	ZERO_ANGLE	15 to 0	mechanical zero degree position; see Table 20	00h/00h
9h	12h/13h	ANG_RNG_MULT_MSB	15 to 6	CLAMP_SW_ANGLE; when the measured angle is bigger than CLAMP_SW_ANGLE the output switches to CLAMP_LO for a positive slope; see Table 25	FFh/C1h
			5 to 0	ANG_RNG_MULT_MSB; most significant bits of the angular range multiplicator; see Table 23	
Ah	14h/15h	ANG_RNG_MULT_LSB	15 and 14	DIAGNOSTIC_LEVEL; diagnostic level behavior of the analog output; see Table 24 **00b** — active LOW (in lower diagnostic range) with driver strength of the analog output **01b** — active HIGH (in upper diagnostic range) with driver strength of the analog output **10b** — reserved **11b** — reserved	04h/00h
			13	SLOPE_DIR; slope of analog output **0b** — rising (not inverted) **1b** — falling (inverted)	
			12 to 0	ANG_RNG_MULT_LSB; least significant bits of the angular range multiplicator	

Table 19. Non-volatile memory registers *...continued*

Address	Command write/read	Register	Bit	Description	Default MSB/LSB
Bh	16h/17h	CLAMP_LO	15	**0b** — reserved	01h/00h
			14 and 13	undefined[2]	
			12 to 0	lower clamping level; see Table 21	
Ch	18h/19h	CLAMP_HI	15 to 13	undefined[2]	13h/00h
			12 to 0	upper clamping level; see Table 22	
Dh	1Ah/1Bh	ID_LO	15 to 0	lower 16 bits of identification code	00h/00h
Eh	1Ch/1Dh	ID_HI	15 to 0	upper 16 bits of identification code	00h/00h
Fh	1Eh/1Fh	CTRL_CUST	15	LOCK; irreversible write protection of non-volatile memory **1b** — enabled	00h/[1]
			14 to 8	MAGNET_LOSS; magnet-loss detection **00h** — disabled **49h** — enabled	
			7 to 0	CRC; checksum (see Section 13.4)	

[1] Variable and individual for each device.

[2] Undefined; must be written as zero for default.

Table 20. ZERO_ANGLE - mechanical zero degree position (address 8h) bit allocation
Data format: unsigned fixed point; resolution: 2^{-16}.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Mechanical angular range 0000h = 0° to FFFFh = 180° – 1 LSB.

Examples:

- Mechanical zero angle 0° = 0000h
- Mechanical zero angle 10° = 0E38h
- Mechanical zero angle 45° = 4000h

Table 21. CLAMP_LO - lower clamping level (address Bh) bit allocation
Data format: unsigned integer (DAC values 256 to 4864); resolution: 2^0.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	U[1]	U[1]	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

[1] Undefined; must be written as zero for default and may return any value when read.

Values 0 to 255 are reserved. It is not permitted to use such values.

Examples:

- 100 %V_{DD} = 5120 (reserved)
- 10 %V_{DD} = 512
- 5 %V_{DD} = 256