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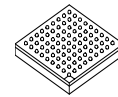
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## MSC8113



FC-PBGA-431  
20 mm × 20 mm

### Tri-Core Digital Signal Processor

- Three StarCore™ SC140 DSP extended cores, each with an SC140 DSP core, 224 Kbyte of internal SRAM M1 memory (1436 Kbyte total), 16 way 16 Kbyte instruction cache (ICache), four-entry write buffer, external cache support, programmable interrupt controller (PIC), local interrupt controller (LIC), and low-power Wait and Stop processing modes.
- 475 Kbyte M2 memory for critical data and temporary data buffering.
- 4 Kbyte boot ROM.
- M2-accessible multi-core MQBus connecting the M2 memory with all three cores, operating at the core frequency, with data bus access of up to 128-bit reads and up to 64-bit writes, central efficient round-robin arbiter for core access to the bus, and atomic operation control of M2 memory access by the cores and the local bus.
- Internal PLL configured are reset by configuration signal values.
- 60x-compatible system bus with 64 or 32 bit data and 32-bit address bus, support for multi-master designs, four-beat burst transfers (eight-beat in 32-bit data mode), port size of 64/32/16/8 bits controlled by the internal memory controller, access to external memory or peripherals, access by an external host to internal resources, slave support with direct access to internal resources including M1 and M2 memories, and on-device arbitration for up to four master devices.
- Direct slave interface (DSI) using a 32/64-bit slave host interface with 21–25 bit addressing and 32/64-bit data transfers, direct access by an external host to internal and external resources, synchronous or asynchronous accesses with burst capability in synchronous mode, dual or single strobe mode, write and read buffers to improve host bandwidth, byte enable signals for 1/2/4/8-byte write granularity, sliding window mode for access using a reduced number of address pins, chip ID decoding to allow one  $\overline{CS}$  signal to control multiple DSPs, broadcast mode to write to multiple DSPs, and big-endian/little-endian/munged support.
- Three mode signal multiplexing: 64-bit DSI and 32-bit system bus, 32-bit DSI and 64-bit system bus, or 32-bit DSI and 32-bit system bus, and Ethernet port (MII/RMII).
- Flexible memory controller with three UPMs, a GPCM, a page-mode SDRAM machine, glueless interface to a variety of memories and devices, byte enables for 64- or 32-bit bus widths, 8 memory banks for external memories, and 2 memory banks for IPBus peripherals and internal memories.
- Multi-channel DMA controller with 16 time-multiplexed single channels, up to four external peripherals,  $\overline{DONE}$  or  $\overline{DRACK}$  protocol for two external peripherals, service for up to 16 internal requests from up to 8 internal FIFOs per channel, FIFO generated watermarks and hungry requests, priority-based time-multiplexing between channels using 16 internal priority levels or round-robin time-multiplexing between channels, flexible channel configuration with connection to local bus or system bus, and flyby transfer support that bypasses the FIFO.
- Up to four independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/ $\mu$ -law conversion, up to 128 Mbps data rate for all channels, with glueless interface to E1 or T1 framers, and can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.
- Ethernet controller with support for 10/100 Mbps MII/RMII/SMII including full- and half-duplex operation, full-duplex flow controls, out-of-sequence transmit queues, programmable maximum frame length including jumbo frames and VLAN tags and priority, retransmission after collision, CRC generation and verification of inbound/outbound packets, address recognition (including exact match, broadcast address, individual hash check, group hash check, and promiscuous mode), pattern matching, insertion with expansion or replacement for transmit frames, VLAN tag insertion, RMON statistics, local bus master DMA for descriptor fetching and buffer access, and optional multiplexing with GPIO (MII/RMII/SMII) or DSI/system bus signals lines (MII/RMII).
- UART with full-duplex operation up to 6.25 Mbps.
- Up to 32 general-purpose input/output (GPIO) ports.
- I<sup>2</sup>C interface that allows booting from EEPROM devices.
- Two timer modules, each with sixteen configurable 16-bit timers.
- Eight programmable hardware semaphores.
- Global interrupt controller (GIC) with interrupt consolidation and routing to  $\overline{INT\_OUT}$ ,  $\overline{NMI\_OUT}$ , and the cores; twenty-four virtual maskable interrupts (8 per core) and three virtual  $\overline{NMI}$  (one per core) that can be generated by a simple write access.
- Optional booting external memory, external host, UART, TDM, or I<sup>2</sup>C.

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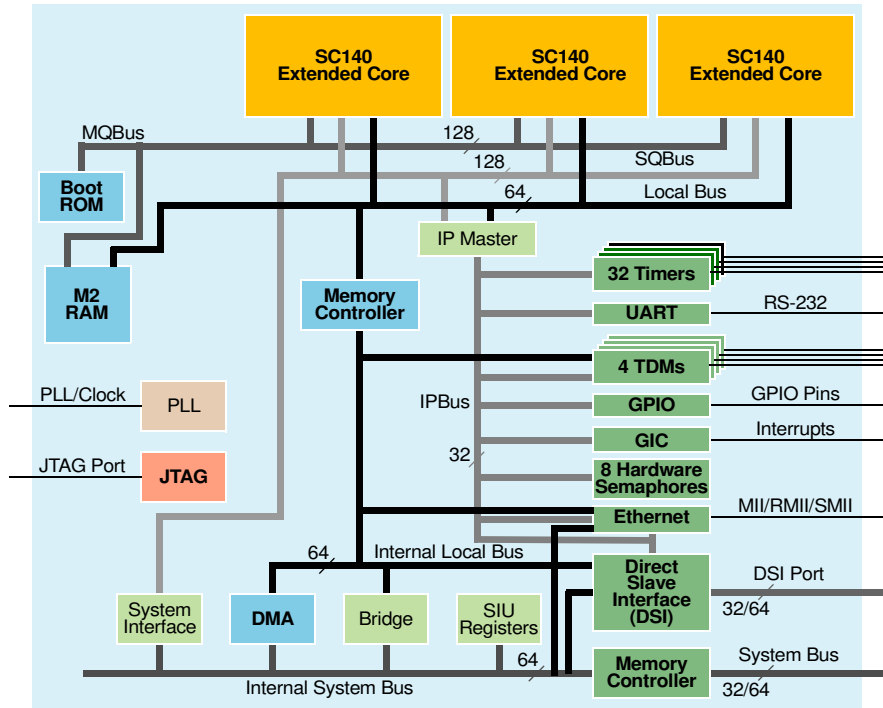
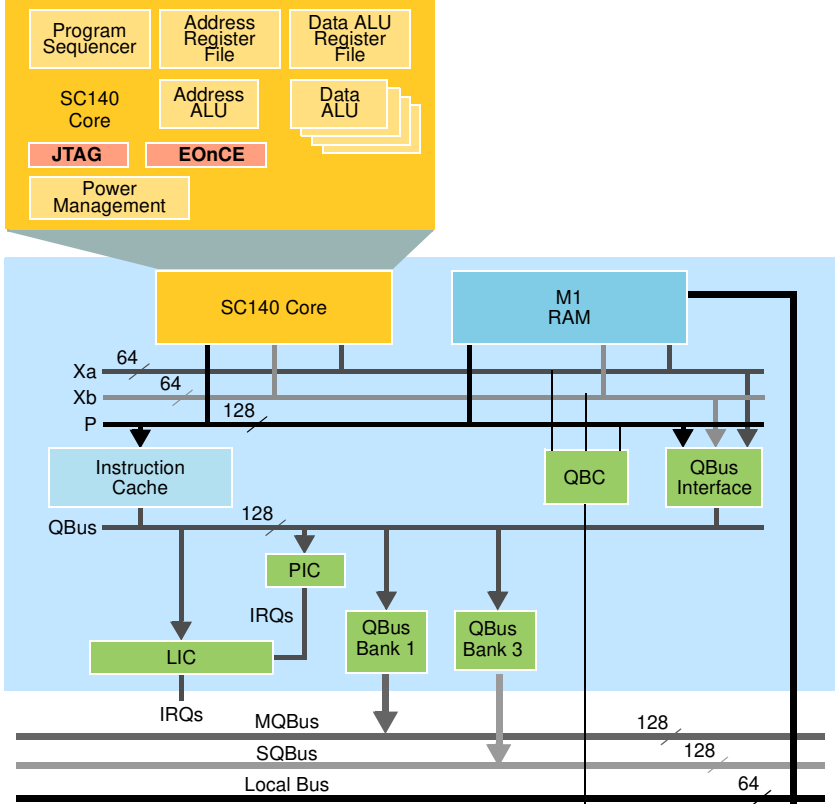


Figure 1. MSC8113 Block Diagram



Notes: 1. The arrows show the data transfer direction.  
 2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. StarCore® SC140 DSP Extended Core Block Diagram

# 1 Pin Assignments

This section includes diagrams of the MSC8113 package ball grid array layouts and pinout allocation tables.

## 1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Top View

|    | 2               | 3                | 4                | 5                | 6                 | 7                   | 8                   | 9                | 10                  | 11              | 12               | 13               | 14               | 15                 | 16                 | 17               | 18               | 19               | 20               | 21               | 22               |     |
|----|-----------------|------------------|------------------|------------------|-------------------|---------------------|---------------------|------------------|---------------------|-----------------|------------------|------------------|------------------|--------------------|--------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----|
| B  |                 | V <sub>DD</sub>  | GND              | GND              | NMI OUT           | GND                 | V <sub>DD</sub>     | GND              | V <sub>DD</sub>     | GND             | V <sub>DD</sub>  | GND              | V <sub>DD</sub>  | GND                | V <sub>DD</sub>    | GND              | V <sub>DD</sub>  | GPI00            | V <sub>DD</sub>  | V <sub>DD</sub>  | GND              |     |
| C  | GND             | V <sub>DD</sub>  | TDO              | S RESET          | GPI028            | HCID1               | GND                 | V <sub>DD</sub>  | GND                 | V <sub>DD</sub> | GND              | V <sub>DD</sub>  | GND              | GND                | GPI030             | GPI02            | GPI01            | GPI07            | GPI03            | GPI05            | GPI06            |     |
| D  | TDI             | EE0              | EE1              | GND              | V <sub>DDH</sub>  | HCID2               | HCID3               | GND              | V <sub>DD</sub>     | GND             | V <sub>DD</sub>  | GND              | V <sub>DD</sub>  | V <sub>DD</sub>    | GPI031             | GPI029           | V <sub>DDH</sub> | GPI04            | V <sub>DDH</sub> | GND              | GPI08            |     |
| E  | TCK             | TRST             | TMS              | HRESET           | GPI027            | HCID0               | GND                 | V <sub>DD</sub>  | GND                 | V <sub>DD</sub> | GND              | V <sub>DD</sub>  | GND              | GND                | V <sub>DD</sub>    | GND              | GND              | GPI09            | GPI013           | GPI010           | GPI012           |     |
| F  | PO RESET        | RST CONF         | NMI              | HA29             | HA22              | GND                 | V <sub>DD</sub>     | V <sub>DD</sub>  | V <sub>DD</sub>     | GND             | V <sub>DD</sub>  | GND              | V <sub>DD</sub>  | ETHRX CLK          | ETHTX CLK          | GPI020           | GPI018           | GPI016           | GPI011           | GPI014           | GPI019           |     |
| G  | HA24            | HA27             | HA25             | HA23             | HA17              | PWE0                | V <sub>DD</sub>     | V <sub>DD</sub>  | BADDR <sub>31</sub> | BM0             | ABB              | V <sub>DD</sub>  | INT OUT          | ETHCR S            | V <sub>DD</sub>    | CS1              | BCTL0            | GPI015           | GND              | GPI017           | GPI022           |     |
| H  | HA20            | HA28             | V <sub>DD</sub>  | HA19             | TEST              | PSD CAS             | PGTA                | V <sub>DD</sub>  | BM1                 | ARTRY           | AACK             | DBB              | HTA              | V <sub>DD</sub>    | TT4                | CS4              | GPI024           | GPI021           | V <sub>DD</sub>  | V <sub>DDH</sub> | A31              |     |
| J  | HA18            | HA26             | V <sub>DD</sub>  | HA13             | GND               | PSDA MUX            | BADDR <sub>27</sub> | V <sub>DD</sub>  | CLKIN               | BM2             | DBG              | V <sub>DD</sub>  | GND              | V <sub>DD</sub>    | TT3                | PSDA10           | BCTL1            | GPI023           | GND              | GPI025           | A30              |     |
| K  | HA15            | HA21             | HA16             | PWE3             | PWE1              | POE                 | BADDR <sub>30</sub> | Res.             | GND                 | GND             | GND              | GND              | CLKOUT           | V <sub>DD</sub>    | TT2                | ALE              | CS2              | GND              | A26              | A29              | A28              |     |
| L  | HA12            | HA14             | HA11             | V <sub>DDH</sub> | V <sub>DDH</sub>  | BADDR <sub>28</sub> | BADDR <sub>29</sub> | GND              | GND                 | MSC8113         |                  |                  |                  | GND                | V <sub>DDH</sub>   | GND              | GND              | CS3              | V <sub>DDH</sub> | A27              | A25              | A22 |
| M  | HD28            | HD31             | V <sub>DDH</sub> | GND              | GND               | GND                 | V <sub>DD</sub>     | V <sub>DDH</sub> | GND                 |                 |                  |                  |                  | GND                | V <sub>DDH</sub>   | GND              | GND              | V <sub>DDH</sub> | HBRST            | V <sub>DDH</sub> | V <sub>DDH</sub> | GND |
| N  | HD26            | HD30             | HD29             | HD24             | PWE2              | V <sub>DDH</sub>    | HWBS <sub>0</sub>   | HBCS             | GND                 | MSC8113         |                  |                  |                  | GND                | HRDS               | BG               | HCS              | CS0              | PSDWE            | GPI026           | A23              | A20 |
| P  | HD20            | HD27             | HD25             | HD23             | HWBS <sub>3</sub> | HWBS <sub>2</sub>   | HWBS <sub>1</sub>   | HCLKIN           | GND                 |                 |                  |                  |                  | GND <sub>SYN</sub> | V <sub>CCSYN</sub> | GND              | GND              | TA               | BR               | TEA              | PSD VAL          | DP0 |
| R  | HD18            | V <sub>DDH</sub> | GND              | HD22             | HWBS <sub>6</sub> | HWBS <sub>4</sub>   | TSZ1                | TSZ3             | GBL                 | V <sub>DD</sub> | V <sub>DD</sub>  | V <sub>DD</sub>  | TT0              | DP7                | DP6                | DP3              | TS               | DP2              | A17              | A18              | A16              |     |
| T  | HD17            | HD21             | HD1              | HD0              | HWBS <sub>7</sub> | HWBS <sub>5</sub>   | TSZ0                | TSZ2             | TBST                | V <sub>DD</sub> | D16              | TT1              | D21              | D23                | DP5                | DP4              | DP1              | D30              | GND              | A15              | A14              |     |
| U  | HD16            | HD19             | HD2              | D2               | D3                | D6                  | D8                  | D9               | D11                 | D14             | D15              | D17              | D19              | D22                | D25                | D26              | D28              | D31              | V <sub>DDH</sub> | A12              | A13              |     |
| V  | HD3             | V <sub>DDH</sub> | GND              | D0               | D1                | D4                  | D5                  | D7               | D10                 | D12             | D13              | D18              | D20              | GND                | D24                | D27              | D29              | A8               | A9               | A10              | A11              |     |
| W  | HD6             | HD5              | HD4              | GND              | GND               | V <sub>DDH</sub>    | V <sub>DDH</sub>    | GND              | HDST1               | HDST0           | V <sub>DDH</sub> | GND              | HD40             | V <sub>DDH</sub>   | HD33               | V <sub>DDH</sub> | HD32             | GND              | GND              | A7               | A6               |     |
| Y  | HD7             | HD15             | V <sub>DDH</sub> | HD9              | V <sub>DD</sub>   | HD60                | HD58                | GND              | V <sub>DDH</sub>    | HD51            | GND              | V <sub>DDH</sub> | HD43             | GND                | V <sub>DDH</sub>   | GND              | HD37             | HD34             | V <sub>DDH</sub> | A4               | A5               |     |
| AA | V <sub>DD</sub> | HD14             | HD12             | HD10             | HD63              | HD59                | GND                 | V <sub>DDH</sub> | HD54                | HD52            | V <sub>DDH</sub> | GND              | V <sub>DDH</sub> | HD46               | GND                | HD42             | HD38             | HD35             | A0               | A2               | A3               |     |
| AB | GND             | HD13             | HD11             | HD8              | HD62              | HD61                | HD57                | HD56             | HD55                | HD53            | HD50             | HD49             | HD48             | HD47               | HD45               | HD44             | HD41             | HD39             | HD36             | A1               | V <sub>DD</sub>  |     |

Figure 3. MSC8113 Package, Top View

Bottom View

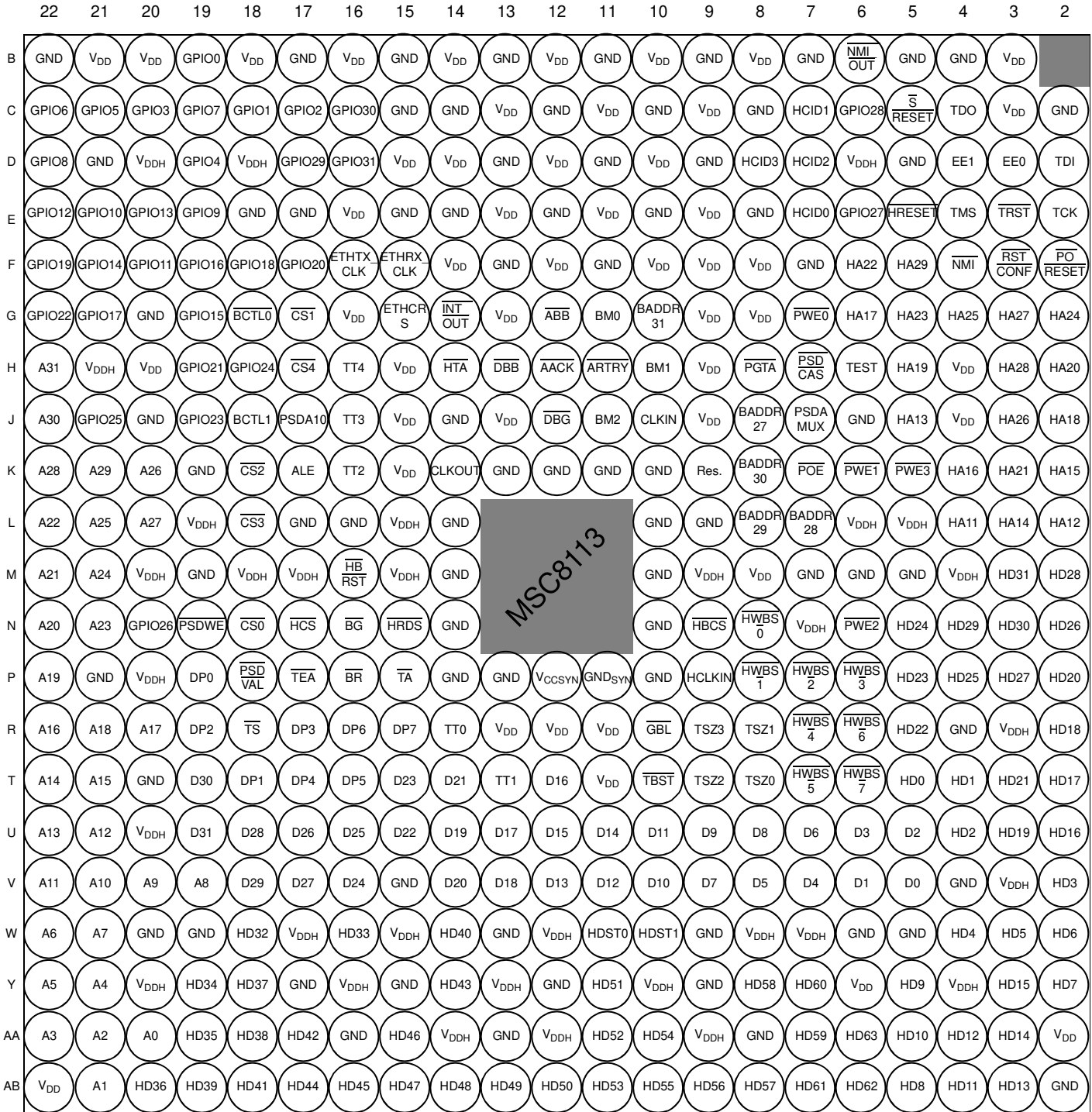


Figure 4. MSC8113 Package, Bottom View

## 1.2 Signal List By Ball Location

Table 1 presents signal list sorted by ball number. -

**Table 1. MSC8113 Signal Listing by Ball Designator**

| Des. | Signal Name                                       | Des. | Signal Name  |
|------|---|------|--|
| B3   | V <sub>DD</sub>                                   | C18  | GPIO1/TIMER0/CHIP_ID1/ $\overline{\text{IRQ5}}$ /ETHTXD1 |
| B4   | GND   | C19  | GPIO7/TDM3RCLK/ $\overline{\text{IRQ5}}$ /ETHTXD3        |
| B5   | GND   | C20  | GPIO3/TDM3TSYN/ $\overline{\text{IRQ1}}$ /ETHTXD2        |
| B6   | $\overline{\text{NMI\_OUT}}$                      | C21  | GPIO5/TDM3TDAT/ $\overline{\text{IRQ3}}$ /ETHRXD3        |
| B7   | GND   | C22  | GPIO6/TDM3RSYN/ $\overline{\text{IRQ4}}$ /ETHRXD2        |
| B8   | V <sub>DD</sub>                                   | D2   | TDI  |
| B9   | GND   | D3   | EE0  |
| B10  | V <sub>DD</sub>                                   | D4   | EE1  |
| B11  | GND   | D5   | GND  |
| B12  | V <sub>DD</sub>                                   | D6   | V <sub>DDH</sub>   |
| B13  | GND   | D7   | HCID2  |
| B14  | V <sub>DD</sub>                                   | D8   | HCID3/HA8  |
| B15  | GND   | D9   | GND  |
| B16  | V <sub>DD</sub>                                   | D10  | V <sub>DD</sub>  |
| B17  | GND   | D11  | GND  |
| B18  | V <sub>DD</sub>                                   | D12  | V <sub>DD</sub>  |
| B19  | GPIO0/CHIP_ID0/ $\overline{\text{IRQ4}}$ /ETHTXD0 | D13  | GND  |
| B20  | V <sub>DD</sub>                                   | D14  | V <sub>DD</sub>  |
| B21  | V <sub>DD</sub>                                   | D15  | V <sub>DD</sub>  |
| B22  | GND   | D16  | GPIO31/TIMER3/SCL  |
| C2   | GND   | D17  | GPIO29/CHIP_ID3/ETHTX_EN                                 |
| C3   | V <sub>DD</sub>                                   | D18  | V <sub>DDH</sub>   |
| C4   | TDO   | D19  | GPIO4/TDM3TCLK/ $\overline{\text{IRQ2}}$ /ETHTX_ER       |
| C5   | $\overline{\text{SRESET}}$                        | D20  | V <sub>DDH</sub>   |
| C6   | GPIO28/UTXD/DREQ2                                 | D21  | GND  |
| C7   | HCID1   | D22  | GPIO8/TDM3RDAT/ $\overline{\text{IRQ6}}$ /ETHCOL         |
| C8   | GND   | E2   | TCK  |
| C9   | V <sub>DD</sub>                                   | E3   | $\overline{\text{TRST}}$                                 |
| C10  | GND   | E4   | TMS  |
| C11  | V <sub>DD</sub>                                   | E5   | $\overline{\text{HRESET}}$                               |
| C12  | GND   | E6   | GPIO27/URXD/DREQ1  |
| C13  | V <sub>DD</sub>                                   | E7   | HCID0  |
| C14  | GND   | E8   | GND  |
| C15  | GND   | E9   | V <sub>DD</sub>  |
| C16  | GPIO30/TIMER2/TMCLK/SDA                           | E10  | GND  |
| C17  | GPIO2/TIMER1/CHIP_ID2/ $\overline{\text{IRQ6}}$   | E11  | V <sub>DD</sub>  |



**Table 1. MSC8113 Signal Listing by Ball Designator (continued)**

| Des. | Signal Name                                | Des. | Signal Name                  |
|------|--|------|------------------------------|
| E12  | GND  | G6   | HA17                         |
| E13  | V <sub>DD</sub>                            | G7   | PWE0/PSDDQM0/PBS0            |
| E14  | GND  | G8   | V <sub>DD</sub>              |
| E15  | GND  | G9   | V <sub>DD</sub>              |
| E16  | V <sub>DD</sub>                            | G10  | IRQ3/BADDR31                 |
| E17  | GND  | G11  | BM0/TC0/BNKSEL0              |
| E18  | GND  | G12  | ABB/IRQ4                     |
| E19  | GPIO9/TDM2TSYN/IRQ7/ETHMDIO                | G13  | V <sub>DD</sub>              |
| E20  | GPIO13/TDM2RCLK/IRQ11/ETHMDC               | G14  | IRQ7/INT_OUT                 |
| E21  | GPIO10/TDM2TCLK/IRQ8/ETHRX_DV/ETHCRS_DV/NC | G15  | ETHCRS/ETHRXD                |
| E22  | GPIO12/TDM2RSYN/IRQ10/ETHRXD1/ETHSYNC      | G16  | V <sub>DD</sub>              |
| F2   | PORESET                                    | G17  | CS1                          |
| F3   | RSTCONF                                    | G18  | BCTL0                        |
| F4   | NMI  | G19  | GPIO15/TDM1TSYN/DREQ1        |
| F5   | HA29                                       | G20  | GND                          |
| F6   | HA22                                       | G21  | GPIO17/TDM1TDAT/DACK1        |
| F7   | GND  | G22  | GPIO22/TDM0TCLK/DONE2/DRACK2 |
| F8   | V <sub>DD</sub>                            | H2   | HA20                         |
| F9   | V <sub>DD</sub>                            | H3   | HA28                         |
| F10  | V <sub>DD</sub>                            | H4   | V <sub>DD</sub>              |
| F11  | GND  | H5   | HA19                         |
| F12  | V <sub>DD</sub>                            | H6   | TEST                         |
| F13  | GND  | H7   | PSDCAS/PGPL3                 |
| F14  | V <sub>DD</sub>                            | H8   | PGTA/PUPMWAIT/PGPL4/PPBS     |
| F15  | ETHRX_CLK/ETHSYNC_IN                       | H9   | V <sub>DD</sub>              |
| F16  | ETHTX_CLK/ETHREF_CLK/ETHCLOCK              | H10  | BM1/TC1/BNKSEL1              |
| F17  | GPIO20/TDM1RDAT                            | H11  | ARTRY                        |
| F18  | GPIO18/TDM1RSYN/DREQ2                      | H12  | AACK                         |
| F19  | GPIO16/TDM1TCLK/DONE1/DRACK1               | H13  | DBB/IRQ5                     |
| F20  | GPIO11/TDM2TDAT/IRQ9/ETHRX_ER/ETHTXD       | H14  | HTA                          |
| F21  | GPIO14/TDM2RDAT/IRQ12/ETHRXD0/NC           | H15  | V <sub>DD</sub>              |
| F22  | GPIO19/TDM1RCLK/DACK2                      | H16  | TT4/CS7                      |
| G2   | HA24                                       | H17  | CS4                          |
| G3   | HA27                                       | H18  | GPIO24/TDM0RSYN/IRQ14        |
| G4   | HA25                                       | H19  | GPIO21/TDM0TSYN              |
| G5   | HA23                                       | H20  | V <sub>DD</sub>              |

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name   | Des. | Signal Name                       |
|------|---|------|-----------------------------------|
| H21  | V <sub>DDH</sub>  | K15  | V <sub>DD</sub>                   |
| H22  | A31   | K16  | TT2/ $\overline{\text{CS5}}$      |
| J2   | HA18  | K17  | ALE                               |
| J3   | HA26  | K18  | $\overline{\text{CS2}}$           |
| J4   | V <sub>DD</sub>   | K19  | GND                               |
| J5   | HA13  | K20  | A26                               |
| J6   | GND   | K21  | A29                               |
| J7   | PSDAMUX/PGPL5   | K22  | A28                               |
| J8   | BADDR27   | L2   | HA12                              |
| J9   | V <sub>DD</sub>   | L3   | HA14                              |
| J10  | CLKIN   | L4   | HA11                              |
| J11  | BM2/TC2/BNKSEL2   | L5   | V <sub>DDH</sub>                  |
| J12  | $\overline{\text{DBG}}$   | L6   | V <sub>DDH</sub>                  |
| J13  | V <sub>DD</sub>   | L7   | BADDR28                           |
| J14  | GND   | L8   | $\overline{\text{IRQ5}}$ /BADDR29 |
| J15  | V <sub>DD</sub>   | L9   | GND                               |
| J16  | TT3/ $\overline{\text{CS6}}$  | L10  | GND                               |
| J17  | PSDA10/PGPL0  | L14  | GND                               |
| J18  | $\overline{\text{BCTL1}}$ / $\overline{\text{CS5}}$                               | L15  | V <sub>DDH</sub>                  |
| J19  | GPIO23/TDM0TDAT/ $\overline{\text{IRQ13}}$  | L16  | GND                               |
| J20  | GND   | L17  | GND                               |
| J21  | GPIO25/TDM0RCLK/ $\overline{\text{IRQ15}}$  | L18  | $\overline{\text{CS3}}$           |
| J22  | A30   | L19  | V <sub>DDH</sub>                  |
| K2   | HA15  | L20  | A27                               |
| K3   | HA21  | L21  | A25                               |
| K4   | HA16  | L22  | A22                               |
| K5   | $\overline{\text{PWE3}}$ / $\overline{\text{PSDDQM3}}$ / $\overline{\text{PBS3}}$ | M2   | HD28                              |
| K6   | $\overline{\text{PWE1}}$ / $\overline{\text{PSDDQM1}}$ / $\overline{\text{PBS1}}$ | M3   | HD31                              |
| K7   | $\overline{\text{POE}}$ / $\overline{\text{PSDRAS}}$ /PGPL2                       | M4   | V <sub>DDH</sub>                  |
| K8   | $\overline{\text{IRQ2}}$ /BADDR30   | M5   | GND                               |
| K9   | Reserved  | M6   | GND                               |
| K10  | GND   | M7   | GND                               |
| K11  | GND   | M8   | V <sub>DD</sub>                   |
| K12  | GND   | M9   | V <sub>DDH</sub>                  |
| K13  | GND   | M10  | GND                               |
| K14  | CLKOUT  | M14  | GND                               |

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name                                 | Des. | Signal Name   |
|------|---|------|---|
| M15  | V <sub>DDH</sub>                            | P12  | V <sub>CCSYN</sub>  |
| M16  | $\overline{\text{HBRST}}$                   | P13  | GND   |
| M17  | V <sub>DDH</sub>                            | P14  | GND   |
| M18  | V <sub>DDH</sub>                            | P15  | $\overline{\text{TA}}$  |
| M19  | GND   | P16  | $\overline{\text{BR}}$  |
| M20  | V <sub>DDH</sub>                            | P17  | $\overline{\text{TEA}}$                                       |
| M21  | A24   | P18  | $\overline{\text{PSDVAL}}$                                    |
| M22  | A21   | P19  | DP0/DREQ1/ $\overline{\text{EXT\_BR2}}$                       |
| N2   | HD26  | P20  | V <sub>DDH</sub>  |
| N3   | HD30  | P21  | GND   |
| N4   | HD29  | P22  | A19   |
| N5   | HD24  | R2   | HD18  |
| N6   | $\overline{\text{PWE2/PSDDQM2/PBS2}}$       | R3   | V <sub>DDH</sub>  |
| N7   | V <sub>DDH</sub>                            | R4   | GND   |
| N8   | $\overline{\text{HWBS0/HDBS0/HWBE0/HDBE0}}$ | R5   | HD22  |
| N9   | $\overline{\text{HBCS}}$                    | R6   | $\overline{\text{HWBS6/HDBS6/HWBE6/HDBE6/PWE6/PSDDQM6/PBS6}}$ |
| N10  | GND   | R7   | $\overline{\text{HWBS4/HDBS4/HWBE4/HDBE4/PWE4/PSDDQM4/PBS4}}$ |
| N14  | GND   | R8   | TSZ1  |
| N15  | $\overline{\text{HRDS/HRW/HRDE}}$           | R9   | TSZ3  |
| N16  | $\overline{\text{BG}}$                      | R10  | $\overline{\text{IRQ1/GBL}}$                                  |
| N17  | $\overline{\text{HCS}}$                     | R11  | V <sub>DD</sub>   |
| N18  | $\overline{\text{CS0}}$                     | R12  | V <sub>DD</sub>   |
| N19  | $\overline{\text{PSDWE/PGPL1}}$             | R13  | V <sub>DD</sub>   |
| N20  | GPIO26/TDM0RDAT                             | R14  | TT0/HA7   |
| N21  | A23   | R15  | $\overline{\text{IRQ7/DP7/DREQ4}}$                            |
| N22  | A20   | R16  | $\overline{\text{IRQ6/DP6/DREQ3}}$                            |
| P2   | HD20  | R17  | $\overline{\text{IRQ3/DP3/DREQ2/EXT\_BR3}}$                   |
| P3   | HD27  | R18  | $\overline{\text{TS}}$  |
| P4   | HD25  | R19  | $\overline{\text{IRQ2/DP2/DACK2/EXT\_DBG2}}$                  |
| P5   | HD23  | R20  | A17   |
| P6   | $\overline{\text{HWBS3/HDBS3/HWBE3/HDBE3}}$ | R21  | A18   |
| P7   | $\overline{\text{HWBS2/HDBS2/HWBE2/HDBE2}}$ | R22  | A16   |
| P8   | $\overline{\text{HWBS1/HDBS1/HWBE1/HDBE1}}$ | T2   | HD17  |
| P9   | HCLKIN                                      | T3   | HD21  |
| P10  | GND   | T4   | HD1/DSISYNC   |
| P11  | GND <sub>SYN</sub>                          | T5   | HD0/SWTE  |

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name   | Des. | Signal Name      |
|------|---|------|------------------|
| T6   | $\overline{\text{HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7}}$ | U21  | A12              |
| T7   | $\overline{\text{HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5}}$ | U22  | A13              |
| T8   | TSZ0  | V2   | HD3/MODCK1       |
| T9   | TSZ2  | V3   | V <sub>DDH</sub> |
| T10  | $\overline{\text{TBST}}$                                      | V4   | GND              |
| T11  | V <sub>DD</sub>   | V5   | D0               |
| T12  | D16   | V6   | D1               |
| T13  | TT1   | V7   | D4               |
| T14  | D21   | V8   | D5               |
| T15  | D23   | V9   | D7               |
| T16  | $\overline{\text{IRQ5/DP5/DACK4/EXT_BG3}}$                    | V10  | D10              |
| T17  | $\overline{\text{IRQ4/DP4/DACK3/EXT_DBG3}}$                   | V11  | D12              |
| T18  | $\overline{\text{IRQ1/DP1/DACK1/EXT_BG2}}$                    | V12  | D13              |
| T19  | D30   | V13  | D18              |
| T20  | GND   | V14  | D20              |
| T21  | A15   | V15  | GND              |
| T22  | A14   | V16  | D24              |
| U2   | HD16  | V17  | D27              |
| U3   | HD19  | V18  | D29              |
| U4   | HD2/DSI64   | V19  | A8               |
| U5   | D2  | V20  | A9               |
| U6   | D3  | V21  | A10              |
| U7   | D6  | V22  | A11              |
| U8   | D8  | W2   | HD6              |
| U9   | D9  | W3   | HD5/CNFGS        |
| U10  | D11   | W4   | HD4/MODCK2       |
| U11  | D14   | W5   | GND              |
| U12  | D15   | W6   | GND              |
| U13  | D17   | W7   | V <sub>DDH</sub> |
| U14  | D19   | W8   | V <sub>DDH</sub> |
| U15  | D22   | W9   | GND              |
| U16  | D25   | W10  | HDST1/HA10       |
| U17  | D26   | W11  | HDST0/HA9        |
| U18  | D28   | W12  | V <sub>DDH</sub> |
| U19  | D31   | W13  | GND              |
| U20  | V <sub>DDH</sub>  | W14  | HD40/D40/ETHRXD0 |

**Table 1. MSC8113 Signal Listing by Ball Designator (continued)**

| Des. | Signal Name               | Des. | Signal Name                 |
|------|---------------------------|------|-----------------------------|
| W15  | V <sub>DDH</sub>          | AA9  | V <sub>DDH</sub>            |
| W16  | HD33/D33/reserved         | AA10 | HD54/D54/ETHTX_EN           |
| W17  | V <sub>DDH</sub>          | AA11 | HD52/D52                    |
| W18  | HD32/D32/reserved         | AA12 | V <sub>DDH</sub>            |
| W19  | GND                       | AA13 | GND                         |
| W20  | GND                       | AA14 | V <sub>DDH</sub>            |
| W21  | A7                        | AA15 | HD46/D46/ETHTXT0            |
| W22  | A6                        | AA16 | GND                         |
| Y2   | HD7                       | AA17 | HD42/D42/ETHRXD2/reserved   |
| Y3   | HD15                      | AA18 | HD38/D38/reserved           |
| Y4   | V <sub>DDH</sub>          | AA19 | HD35/D35/reserved           |
| Y5   | HD9                       | AA20 | A0                          |
| Y6   | V <sub>DD</sub>           | AA21 | A2                          |
| Y7   | HD60/D60/ETHCOL/reserved  | AA22 | A3                          |
| Y8   | HD58/D58/ETHMDC           | AB2  | GND                         |
| Y9   | GND                       | AB3  | HD13                        |
| Y10  | V <sub>DDH</sub>          | AB4  | HD11                        |
| Y11  | HD51/D51                  | AB5  | HD8                         |
| Y12  | GND                       | AB6  | HD62/D62                    |
| Y13  | V <sub>DDH</sub>          | AB7  | HD61/D61                    |
| Y14  | HD43/D43/ETHRXD3/reserved | AB8  | HD57/D57/ETHRX_ER           |
| Y15  | GND                       | AB9  | HD56/D56/ETHRX_DV/ETHCRS_DV |
| Y16  | V <sub>DDH</sub>          | AB10 | HD55/D55/ETHTX_ER/reserved  |
| Y17  | GND                       | AB11 | HD53/D53                    |
| Y18  | HD37/D37/reserved         | AB12 | HD50/D50                    |
| Y19  | HD34/D34/reserved         | AB13 | HD49/D49/ETHTXD3/reserved   |
| Y20  | V <sub>DDH</sub>          | AB14 | HD48/D48/ETHTXD2/reserved   |
| Y21  | A4                        | AB15 | HD47/D47/ETHTXD1            |
| Y22  | A5                        | AB16 | HD45/D45                    |
| AA2  | V <sub>DD</sub>           | AB17 | HD44/D44                    |
| AA3  | HD14                      | AB18 | HD41/D41/ETHRXD1            |
| AA4  | HD12                      | AB19 | HD39/D39/reserved           |
| AA5  | HD10                      | AB20 | HD36/D36/reserved           |
| AA6  | HD63/D63                  | AB21 | A1                          |
| AA7  | HD59/D59/ETHMDIO          | AB22 | V <sub>DD</sub>             |
| AA8  | GND                       |      |                             |

## 2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8113 Reference Manual*.

### 2.1 Maximum Ratings

#### CAUTION

**This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or  $V_{DD}$ ).**

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

**Table 2** describes the maximum electrical ratings for the MSC8113.

**Table 2. Absolute Maximum Ratings**

| Rating                         | Symbol  | Value       | Unit |
|--------------------------------|---|-------------|------|
| Core and PLL supply voltage    | $V_{DD}$  | -0.2 to 1.6 | V    |
| I/O supply voltage             | $V_{DDH}$   | -0.2 to 4.0 | V    |
| Input voltage                  | $V_{IN}$  | -0.2 to 4.0 | V    |
| Maximum operating temperature: | $T_J$   | 105         | °C   |
| Minimum operating temperature  | $T_J$   | -40         | °C   |
| Storage temperature range      | $T_{STG}$   | -55 to +150 | °C   |
| <b>Notes:</b>                  | <ol style="list-style-type: none"> <li>1. Functional operating conditions are given in <b>Table 3</b>.</li> <li>2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.</li> <li>3. <b>Section 3.5, Thermal Considerations</b> includes a formula for computing the chip junction temperature (<math>T_J</math>).</li> </ol> |             |      |

## 2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

| Rating                       | Symbol                  | Value                 | Unit |
|------------------------------|-------------------------|-----------------------|------|
| Core and PLL supply voltage: | $V_{DD}$<br>$V_{CCSYN}$ | 1.07 to 1.13          | V    |
| I/O supply voltage           | $V_{DDH}$               | 3.135 to 3.465        | V    |
| Input voltage                | $V_{IN}$                | -0.2 to $V_{DDH}+0.2$ | V    |
| Operating temperature range: | $T_J$                   | -40 to 105            | °C   |

## 2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8113 for the FC-PBGA packages.

**Table 4. Thermal Characteristics for the MSC8113**

| Characteristic  | Symbol          | FC-PBGA<br>20 × 20 mm <sup>5</sup> |                               | Unit |
|---|-----------------|------------------------------------|-------------------------------|------|
|   |                 | Natural<br>Convection              | 200 ft/min<br>(1 m/s) airflow |      |
| Junction-to-ambient <sup>1, 2</sup>                   | $R_{\theta JA}$ | 26                                 | 21                            | °C/W |
| Junction-to-ambient, four-layer board <sup>1, 3</sup> | $R_{\theta JA}$ | 19                                 | 15                            | °C/W |
| Junction-to-board (bottom) <sup>4</sup>               | $R_{\theta JB}$ | 9                                  |                               | °C/W |
| Junction-to-case <sup>5</sup>                         | $R_{\theta JC}$ | 0.9                                |                               | °C/W |
| Junction-to-package-top <sup>6</sup>                  | $\Psi_{JT}$     | 1                                  |                               | °C/W |

**Notes:**

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- Per JEDEC JESD51-6 with the board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

## 2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8113. The measurements in Table 5 assume the following system conditions:

- $T_A = 25\text{ °C}$
- $V_{DD} = 1.1\text{ V nominal} = 1.07\text{--}1.13\text{ V}_{DC}$
- $V_{DDH} = 3.3\text{ V} \pm 5\% V_{DC}$
- $GND = 0\text{ V}_{DC}$

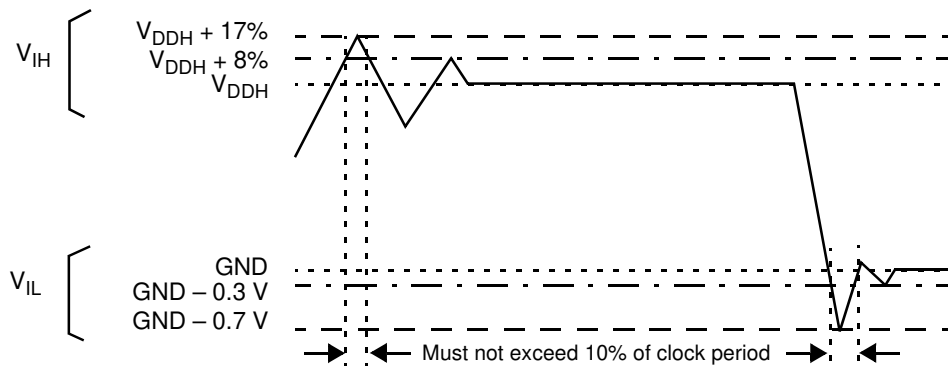
**Note:** The leakage current is measured for nominal  $V_{DDH}$  and  $V_{DD}$ .

Table 5. DC Electrical Characteristics

| Characteristic   | Symbol    | Min  | Typical          | Max   | Unit          |
|--|-----------|------|------------------|-------|---------------|
| Input high voltage <sup>1</sup> , all inputs except CLKIN                | $V_{IH}$  | 2.0  | —                | 3.465 | V             |
| Input low voltage <sup>1</sup>   | $V_{IL}$  | GND  | 0                | 0.8   | V             |
| CLKIN input high voltage   | $V_{IHC}$ | 2.4  | 3.0              | 3.465 | V             |
| CLKIN input low voltage  | $V_{ILC}$ | GND  | 0                | 0.8   | V             |
| Input leakage current, $V_{IN} = V_{DDH}$                                | $I_{IN}$  | -1.0 | 0.09             | 1     | $\mu\text{A}$ |
| Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$ | $I_{OZ}$  | -1.0 | 0.09             | 1     | $\mu\text{A}$ |
| Signal low input current, $V_{IL} = 0.8 \text{ V}^2$                     | $I_L$     | -1.0 | 0.09             | 1     | $\mu\text{A}$ |
| Signal high input current, $V_{IH} = 2.0 \text{ V}^2$                    | $I_H$     | -1.0 | 0.09             | 1     | $\mu\text{A}$ |
| Output high voltage, $I_{OH} = -2 \text{ mA}$ , except open drain pins   | $V_{OH}$  | 2.0  | 3.0              | —     | V             |
| Output low voltage, $I_{OL} = 3.2 \text{ mA}$                            | $V_{OL}$  | —    | 0                | 0.4   | V             |
| Internal supply current:   |           |      |                  |       |               |
| • Wait mode  | $I_{DDW}$ | —    | 375 <sup>3</sup> | —     | mA            |
| • Stop mode  | $I_{DDS}$ | —    | 290 <sup>3</sup> | —     | mA            |
| Typical power 400 MHz at 1.1 V <sup>4</sup>                              | P         | —    | 826              | —     | mW            |
| Typical power 300 MHz at 1.1 V <sup>4</sup>                              |           | —    | 676              | —     | mW            |

**Notes:**

1. See **Figure 5** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.1 V core at 25°C junction temperature.
4. The typical power values were calculated using a power calculator configured for three cores performing an EFR code with the device running at the specified operating frequency and a junction temperature of 25°C. No peripherals were included. The calculator was created using CodeWarrior<sup>®</sup> 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Section 3** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines (AN2601)*.


 Figure 5. Overshoot/Undershoot Voltage for  $V_{IH}$  and  $V_{IL}$



## 2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

### 2.5.1 Output Buffer Impedances

Table 6. Output Buffer Impedances

| Output Buffers    | Typical Impedance (Ω) |
|-------------------|-----------------------|
| System bus        | 50                    |
| Memory controller | 50                    |
| Parallel I/O      | 50                    |

**Note:** These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.

### 2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8113 device:

- $\overline{\text{PORESET}}$  and  $\overline{\text{TRST}}$  must be asserted externally for the duration of the power-up sequence. See **Table 11** for timing.
- If possible, bring up the  $V_{\text{DD}}$  and  $V_{\text{DDH}}$  levels together. For designs with separate power supplies, bring up the  $V_{\text{DD}}$  levels and then the  $V_{\text{DDH}}$  levels (see **Figure 7**).
- CLKIN should start toggling at least 16 cycles (starting after  $V_{\text{DDH}}$  reaches its nominal level) before  $\overline{\text{PORESET}}$  deassertion to guarantee correct device operation (see **Figure 6** and **Figure 7**).
- CLKIN must not be pulled high during  $V_{\text{DDH}}$  power-up. CLKIN can toggle during this period.

The following figures show acceptable start-up sequence examples. **Figure 6** shows a sequence in which  $V_{\text{DD}}$  and  $V_{\text{DDH}}$  are raised together. **Figure 7** shows a sequence in which  $V_{\text{DDH}}$  is raised after  $V_{\text{DD}}$  and CLKIN begins to toggle as  $V_{\text{DDH}}$  rises.

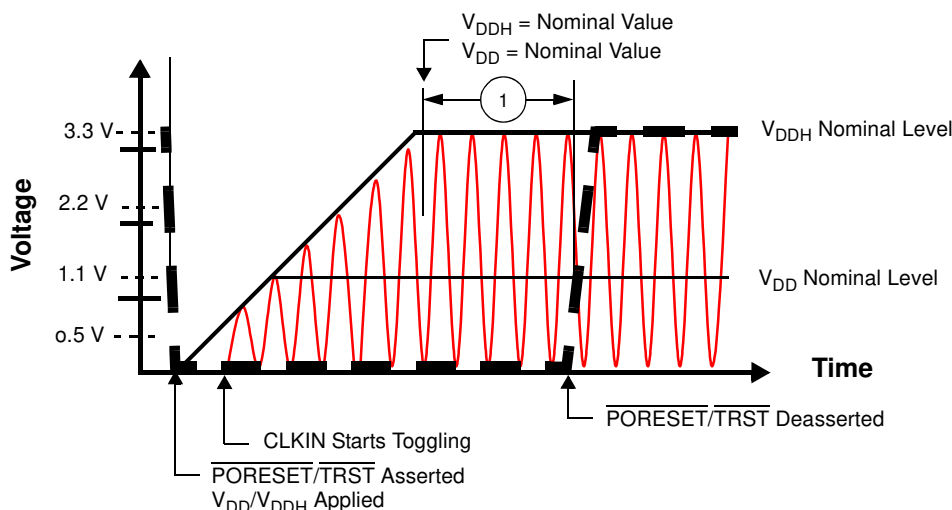
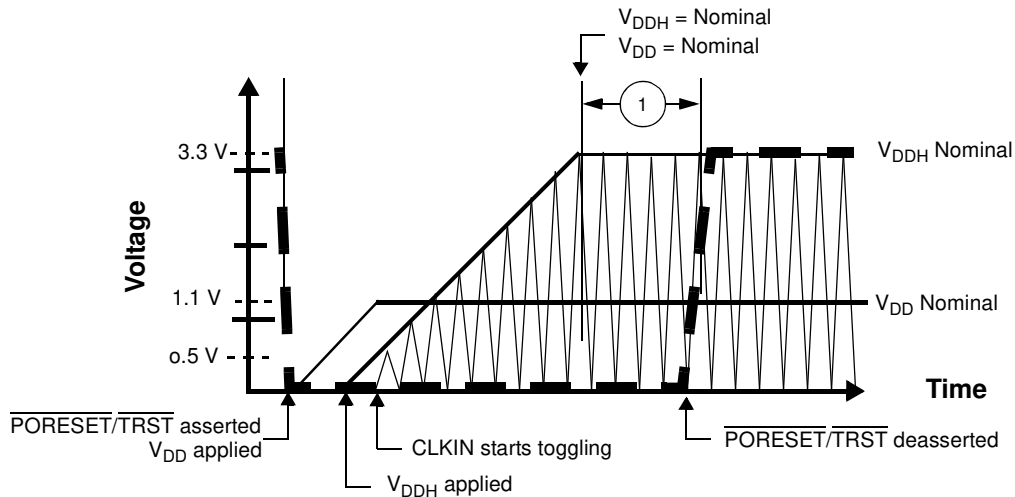
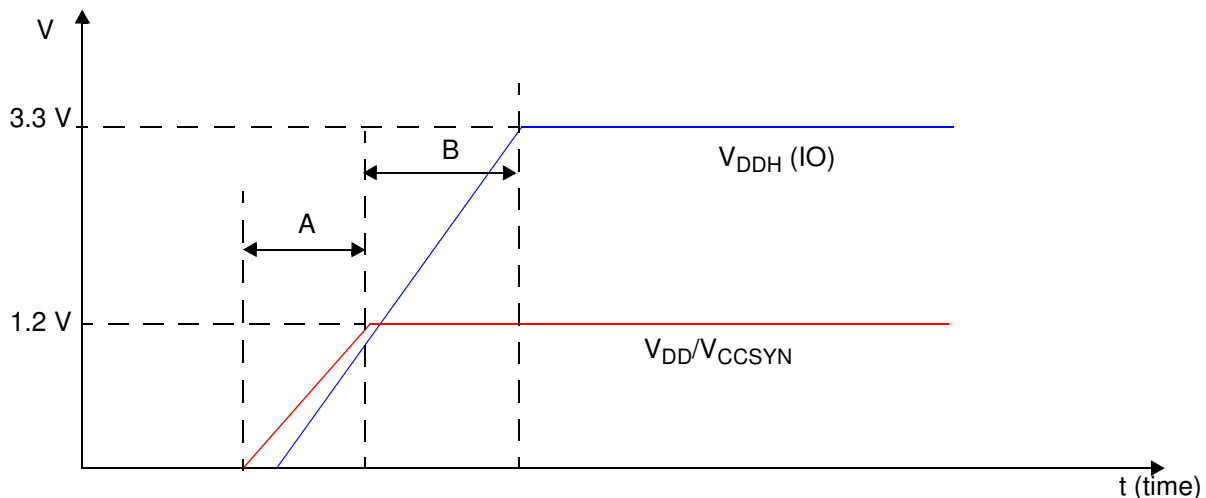


Figure 6. Start-Up Sequence:  $V_{\text{DD}}$  and  $V_{\text{DDH}}$  Raised Together



**Figure 7. Start-Up Sequence:  $V_{DD}$  Raised Before  $V_{DDH}$  with CLKIN Started with  $V_{DDH}$**

In all cases, the power-up sequence must follow the guidelines shown in **Figure 8**.



**Figure 8. Power-Up Sequence for  $V_{DDH}$  and  $V_{DD}/V_{CCSYN}$**

The following rules apply:

1. During time interval A,  $V_{DDH}$  should always be equal to or less than the  $V_{DD}/V_{CCSYN}$  voltage level. The duration of interval A should be kept below 10 ms.
2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

### 2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

**Table 7. Maximum Frequencies**

| Characteristic               | Maximum in MHz |
|------------------------------|----------------|
| Core frequency               | 300/400        |
| Reference frequency (REFCLK) | 100/133        |

**Table 7. Maximum Frequencies**

| Characteristic   | Maximum in MHz  |
|--|---|
| Internal bus frequency (BCLK)  | 100/133   |
| DSI clock frequency (HCLKIN)<br>• Core frequency = 300 MHz<br>• Core frequency = 400 MHz | HCLKIN ≤ (min{70 MHz, CLKOUT})<br>HCLKIN ≤ (min{100 MHz, CLKOUT}) |
| External clock frequency (CLKIN or CLKOUT)   | 100/133   |

**Table 8. Clock Frequencies**

| Characteristics   | Symbol              | 300 MHz Device |     | 400 MHz Device |       |
|---|---------------------|----------------|-----|----------------|-------|
|   |                     | Min            | Max | Min            | Max   |
| CLKIN frequency   | F <sub>CLKIN</sub>  | 20             | 100 | 20             | 133.3 |
| BCLK frequency  | F <sub>BCLK</sub>   | 40             | 100 | 40             | 133.3 |
| Reference clock (REFCLK) frequency  | F <sub>REFCLK</sub> | 40             | 100 | 40             | 133.3 |
| Output clock (CLKOUT) frequency   | F <sub>CLKOUT</sub> | 40             | 100 | 40             | 133.3 |
| SC140 core clock frequency  | F <sub>CORE</sub>   | 200            | 300 | 200            | 400   |
| <b>Note:</b> The rise and fall time of external clocks should be 3 ns maximum |                     |                |     |                |       |

**Table 9. System Clock Parameters**

| Characteristic   | Min | Max                | Unit              |
|--|-----|--------------------|-------------------|
| Phase jitter between BCLK and CLKIN                                    | —   | 0.3                | ns                |
| CLKIN frequency  | 20  | see <b>Table 8</b> | MHz               |
| CLKIN slope  | —   | 3                  | ns                |
| PLL input clock (after predivider)                                     | 20  | 100                | MHz               |
| PLL output frequency (VCO output)<br>• 300 MHz core<br>• 400 MHz core  | 800 | 1200<br>1600       | MHz<br>MHz<br>MHz |
| CLKOUT frequency jitter <sup>1</sup>                                   | —   | 200                | ps                |
| CLKOUT phase jitter <sup>1</sup> with CLKIN phase jitter of ±100 ps.   | —   | 500                | ps                |
| <b>Notes:</b> 1. Peak-to-peak.<br>2. Not tested. Guaranteed by design. |     |                    |                   |

## 2.5.4 Reset Timing

The MSC8113 has several inputs to the reset logic:

- Power-on reset ( $\overline{\text{PORESET}}$ )
- External hard reset ( $\overline{\text{HRESET}}$ )
- External soft reset ( $\overline{\text{SRESET}}$ )
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8113 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.

Table 10. Reset Sources

| Name                               | Direction     | Description   |
|------------------------------------|---------------|---|
| Power-on reset (PORESET)           | Input         | Initiates the power-on reset flow that resets the MSC8113 and configures various attributes of the MSC8113. On PORESET, the entire MSC8113 device is reset. SPLL states is reset, HRESET and SRESET are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when PORESET is asserted.   |
| External hard reset (HRESET)       | Input/ Output | Initiates the hard reset flow that configures various attributes of the MSC8113. While HRESET is asserted, SRESET is also asserted. HRESET is an open-drain pin. Upon hard reset, HRESET and SRESET are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigured. These features are defined in the 32-bit hard reset configuration word described in <i>Hard Reset Configuration Word</i> section of the <i>Reset</i> chapter in the <i>MSC8113 Reference Manual</i> . |
| External soft reset (SRESET)       | Input/ Output | Initiates the soft reset flow. The MSC8113 detects an external assertion of SRESET only if it occurs while the MSC8113 is not asserting reset. SRESET is an open-drain pin. Upon soft reset, SRESET is driven, the SC140 extended cores are reset, and system configuration is maintained.  |
| Software watchdog reset            | Internal      | When the MSC8113 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.   |
| Bus monitor reset                  | Internal      | When the MSC8113 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.  |
| Host reset command through the TAP | Internal      | When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.  |

Table 11 summarizes the reset actions that occur as a result of the different reset sources.

Table 11. Reset Actions for Each Reset Source

| Reset Action/Reset Source   | Power-On Reset (PORESET) | Hard Reset (HRESET)                                     | Soft Reset (SRESET) |                                       |
|---|--------------------------|---|---------------------|---------------------------------------|
|   | External only            | External or Internal (Software Watchdog or Bus Monitor) | External            | JTAG Command: EXTEST, CLAMP, or HIGHZ |
| Configuration pins sampled (Refer to Section 2.5.4.1 for details).            | Yes                      | No  | No                  | No                                    |
| SPLL state reset  | Yes                      | No  | No                  | No                                    |
| System reset configuration write through the DSI                              | Yes                      | No  | No                  | No                                    |
| System reset configuration write through the system bus                       | Yes                      | Yes   | No                  | No                                    |
| HRESET driven   | Yes                      | Yes   | No                  | No                                    |
| SIU registers reset   | Yes                      | Yes   | No                  | No                                    |
| IPBus modules reset (TDM, UART, Timers, DSI, IPBus master, GIC, HS, and GPIO) | Yes                      | Yes   | Yes                 | Yes                                   |
| SRESET driven   | Yes                      | Yes   | Yes                 | Depends on command                    |
| SC140 extended cores reset  | Yes                      | Yes   | Yes                 | Yes                                   |
| MQBS reset  | Yes                      | Yes   | Yes                 | Yes                                   |

### 2.5.4.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after V<sub>DD</sub> and V<sub>DDH</sub> are both at their nominal levels.

### 2.5.4.2 Reset Configuration

The MSC8113 has two mechanisms for writing the reset configuration:

- Through the direct slave interface (DSI)
- Through the system bus. When the reset configuration is written through the system bus, the MSC8113 acts as a configuration master or a configuration slave. If configuration slave is selected, but no special configuration word is written, a default configuration word is applied.

Fourteen signal levels (see **Chapter 1** for signal description details) are sampled on  $\overline{\text{PORESET}}$  deassertion to define the Reset Configuration Mode and boot and operating conditions:

- $\overline{\text{RSTCONF}}$
- CNFGS
- DSISYNC
- DSI64
- CHIP\_ID[0–3]
- BM[0–2]
- SWTE
- MODCK[1–2]

### 2.5.4.3 Reset Timing Tables

**Table 12** and **Figure 9** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

**Table 12. Timing for a Reset Configuration Write through the DSI or System Bus**

| No.          | Characteristics  | Expression  | Min               | Max             | Unit  |
|--------------|--|---|-------------------|-----------------|---|
| 1            | Required external $\overline{\text{PORESET}}$ duration minimum<br><ul style="list-style-type: none"> <li>• CLKIN = 20 MHz</li> <li>• CLKIN = 100 MHz (300 MHz core)</li> <li>• CLKIN = 133 MHz (400 MHz core)</li> </ul>   | $16/\text{CLKIN}$   | 800<br>160<br>120 | —<br>—<br>—     | ns<br>ns<br>ns                                  |
| 2            | Delay from deassertion of external $\overline{\text{PORESET}}$ to deassertion of internal $\overline{\text{PORESET}}$<br><ul style="list-style-type: none"> <li>• CLKIN = 20 MHz to 133 MHz</li> </ul>   | $1024/\text{CLKIN}$   | 6.17              | 51.2            | $\mu\text{s}$                                   |
| 3            | Delay from de-assertion of internal $\overline{\text{PORESET}}$ to SPLL lock<br><ul style="list-style-type: none"> <li>• CLKIN = 20 MHz (RDF = 1)</li> <li>• CLKIN = 100 MHz (RDF = 1) (300 MHz core)</li> <li>• CLKIN = 133 MHz (RDF = 2) (400 MHz core)</li> </ul> | $6400/(\text{CLKIN}/\text{RDF})$<br>(PLL reference clock-division factor) | 320<br>64<br>96   | 320<br>64<br>96 | $\mu\text{s}$<br>$\mu\text{s}$<br>$\mu\text{s}$ |
| 5            | Delay from SPLL to $\overline{\text{HRESET}}$ deassertion<br><ul style="list-style-type: none"> <li>• REFCLK = 40 MHz to 133 MHz</li> </ul>  | $512/\text{REFCLK}$   | 3.08              | 12.8            | $\mu\text{s}$                                   |
| 6            | Delay from SPLL lock to $\overline{\text{SRESET}}$ deassertion<br><ul style="list-style-type: none"> <li>• REFCLK = 40 MHz to 133 MHz</li> </ul>   | $515/\text{REFCLK}$   | 3.10              | 12.88           | $\mu\text{s}$                                   |
| 7            | Setup time from assertion of $\overline{\text{RSTCONF}}$ , CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2] before deassertion of $\overline{\text{PORESET}}$  |   | 3                 | —               | ns  |
| 8            | Hold time from deassertion of $\overline{\text{PORESET}}$ to deassertion of $\overline{\text{RSTCONF}}$ , CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2]   |   | 5                 | —               | ns  |
| <b>Note:</b> | Timings are not tested, but are guaranteed by design.  |   |                   |                 |   |

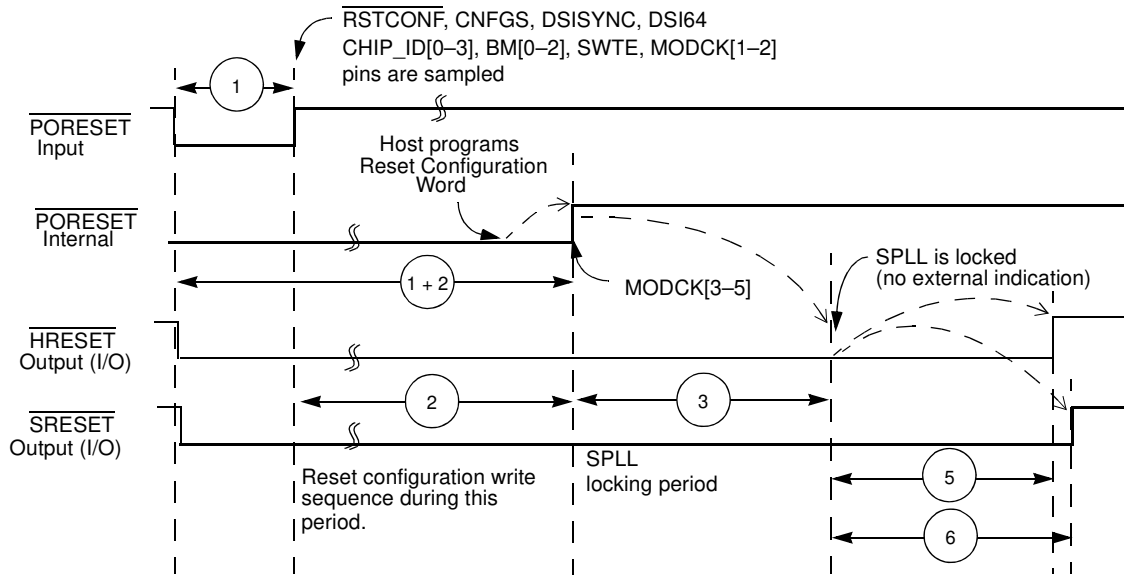


Figure 9. Timing Diagram for a Reset Configuration Write

## 2.5.5 System Bus Access Timing

### 2.5.5.1 Core Data Transfers

Generally, all MSC8113 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 13** shows.

Table 13. Tick Spacing for Memory Controller Signals

| BCLK/SC140 clock    | Tick Spacing (T1 Occurs at the Rising Edge of REFCLK) |            |             |
|---------------------|---|------------|-------------|
|                     | T2  | T3         | T4          |
| 1:4, 1:6, 1:8, 1:10 | 1/4 REFCLK  | 1/2 REFCLK | 3/4 REFCLK  |
| 1:3                 | 1/6 REFCLK  | 1/2 REFCLK | 4/6 REFCLK  |
| 1:5                 | 2/10 REFCLK   | 1/2 REFCLK | 7/10 REFCLK |

Figure 10 is a graphical representation of **Table 13**.

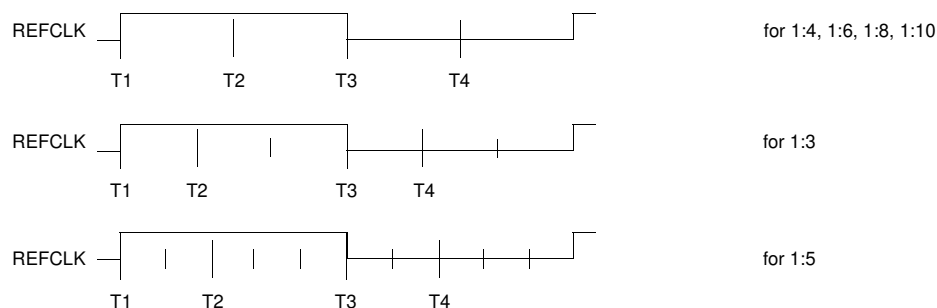


Figure 10. Internal Tick Spacing for Memory Controller Signals

The UPM machine and GPCM machine outputs change on the internal tick selected by the memory controller configuration. The AC timing specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

**Table 14. AC Timing for SIU Inputs**

| No.             | Characteristic  | Ref = CLKIN at 1.1 V and 100/133 MHz | Units    |
|-----------------|---|--------------------------------------|----------|
| 10              | Hold time for all signals after the 50% level of the REFCLK rising edge   | 0.5                                  | ns       |
| 11a             | $\overline{\text{ARTRY}}/\overline{\text{ABB}}$ set-up time before the 50% level of the REFCLK rising edge  | 3.1                                  | ns       |
| 11b             | $\overline{\text{DBG}}/\overline{\text{DBB}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{TC}}$ set-up time before the 50% level of the REFCLK rising edge   | 3.6                                  | ns       |
| 11c             | $\overline{\text{AACK}}$ set-up time before the 50% level of the REFCLK rising edge   | 3.0                                  | ns       |
| 11d             | $\overline{\text{TA}}/\overline{\text{TEA}}/\overline{\text{PSDVAL}}$ set-up time before the 50% level of the REFCLK rising edge<br><ul style="list-style-type: none"> <li>• Data-pipeline mode</li> <li>• Non-pipeline mode</li> </ul>   | 3.5<br>4.4                           | ns<br>ns |
| 12              | Data bus set-up time before REFCLK rising edge in Normal mode<br><ul style="list-style-type: none"> <li>• Data-pipeline mode</li> <li>• Non-pipeline mode</li> </ul>  | 1.9<br>4.2                           | ns<br>ns |
| 13 <sup>1</sup> | Data bus set-up time before the 50% level of the REFCLK rising edge in ECC and PARITY modes<br><ul style="list-style-type: none"> <li>• Data-pipeline mode</li> <li>• Non-pipeline mode</li> </ul>  | 2.0<br>8.2                           | ns<br>ns |
| 14 <sup>1</sup> | DP set-up time before the 50% level of the REFCLK rising edge<br><ul style="list-style-type: none"> <li>• Data-pipeline mode</li> <li>• Non-pipeline mode</li> </ul>  | 2.0<br>7.9                           | ns<br>ns |
| 15a             | $\overline{\text{TS}}$ and Address bus set-up time before the 50% level of the REFCLK rising edge<br><ul style="list-style-type: none"> <li>• Extra cycle mode (SIUBCR[EXDD] = 0)</li> <li>• No extra cycle mode (SIUBCR[EXDD] = 1)</li> </ul>  | 4.2<br>5.5                           | ns<br>ns |
| 15b             | Address attributes: $\overline{\text{TT}}/\overline{\text{TBST}}/\overline{\text{TSZ}}/\overline{\text{GBL}}$ set-up time before the 50% level of the REFCLK rising edge<br><ul style="list-style-type: none"> <li>• Extra cycle mode (SIUBCR[EXDD] = 0)</li> <li>• No extra cycle mode (SIUBCR[EXDD] = 1)</li> </ul> | 3.7<br>4.8                           | ns<br>ns |
| 16              | PUPMWAIT signal set-up time before the 50% level of the REFCLK rising edge  | 3.7                                  | ns       |
| 17              | $\overline{\text{IRQx}}$ setup time before the 50% level; of the REFCLK rising edge <sup>3</sup>  | 4.0                                  | ns       |
| 18              | $\overline{\text{IRQx}}$ minimum pulse width <sup>3</sup>   | $6.0 + T_{\text{REFCLK}}$            | ns       |
| <b>Notes:</b>   | <ol style="list-style-type: none"> <li>1. Timings specifications 13 and 14 in non-pipeline mode are more restrictive than MSC8102 timings.</li> <li>2. Values are measured from the 50% TTL transition level relative to the 50% level of the REFCLK rising edge.</li> <li>3. Guaranteed by design.</li> </ol>        |                                      |          |

Table 15. AC Timing for SIU Outputs

| No.             | Characteristic  | Bus Speed in MHz <sup>3</sup><br>Ref = CLKIN at 1.1 V<br>and 100/ 133 MHz | Units    |
|-----------------|---|---|----------|
| 30 <sup>2</sup> | Minimum delay from the 50% level of the REFCLK for all signals  | 0.9   | ns       |
| 31              | $\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ max delay from the 50% level of the REFCLK rising edge  | 6.0   | ns       |
| 32a             | Address bus max delay from the 50% level of the REFCLK rising edge <ul style="list-style-type: none"> <li>• Multi-master mode (SIUBCR[EBM] = 1)</li> <li>• Single-master mode (SIUBCR[EBM] = 0)</li> </ul>  | 6.4<br>5.3  | ns<br>ns |
| 32b             | Address attributes: $\overline{\text{TT}}[0-1]/\overline{\text{TBST}}/\overline{\text{TSZ}}/\overline{\text{GBL}}$ max delay from the 50% level of the REFCLK rising edge   | 6.4   | ns       |
| 32c             | Address attributes: $\overline{\text{TT}}[2-4]/\overline{\text{TC}}$ max delay from the 50% level of the REFCLK rising edge   | 6.9   | ns       |
| 32d             | $\overline{\text{BADDR}}$ max delay from the 50% level of the REFCLK rising edge  | 5.2   | ns       |
| 33a             | Data bus max delay from the 50% level of the REFCLK rising edge <ul style="list-style-type: none"> <li>• Data-pipeline mode</li> <li>• Non-pipeline mode</li> </ul>   | 4.8<br>7.1  | ns<br>ns |
| 33b             | DP max delay from the 50% level of the REFCLK rising edge <ul style="list-style-type: none"> <li>• Data-pipeline mode</li> <li>• Non-pipeline mode</li> </ul>   | 6.0<br>7.5  | ns<br>ns |
| 34              | Memory controller signals/ $\overline{\text{ALE}}/\overline{\text{CS}}[0-4]$ max delay from the 50% level of the REFCLK rising edge   | 5.1   | ns       |
| 35a             | $\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{DBB}}$ max delay from the 50% level of the REFCLK rising edge  | 6.0   | ns       |
| 35b             | $\overline{\text{AACK}}/\overline{\text{ABB}}/\overline{\text{TS}}/\overline{\text{CS}}[5-7]$ max delay from the 50% level of the REFCLK rising edge  | 5.5   | ns       |
| <b>Notes:</b>   | <ol style="list-style-type: none"> <li>1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level and assume a 20 pF load except where otherwise specified.</li> <li>2. Except for specification 30, which is specified for a 10 pF load, all timings in this table are specified for a 20 pF load. Decreasing the load results in a timing decrease at the rate of 0.3 ns per 5 pF decrease in load. Increasing the load results in a timing increase at the rate of 0.15 ns per 5 pF increase in load.</li> <li>3. The maximum bus frequency depends on the mode:                             <ul style="list-style-type: none"> <li>• In 60x-compatible mode connected to another MSC8113 device, the frequency is determined by adding the input and output longest timing values, which results in the total delay for 20 pF output capacitance. You must also account for other influences that can affect timing, such as on-board clock skews, on-board noise delays, and so on.</li> <li>• In single-master mode, the frequency depends on the timing of the devices connected to the MSC8113.</li> <li>• To achieve maximum performance on the bus in single-master mode, disable the DBB signal by writing a 1 to the SIUMCR[BDD] bit. See the SIU chapter in the <i>MSC8113 Reference Manual</i> for details.</li> </ul> </li> </ol> |   |          |



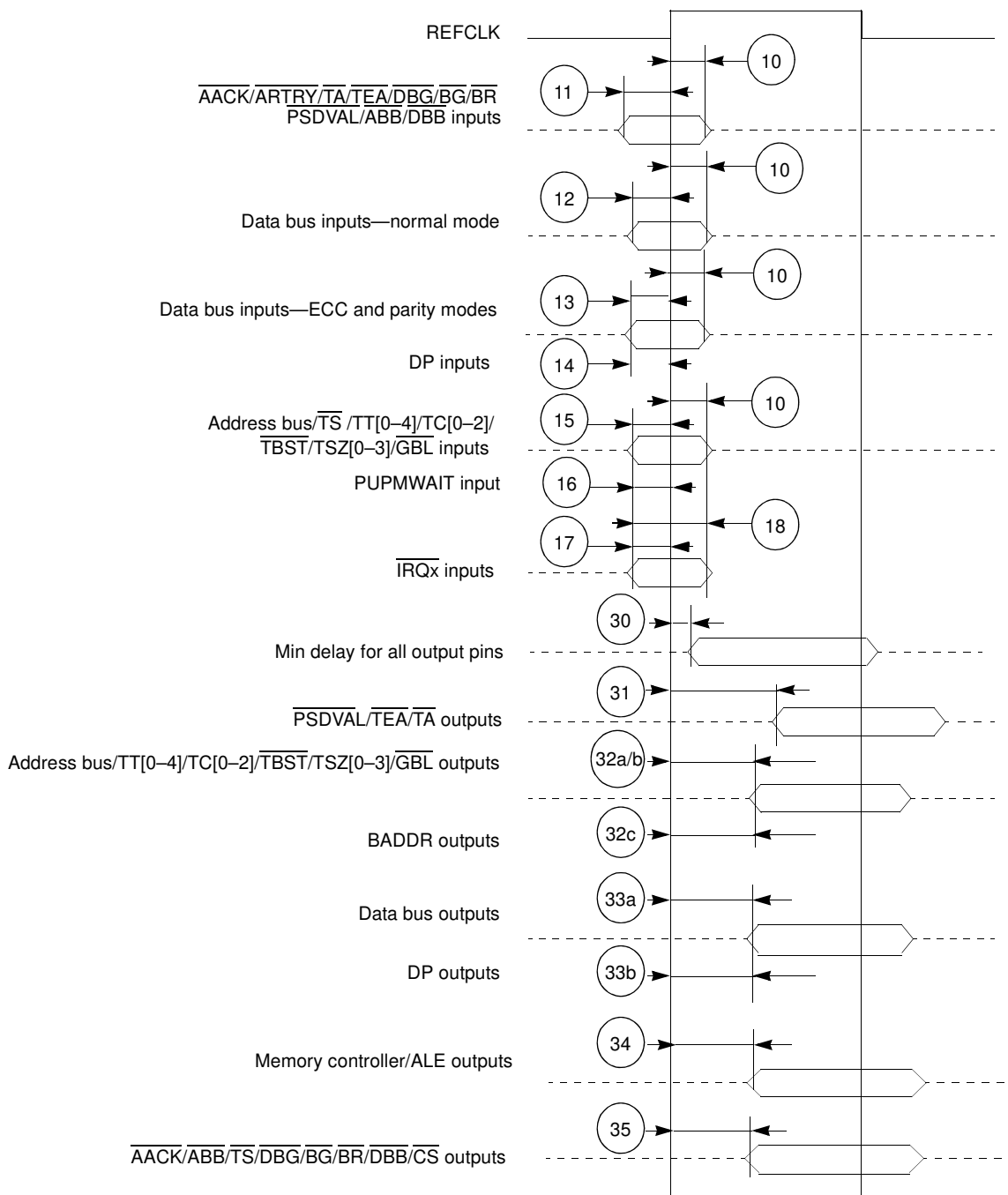


Figure 11. SIU Timing Diagram

### 2.5.5.2 CLKIN to CLKOUT Skew

Table 17 describes the CLKOUT-to-CLKIN skew timing.

Table 16. CLKOUT Skew

| No.  | Characteristic   | Min <sup>1</sup> | Max <sup>1</sup> | Units |
|--|--|------------------|------------------|-------|
| 20   | Rise-to-rise skew  | 0.0              | 0.95             | ns    |
| 21   | Fall-to-fall skew  | -1.5             | 1.0              | ns    |
| 23   | CLKOUT phase (1.1 V, 133 MHz)<br>• Phase high<br>• Phase low | 2.2              | —                | ns    |
|  |  | 2.2              | —                | ns    |
| 24   | CLKOUT phase (1.1 V, 100 MHz)<br>• Phase high<br>• Phase low | 3.3              | —                | ns    |
|  |  | 3.3              | —                | ns    |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. A positive number indicates that CLKOUT precedes CLKIN, A negative number indicates that CLKOUT follows CLKIN.</li> <li>2. Skews are measured in clock mode 29, with a CLKIN:CLKOUT ratio of 1:1. The same skew is valid for all clock modes.</li> <li>3. CLKOUT skews are measured using a load of 10 pF.</li> <li>4. CLKOUT skews and phase are not measured for 500/166 Mhz parts because these parts only use CLKIN mode.</li> </ol> |  |                  |                  |       |

For designs that use the CLKOUT synchronization mode, use the skew values listed in Table 16 to adjust the rise-to-fall timing values specified for CLKIN synchronization. Figure 12 shows the relationship between the CLKOUT and CLKIN timings.

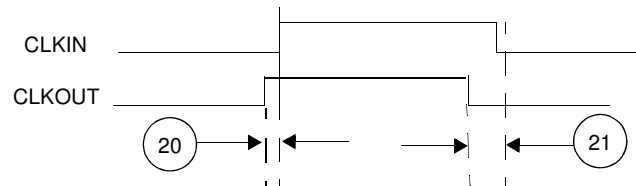


Figure 12. CLKOUT and CLKIN Signals.

### 2.5.5.3 DMA Data Transfers

Table 17 describes the DMA signal timing.

Table 17. DMA Signals

| No. | Characteristic  | Ref = CLKIN |     | Units |
|-----|---|-------------|-----|-------|
|     |   | Min         | Max |       |
| 37  | DREQ set-up time before the 50% level of the falling edge of REFCLK | 5.0         | —   | ns    |
| 38  | DREQ hold time after the 50% level of the falling edge of REFCLK    | 0.5         | —   | ns    |
| 39  | DONE set-up time before the 50% level of the rising edge of REFCLK  | 5.0         | —   | ns    |
| 40  | DONE hold time after the 50% level of the rising edge of REFCLK     | 0.5         | —   | ns    |
| 41  | DACK/DRACK/DONE delay after the 50% level of the REFCLK rising edge | 0.5         | 7.5 | ns    |

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in Table 17. Figure 13 shows synchronous peripheral interaction.