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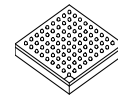
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MSC8144



FC-PBGA-783
29 mm × 29 mm

Quad Core Digital Signal Processor

- Four StarCore® SC3400 DSP subsystems, each with an SC3400 DSP core, 16 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, memory management unit (MMU), extended programmable interrupt controller (EPIC), two general-purpose 32-bit timers, debug and profiling support, and low-power Wait and Stop processing modes.
- Chip-level arbitration and system (CLASS) that provides full fabric non-blocking arbitration between the processing elements and other initiators and the M2 memory, DDR SRAM controller, device configuration control and status registers, and other targets.
- 128 Kbyte L2 shared instruction cache.
- 512 Kbyte M2 memory for critical data and temporary data buffering.
- 10 Mbyte 128-bit wide M3 memory.
- 96 Kbyte boot ROM.
- Three input clocks (shared, global, and differential).
- Four PLLs (system, core, global, and serial RapidIO).
- DDR controller with up to a 200 MHz clock (400 MHz data rate), 16/32 bit data bus, supporting up to 1 Gbyte in up to two banks and support for DDR1 and DDR2.
- DMA controller with 16 bidirectional channels with up to 1024 buffer descriptors, and programmable priority, buffer, and multiplexing configuration.
- Up to eight independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/ μ -law conversion, up to 128 Mbps data rate for all channels, with glueless interface to E1 or T1 framers, and can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.
- QUICC Engine™ technology subsystem with dual RISC processors, 48 Kbyte multi-master RAM, 48 Kbyte instruction RAM, supporting three communication controllers with one ATM and two Gigabit Ethernet interfaces, to offload scheduling tasks from the DSP cores.
- The two Ethernet controllers support 10/100/1000 Mbps operations via MII/RMII/SMII/RGMII/SGMII and the SGMII protocol using a 4-pin SerDes interface at 1000 Mbps data rate only.
- The ATM controller supports UTOPIA level II 8/16 bits at 25/50 MHz in UTOPIA/POS mode with adaptation layer support AAL0, AAL2, and AAL5.
- PCI designed to comply with the PCI specification revision 2.2 at 33 MHz or 66 MHz with access to all PCI address spaces.
- Serial RapidIO® 1x/4x endpoint corresponds to Specification 1.2 of the RapidIO trade association, and supports read, write, messages, doorbells, and maintenance accesses in inbound mode, and messages and doorbells in outbound mode.
- I/O interrupt concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to $\overline{\text{INT_OUT}}$, $\overline{\text{NMI_OUT}}$, and the cores.
- UART that permits full-duplex operation with a bit rate of up to 6.25 Mbps.
- Serial peripheral interface (SPI).
- Four timer modules, each with four configurable 16-bit timers.
- Four software watchdog timer (SWT) modules.
- Up to 32 general-purpose input/output (GPIO) ports, 16 of which can be configured as maskable interrupt inputs.
- I²C interface that allows booting from EEPROM devices.
- Eight programmable hardware semaphores.
- Thirty two virtual maskable interrupts and one virtual $\overline{\text{NMI}}$ that can be generated by a simple write access.
- Optional booting via serial RapidIO port, PCI, I²C, SPI, or Ethernet interfaces.

Note: This document supports mask set M31H.

Table of Contents

1	Pin Assignments and Reset States	4	Figure 12. Transmitter Output Compliance Mask	46
1.1	FC-PBGA Ball Layout Diagrams	4	Figure 13. Single Frequency Sinusoidal Jitter Limits	48
1.2	Signal List By Ball Location	6	Figure 14. Receiver Input Compliance Mask	49
2	Electrical Characteristics	26	Figure 15. PCI AC Test Load	51
2.1	Maximum Ratings	26	Figure 16. PCI Input AC Timing Measurement Conditions	51
2.2	Recommended Operating Conditions	27	Figure 17. PCI Output AC Timing Measurement Condition	51
2.3	Default Output Driver Characteristics	28	Figure 18. TDM Inputs Signals	52
2.4	Thermal Characteristics	28	Figure 20. TDM Output Signals	53
2.5	DC Electrical Characteristics	29	Figure 21. UART Input Timing	53
2.6	AC Timings	35	Figure 22. UART Output Timing	53
3	Hardware Design Considerations	64	Figure 23. Timer Timing	54
3.1	Start-up Sequencing Recommendations	64	Figure 24. MII Management Interface Timing	55
3.2	Power Supply Design Considerations	66	Figure 25. MII Transmit AC Timing	55
3.3	Clock and Timing Signal Board Layout Considerations	67	Figure 26. AC Test Load	56
3.4	Connectivity Guidelines	67	Figure 27. MII Receive AC Timing	56
4	Ordering Information	76	Figure 28. RMIIT Transmit and Receive AC Timing	57
5	Package Information	77	Figure 29. AC Test Load	57
6	Product Documentation	77	Figure 30. SMII Mode Signal Timing	58
7	Revision History	78	Figure 31. RGMII AC Timing and Multiplexing	59
	List of Figures		Figure 32. ATM/UTOPIA/POS AC Test Load	60
	Figure 1. MSC8144 Block Diagram	3	Figure 33. ATM/UTOPIA/POS AC Timing (External Clock)	60
	Figure 2. StarCore SC3400 DSP Core Subsystem Block Diagram	3	Figure 34. SPI AC Test Load	61
	Figure 3. MSC8144 FC-PBGA Package, Top View	4	Figure 35. SPI AC Timing in Slave Mode (External Clock)	61
	Figure 4. MSC8144 FC-PBGA Package, Bottom View	5	Figure 36. SPI AC Timing in Master Mode (Internal Clock)	62
	Figure 5. SerDes Reference Clocks Input Stage	31	Figure 37. Asynchronous Signal Timing	62
	Figure 6. Start-Up Sequence with V_{DD} Raised Before V_{DDIO} with CLKIN Started with V_{DDIO}	35	Figure 38. Test Clock Input Timing	63
	Figure 7. Timing for a Reset Configuration Write	38	Figure 39. Boundary Scan (JTAG) Timing	63
	Figure 8. Timing for t_{DDKMH}	41	Figure 40. Test Access Port Timing	64
	Figure 9. DDR SDRAM Output Timing	41	Figure 41. TRST Timing	64
	Figure 10. DDR AC Test Load	42	Figure 42. V_{DDM3} , V_{DDM3IO} and V_{25M3} Power-on Sequence	65
	Figure 11. Differential V_{PP} of Transmitter or Receiver	42	Figure 44. MSC8144 Mechanical Information, 783-ball FC-PBGA Package	77

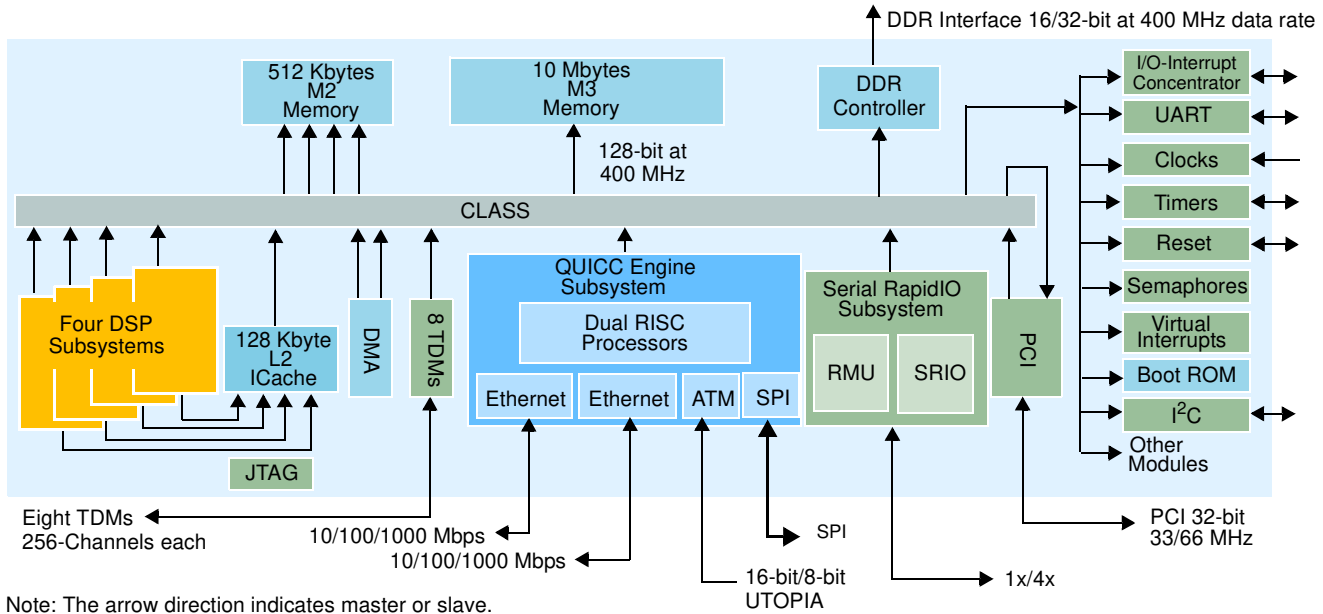


Figure 1. MSC8144 Block Diagram

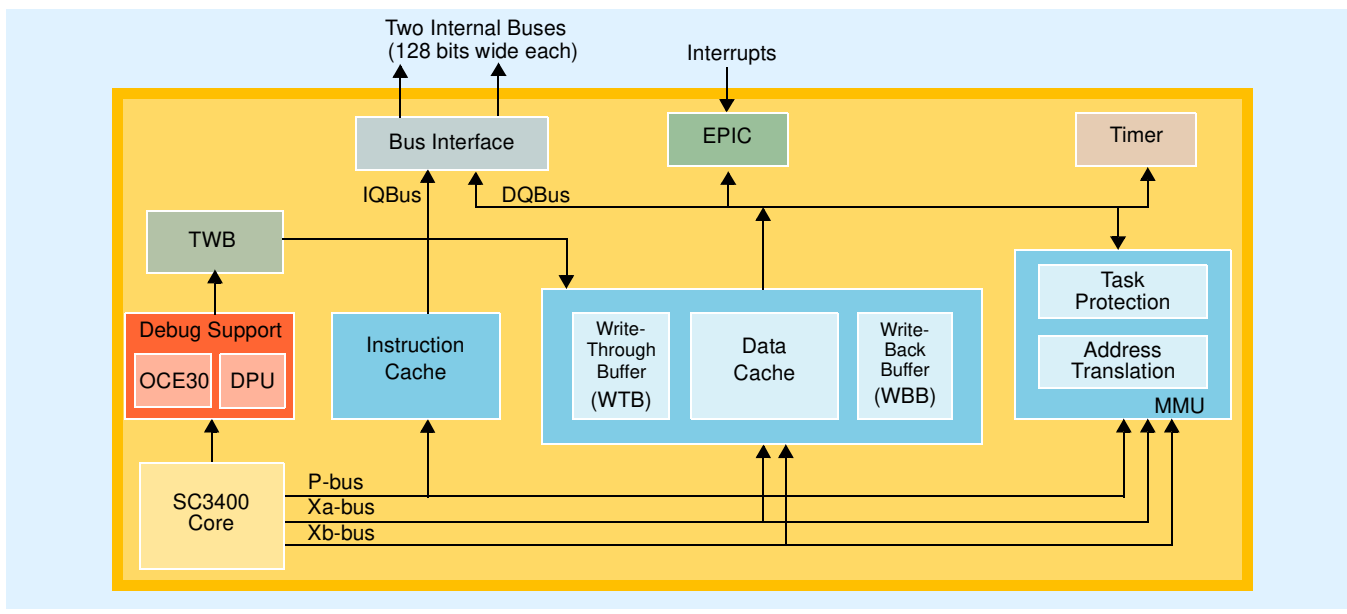


Figure 2. StarCore SC3400 DSP Core Subsystem Block Diagram

1 Pin Assignments and Reset States

This section includes diagrams of the MSC8144 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in [Figure 3](#) and [Figure 4](#) with their ball location index numbers.

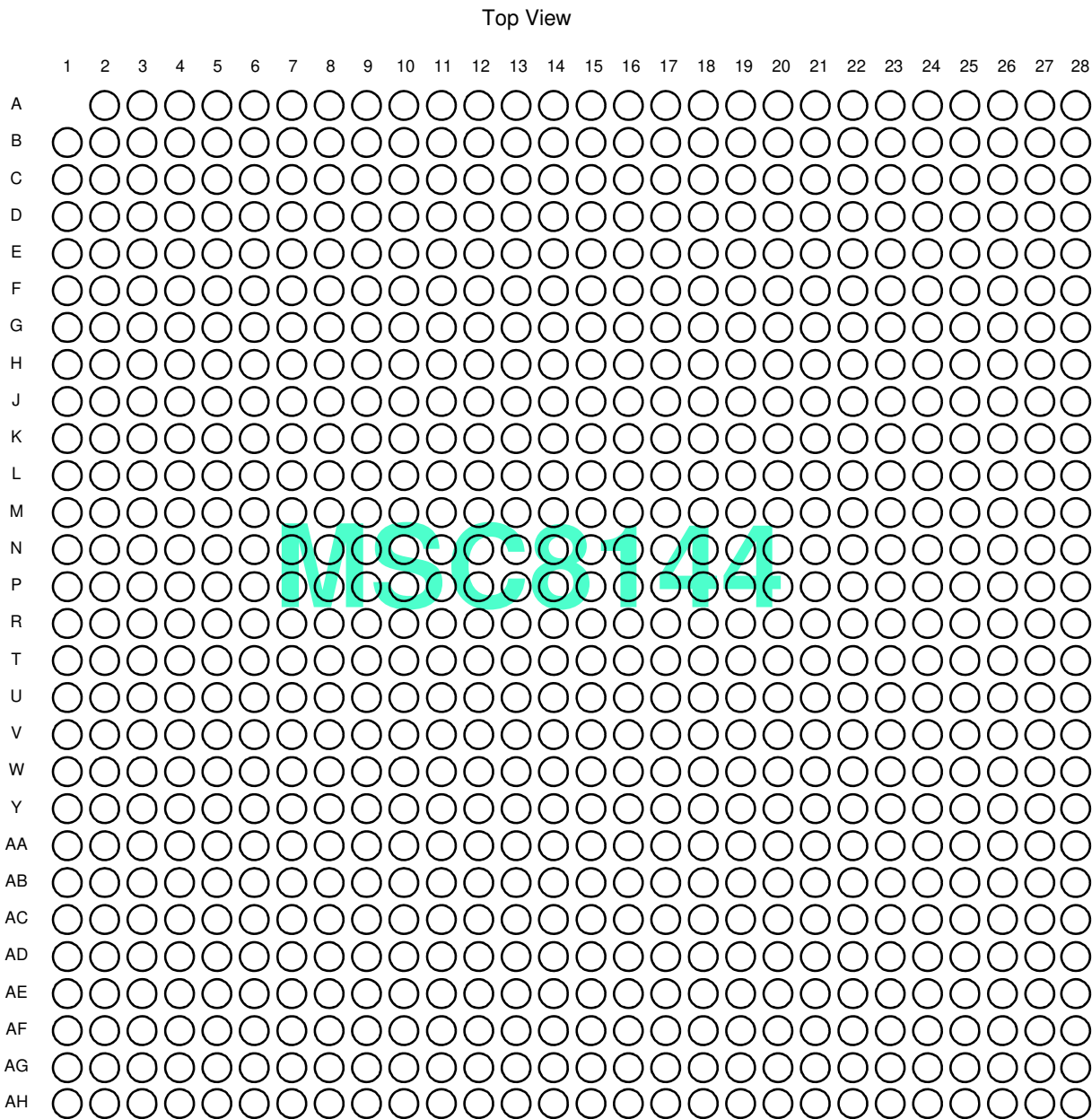


Figure 3. MSC8144 FC-PBGA Package, Top View

Bottom View

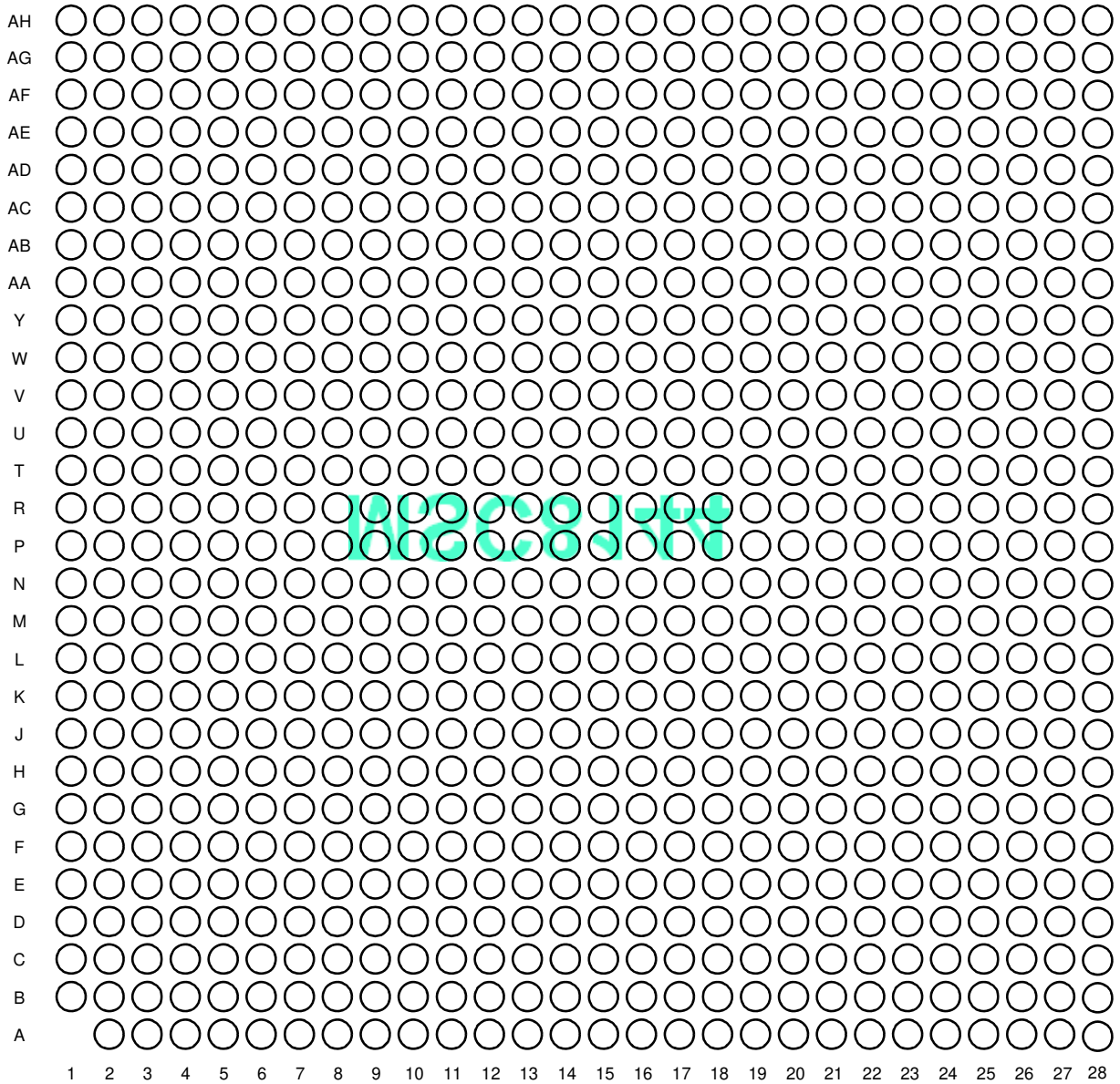


Figure 4. MSC8144 FC-PBGA Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}	
A4	V _{DDGE2}										V _{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}	
A6	GE2_TD0/PCI_CBE0		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}	
A7	SRIO_IMP_CAL_RX										V _{DDSDXC}
A8	Reserved ¹										—
A9	Reserved ¹										—
A10	Reserved ¹										—
A11	Reserved ¹										—
A12	SRIO_RXD0										V _{DDSDXC}
A13	V _{DDSDXC}										V _{DDSDXC}
A14	SRIO_RXD1										V _{DDSDXC}
A15	V _{DDSDXC}										V _{DDSDXC}
A16	SRIO_REF_CLK										V _{DDSDXC}
A17	V _{DDRIOPLL}										GND _{RIOPLL}
A18	GND _{SXC}										GND _{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DDSDXC}	
A20	V _{DDSDXC}										V _{DDSDXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DDSDXC}	
A22	V _{DDSDXC}										V _{DDSDXC}
A23	SRIO_IMP_CAL_TX										V _{DDSDXP}
A24	MDQ28										V _{DDDDR}
A25	MDQ29										V _{DDDDR}
A26	MDQ30										V _{DDDDR}
A27	MDQ31										V _{DDDDR}
A28	MDQS3										V _{DDDDR}
B1	Reserved ¹										—
B2	GE2_TD1/PCI_CBE1		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}	
B3	GE2_TX_EN/PCI_CBE2		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}	
B4	GE_MDIO		Ethernet							V _{DDGE2}	
B5	GND										GND
B6	GE_MDC		Ethernet							V _{DDGE2}	
B7	GND _{SXC}										GND _{SXC}
B8	Reserved ¹										—
B9	Reserved ¹										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
B10	Reserved ¹									—
B11	Reserved ¹									—
B12	SRIO_RXD0									V _{DD} SXC
B13	GND _{SXC}									GND _{SXC}
B14	SRIO_RXD1									V _{DD} SXC
B15	GND _{SXC}									GND _{SXC}
B16	SRIO_REF_CLK									V _{DD} SXC
B17	Reserved ¹									—
B18	V _{DD} SXC									V _{DD} SXC
B19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXC
B20	GND _{SXC}									GND _{SXC}
B21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXC
B22	GND _{SXC}									GND _{SXC}
B23	GND _{SXP}									GND _{SXP}
B24	MDQ27									V _{DD} DDR
B25	V _{DD} DDR									V _{DD} DDR
B26	GND									GND
B27	V _{DD} DDR									V _{DD} DDR
B28	MDQS3									V _{DD} DDR
C1	Reserved ¹									—
C2	GE2_RX_CLK/PCI_AD29		Ethernet 2			PCI	Ethernet 2			V _{DD} GE2
C3	V _{DD} GE2									V _{DD} GE2
C4	TDM7RSYN/GE2_TD2/ PCI_AD2/UTP_TER		TDM	PCI			Ethernet 2	UTOPIA	V _{DD} GE2	
C5	TDM7RCLK/GE2_RD2/ PCI_AD0/UTP_RVL		TDM	PCI			Ethernet 2	UTOPIA	V _{DD} GE2	
C6	V _{DD} GE2									V _{DD} GE2
C7	GE2_RD0/PCI_AD27		Ethernet 2			PCI	Ethernet 2			V _{DD} GE2
C8	Reserved ¹									—
C9	Reserved ¹									—
C10	Reserved ¹									—
C11	Reserved ¹									—
C12	V _{DD} SXP									V _{DD} SXP
C13	SRIO_TXD0									V _{DD} SXP
C14	V _{DD} SXP									V _{DD} SXP
C15	SRIO_TXD1									V _{DD} SXP
C16	GND _{SXC}									GND _{SXC}
C17	GND _{RIOPLL}									GND _{RIOPLL}
C18	Reserved ¹									—
C19	V _{DD} SXP									V _{DD} SXP
C20	SRIO_TXD2/GE1_SGMII_T X		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
C21	V _{DD} SXP										V _{DD} SXP
C22	SRIO_TXD3/GE2_SGMII_T X		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP	
C23	V _{DD} SXP										V _{DD} SXP
C24	MDQ26										V _{DD} DDR
C25	MDQ25										V _{DD} DDR
C26	MDM3										V _{DD} DDR
C27	GND										GND
C28	MDQ24										V _{DD} DDR
D1	Reserved ¹										—
D2	GE2_RD1/PCI_AD28		Ethernet 2			PCI	Ethernet 2			V _{DD} GE2	
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD		TDM		PCI		Ethernet 2		UTOPIA	V _{DD} GE2	
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA		TDM		PCI		Ethernet 2		UTOPIA	V _{DD} GE2	
D6	GE1_RD0/UTP_RD2/ PCI_CBE2		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DD} GE1
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER		TDM		PCI		Ethernet 2		UTOPIA	V _{DD} GE2	
D8	Reserved ¹										—
D9	Reserved ¹										—
D10	Reserved ¹										—
D11	Reserved ¹										—
D12	GND _{SXP}										GND _{SXP}
D13	SRIO_TXD0										V _{DD} SXP
D14	GND _{SXP}										GND _{SXP}
D15	SRIO_TXD1										V _{DD} SXP
D16	V _{DD} SXC										V _{DD} SXC
D17	Reserved ¹										—
D18	Reserved ¹										—
D19	GND _{SXP}										GND _{SXP}
D20	SRIO_TXD2/GE1_SGMII_T X		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP	
D21	GND _{SXP}										GND _{SXP}
D22	SRIO_TXD3/GE2_SGMII_T X		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP	
D23	GND _{SXP}										GND _{SXP}
D24	MDQ23										V _{DD} DDR
D25	V _{DD} DDR										V _{DD} DDR
D26	MDQ22										V _{DD} DDR
D27	MDQ21										V _{DD} DDR
D28	MDQS2										V _{DD} DDR
E1	Reserved ¹										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E6	V _{DDGE1}								V _{DDGE1}	
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E8	Reserved ¹								—	
E9	Reserved ¹								—	
E10	GND								GND	
E11	V _{DD}								V _{DD}	
E12	GND								GND	
E13	V _{DD}								V _{DD}	
E14	GND								GND	
E15	V _{DD}								V _{DD}	
E16	GND								GND	
E17	V _{DD}								V _{DD}	
E18	GND								GND	
E19	V _{DD}								V _{DD}	
E20	GND								GND	
E21	V _{DD}								V _{DD}	
E22	GND								GND	
E23	V _{DDDDR}								V _{DDDDR}	
E24	MDQ20								V _{DDDDR}	
E25	GND								GND	
E26	V _{DDDDR}								V _{DDDDR}	
E27	GND								GND	
E28	MDQS2								V _{DDDDR}	
F1	Reserved ¹								—	
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F3	V _{DDGE1}								V _{DDGE1}	
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F6	GND								GND	
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F8	V _{DDGE1}								V _{DDGE1}	
F9	GND								GND	

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
F10	V _{DD}									V _{DD}
F11	GND									GND
F12	V _{DD}									V _{DD}
F13	GND									GND
F14	V _{DD}									V _{DD}
F15	GND									GND
F16	V _{DD}									V _{DD}
F17	GND									GND
F18	V _{DD}									V _{DD}
F19	GND									GND
F20	V _{DD}									V _{DD}
F21	Reserved ¹									—
F22	V _{DDDDR}									V _{DDDDR}
F23	GND									GND
F24	MDQ19									V _{DDDDR}
F25	MDQ18									V _{DDDDR}
F26	MDM2									V _{DDDDR}
F27	MDQ17									V _{DDDDR}
F28	MDQ16									V _{DDDDR}
G1	Reserved ¹									—
G2	$\overline{\text{SRESET}}^4$									V _{DDIO}
G3	GND									GND
G4	$\overline{\text{PORESET}}^4$									V _{DDIO}
G5	GE1_COL/UTP_RD1		UTOPIA	Ethernet 1	UTOPIA		Ethernet 1	UTOPIA	V _{DDIO}	
G6	GE1_TD2/UTP_TD4/ PCI_AD29		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
G7	GE1_RX_DV/UTP_RD7		UTOPIA	Ethernet 1	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}	
G8	GE1_TX_ER/UTP_TD7/ PCI_CBE1		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
G9	V _{DD}									V _{DD}
G10	GND									GND
G11	V _{DD}									V _{DD}
G12	GND									GND
G13	V _{DD}									V _{DD}
G14	GND									GND
G15	V _{DD}									V _{DD}
G16	GND									GND
G17	V _{DD}									V _{DD}
G18	GND									GND
G19	V _{DD}									V _{DD}
G20	GND									GND
G21	Reserved ¹	—								—
G22	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
G23	MBA1									V _{DDDDR}
G24	MA3									V _{DDDDR}
G25	MA8									V _{DDDDR}
G26	V _{DDDDR}									V _{DDDDR}
G27	GND									GND
G28	$\overline{\text{MCK0}}$									V _{DDDDR}
H1	Reserved ¹									—
H2	CLKIN									V _{DDIO}
H3	$\overline{\text{HRESET}}$									V _{DDIO}
H4	PCI_CLK_IN									V _{DDIO}
H5	$\overline{\text{NMI}}$									V _{DDIO}
H6	URXD/GPIO14/ $\overline{\text{IRQ8}}$ / RC_LDF ^{3, 6}	$\overline{\text{RC_LDF}}$	UART/GPIO/IRQ							V _{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/ $\overline{\text{IRQ15}}$ ^{3, 6}		GPIO/ IRQ	Ethernet 1	PCI		GPIO/ IRQ	Ethernet 1		V _{DDIO}
H8	GE1_CRSS/PCI_AD5		PCI	Ethernet 1	PCI		Ethernet 1		V _{DDIO}	
H9	GND									GND
H10	V _{DD}									V _{DD}
H11	GND									GND
H12	V _{DD}									V _{DD}
H13	GND									GND
H14	V _{DD}									V _{DD}
H15	V _{DD}									V _{DD}
H16	V _{DD}									V _{DD}
H17	GND									GND
H18	V _{DD}									V _{DD}
H19	GND									GND
H20	V _{DD}									V _{DD}
H21	V _{DD}									V _{DD}
H22	V _{DDDDR}									V _{DDDDR}
H23	MBA0									V _{DDDDR}
H24	MA15									V _{DDDDR}
H25	V _{DDDDR}									V _{DDDDR}
H26	MA9									V _{DDDDR}
H27	MA7									V _{DDDDR}
H28	MCK0									V _{DDDDR}
J1	Reserved ¹									—
J2	GND									GND
J3	V _{DDIO}									V _{DDIO}
J4	STOP_BS									V _{DDIO}
J5	$\overline{\text{NMI_OUT}}$ ⁴									V _{DDIO}
J6	$\overline{\text{INT_OUT}}$ ⁴									V _{DDIO}
J7	SDA/GPIO27 ^{3, 4, 6}		I2C/GPIO							V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
J8	V _{DDIO}									V _{DDIO}
J9	V _{DD}									V _{DD}
J10	GND									GND
J11	V _{DD}									V _{DD}
J12	GND									GND
J13	V _{DD}									V _{DD}
J14	GND									GND
J15	GND									GND
J16	GND									GND
J17	V _{DD}									V _{DD}
J18	GND									GND
J19	V _{DD}									V _{DD}
J20	GND									GND
J21	GND									GND
J22	GND									GND
J23	GND									GND
J24	V _{DDDDR}									V _{DDDDR}
J25	GND									GND
J26	V _{DDDDR}									V _{DDDDR}
J27	GND									GND
J28	V _{DDDDR}									V _{DDDDR}
K1	Reserved ¹									—
K2	Reserved ¹									—
K3	Reserved ¹									—
K4	Reserved ¹									—
K5	V _{DDPLL2A}									V _{DDPLL2A}
K6	GND									GND
K7	V _{DDPLL0A}									V _{DDPLL0A}
K8	V _{DDPLL1A}									V _{DDPLL1A}
K9	V _{DD}									V _{DD}
K10	GND									GND
K11	V _{DD}									V _{DD}
K12	GND									GND
K13	V _{DD}									V _{DD}
K14	V _{DD}									V _{DD}
K15	V _{DD}									V _{DD}
K16	V _{DD}									V _{DD}
K17	V _{DD}									V _{DD}
K18	GND									GND
K19	V _{DD}									V _{DD}
K20	GND									GND
K21	V _{DD}									V _{DD}
K22	V _{DDDDR}									V _{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
K23	MBA2									V _{DDDDR}
K24	MA10									V _{DDDDR}
K25	MA12									V _{DDDDR}
K26	MA14									V _{DDDDR}
K27	MA4									V _{DDDDR}
K28	MV _{REF}									V _{DDDDR}
L1	Reserved ¹									—
L2	CLKOUT									V _{DDIO}
L3	TMR1/UTP_IR/PCI_CBE3/ GPIO17 ^{3, 6}		UTOPIA	TMR/ GPIO	UTOPIA	PCI	UTOPIA			V _{DDIO}
L4	TMR4/PCI_PAR/GPIO20 ^{3, 6} / UTP_REOP		TIMER/GPIO			PCI	TIMER/GPIO			V _{DDIO}
L5	GND									GND
L6	TMR2/PCI_FRAME/ GPIO18 ^{3, 6}		TIMER/GPIO			PCI	TIMER/GPIO	UTOPIA		V _{DDIO}
L7	SCL/GPIO26 ^{3, 4, 6}		I ² C/GPIO							V _{DDIO}
L8	UTXD/GPIO15/IRQ ^{3, 6}		UART/GPIO/IRQ							V _{DDIO}
L9	GND									GND
L10	V _{DD}									V _{DD}
L11	GND									GND
L12	V _{DD}									V _{DD}
L13	GND									GND
L14	V _{DD}									V _{DD}
L15	Reserved ¹									GND
L16	V _{DD}									V _{DD}
L17	GND									GND
L18	V _{DD}									V _{DD}
L19	GND									GND
L20	V _{DD}									V _{DD}
L21	GND									GND
L22	GND									GND
L23	MCKE1									V _{DDDDR}
L24	MA1									V _{DDDDR}
L25	V _{DDDDR}									V _{DDDDR}
L26	GND									GND
L27	V _{DDDDR}									V _{DDDDR}
L28	MCK1									V _{DDDDR}
M1	Reserved ¹									—
M2	TRST									V _{DDIO}
M3	EE0									V _{DDIO}
M4	EE1									V _{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA	PCI	UTOPIA				V _{DDIO}	
M6	UTP_RADDR0/PCI_AD7		UTOPIA	PCI	UTOPIA				V _{DDIO}	
M7	UTP_TD8/PCI_AD30		UTOPIA	PCI	UTOPIA				V _{DDIO}	

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
M8	V _{DDIO}									V _{DDIO}
M9	V _{DD}									V _{DD}
M10	GND									GND
M11	V _{DD}									V _{DD}
M12	GND									GND
M13	V _{DD}									V _{DD}
M14	GND									GND
M15	V _{DD}									V _{DD}
M16	GND									GND
M17	V _{DD}									V _{DD}
M18	GND									GND
M19	V _{DD}									V _{DD}
M20	GND									GND
M21	V _{DD}									V _{DD}
M22	V _{DDDDR}									V _{DDDDR}
M23	MCS1									V _{DDDDR}
M24	MA13									V _{DDDDR}
M25	MA2									V _{DDDDR}
M26	MA0									V _{DDDDR}
M27	GND									GND
M28	MCK1									V _{DDDDR}
N1	Reserved ¹									—
N2	V _{DDIO}									V _{DDIO}
N3	TMS									V _{DDIO}
N4	UTP_RD10/PCI_AD14 ⁵		UTOPIA	PCI	UTOPIA				V _{DDIO}	
N5	V _{DDIO}		Power						V _{DDIO}	
N6	UTP_RADDR1/PCI_AD8		UTOPIA	PCI	UTOPIA				V _{DDIO}	
N7	UTP_TD9/PCI_AD31		UTOPIA	PCI	UTOPIA				V _{DDIO}	
N8	TMR3/PCI_IRDY/GPIO19 ^{3,6} /UTP_TEOP		TIMER/GPIO			PCI	TIMER/GPIO	UTOPIA	V _{DDIO}	
N9	GND									GND
N10	V _{DDM3}									V _{DDM3}
N11	V _{DD}									V _{DD}
N12	V _{DDM3}									V _{DDM3}
N13	V _{DD}									V _{DD}
N14	V _{DDM3}									V _{DDM3}
N15	V _{DD}									V _{DD}
N16	V _{DDM3}									V _{DDM3}
N17	V _{DD}									V _{DD}
N18	V _{DDM3}									V _{DDM3}
N19	V _{DD}									V _{DD}
N20	V _{DDM3}									V _{DDM3}
N21	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
N22	GND										GND
N23	MODT1										V _{DDDDR}
N24	MCKE0										V _{DDDDR}
N25	V _{DDDDR}										V _{DDDDR}
N26	MA5										V _{DDDDR}
N27	MA6										V _{DDDDR}
N28	MA11										V _{DDDDR}
P1	Reserved ¹										—
P2	TDI ⁵										V _{DDIO}
P3	UTP_RD11/PCI_AD15		UTOPIA	PCI	UTOPIA						V _{DDIO}
P4	GND										GND
P5	UTP_RADDR3/PCI_AD10		UTOPIA	PCI	UTOPIA						V _{DDIO}
P6	UTP_RADDR2/PCI_AD9		UTOPIA	PCI	UTOPIA						V _{DDIO}
P7	PCI_GNT ³ /GPIO29/IRQ7 ^{3, 6}		GPIO/IRQ	PCI			GPIO/IRQ				V _{DDIO}
P8	PCI_STOP ⁶ /GPIO30/IRQ2 ^{3, 6}		GPIO/IRQ	PCI			GPIO/IRQ				V _{DDIO}
P9	GND										GND
P10	GND										GND
P11	V _{DDM3}										V _{DDM3}
P12	GND										GND
P13	V _{DDM3}										V _{DDM3}
P14	GND										GND
P15	V _{DDM3}										V _{DDM3}
P16	GND										GND
P17	V _{DDM3}										V _{DDM3}
P18	GND										GND
P19	V _{DDM3}										V _{DDM3}
P20	GND										GND
P21	GND										GND
P22	V _{DDDDR}										V _{DDDDR}
P23	MCS0										V _{DDDDR}
P24	MRAS										V _{DDDDR}
P25	GND										GND
P26	V _{DDDDR}										V _{DDDDR}
P27	GND										GND
P28	MCK2										V _{DDDDR}
R1	Reserved ¹										—
R2	TCK										V _{DDIO}
R3	TDO										V _{DDIO}
R4	UTP_RD12/PCI_AD16		UTOPIA	PCI	UTOPIA						V _{DDIO}
R5	UTP_RCLAV_PDRPA/PCI_AD12		UTOPIA	PCI	UTOPIA						V _{DDIO}
R6	UTP_RADDR4/PCI_AD11		UTOPIA	PCI	UTOPIA						V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
R7	V _{DDIO}									V _{DDIO}
R8	PCI_REQ		PCI							V _{DDIO}
R9	GND									GND
R10	GND									GND
R11	GND									GND
R12	GND									GND
R13	GND									GND
R14	GND									GND
R15	GND									GND
R16	GND									GND
R17	GND									GND
R18	GND									GND
R19	GND									GND
R20	GND									GND
R21	GND									GND
R22	GND									GND
R23	MODT0									V _{DDDDR}
R24	MDIC1									V _{DDDDR}
R25	MDIC0									V _{DDDDR}
R26	MCAS									V _{DDDDR}
R27	MWE									V _{DDDDR}
R28	MCK2									V _{DDDDR}
T1	Reserved ¹									—
T2	UTP_RPRTY/PCI_AD21		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T3	UTP_RD13/PCI_AD17		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T4	V _{DDIO}									V _{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T6	UTP_RD15/PCI_AD19		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T7	PCI_TRDY		PCI							V _{DDIO}
T8	PCI_DEVSEL/GPIO31/IRQ ^{3, 6}		GPIO/IRQ		PCI		GPIO/IRQ			V _{DDIO}
T9	GND									GND
T10	GND									GND
T11	GND									GND
T12	GND									GND
T13	GND									GND
T14	GND									GND
T15	GND									GND
T16	GND									GND
T17	GND									GND
T18	GND									GND
T19	GND									GND
T20	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
T21	GND									GND
T22	V _{DDDDR}									V _{DDDDR}
T23	GND									GND
T24	V _{DDDDR}									V _{DDDDR}
T25	GND									GND
T26	V _{DDDDR}									V _{DDDDR}
T27	GND									GND
T28	V _{DDDDR}									V _{DDDDR}
U1	Reserved ¹									—
U2	UTP_TCLK/PCI_AD29		UTOPIA	PCI	UTOPIA					V _{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA	PCI	UTOPIA					V _{DDIO}
U4	UTP_TADDR2		UTOPIA							V _{DDIO}
U5	GND									GND
U6	UTP_REN/PCI_AD20		UTOPIA	PCI	UTOPIA					V _{DDIO}
U7	PCI_AD26		PCI							V _{DDIO}
U8	PCI_AD25		PCI							V _{DDIO}
U9	Reserved ¹									V _{DDIO}
U10	V _{D_{DM3}}									V _{D_{DM3}}
U11	GND									GND
U12	V _{D_{DM3}}									V _{D_{DM3}}
U13	GND									GND
U14	V _{D_{DM3}}									V _{D_{DM3}}
U15	GND									GND
U16	V _{D_{DM3}}									V _{D_{DM3}}
U17	GND									GND
U18	V _{D_{DM3}}									V _{D_{DM3}}
U19	GND									GND
U20	V _{D_{DM3}}									V _{D_{DM3}}
U21	GND									GND
U22	GND									GND
U23	MDQ7									V _{DDDDR}
U24	MDQ3									V _{DDDDR}
U25	MDQ4									V _{DDDDR}
U26	MDQ5									V _{DDDDR}
U27	MDQ1									V _{DDDDR}
U28	MDQ0									V _{DDDDR}
V1	Reserved ¹									—
V2	UTP_TD10/PCI_CBE0		UTOPIA	PCI	UTOPIA					V _{DDIO}
V3	UTP_TADDR3		UTOPIA							V _{DDIO}
V4	UTP_TD1/PCI_PERR		UTOPIA	PCI	UTOPIA					V _{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA	PCI	UTOPIA					V _{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA	PCI	UTOPIA					V _{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA	PCI	UTOPIA					V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
V8	VDDIO									VDDIO
V9	Reserved ¹									VDDIO
V10	GND									GND
V11	VDDM3									VDDM3
V12	GND									GND
V13	VDDM3									VDDM3
V14	GND									GND
V15	VDDM3									VDDM3
V16	GND									GND
V17	VDDM3									VDDM3
V18	GND									GND
V19	VDDM3									VDDM3
V20	GND									GND
V21	GND									GND
V22	VDDDDR									VDDDDR
V23	MDQ2									VDDDDR
V24	VDDDDR									VDDDDR
V25	MDQ6									VDDDDR
V26	GND									GND
V27	VDDDDR									VDDDDR
V28	MDQS0									VDDDDR
W1	Reserved ¹									—
W2	UTP_TD12/PCI_CBE2		UTOPIA	PCI		UTOPIA				VDDIO
W3	UTP_TD11/PCI_CBE1		UTOPIA	PCI		UTOPIA				VDDIO
W4	VDDIO									VDDIO
W5	GND									GND
W6	UTP_TD15/PCI_IRDY		UTOPIA	PCI		UTOPIA				VDDIO
W7	UTP_TD0/PCI_SERR		UTOPIA	PCI		UTOPIA				VDDIO
W8	UTP_RSOC/PCI_AD22		UTOPIA	PCI		UTOPIA				VDDIO
W9	Reserved ¹									VDDIO
W10	VDDM3									VDDM3
W11	GND									GND
W12	V _{25M3}									V _{25M3}
W13	GND									GND
W14	VDDM3									VDDM3
W15	V _{25M3}									V _{25M3}
W16	VDDM3									VDDM3
W17	GND									GND
W18	V _{25M3}									V _{25M3}
W19	GND									GND
W20	VDDM3									VDDM3
W21	GND									GND
W22	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
W23	MDQ10									VDDDDR
W24	GND									GND
W25	MDQ11									VDDDDR
W26	MDM0									VDDDDR
W27	GND									GND
W28	MDQS0									VDDDDR
Y1	Reserved ¹									-
Y2	UTP_TD14/PCI_FRAME		UTOPIA	PCI	UTOPIA					VDDIO
Y3	TDM5TSYN/PCI_AD18/ GPIO12 ^{3, 6}		TDM/GPIO		PCI	TDM/GPIO				VDDIO
Y4	TDM5TCLK/PCI_AD16		TDM		PCI	TDM				VDDIO
Y5	TDM4RCLK/PCI_AD7		TDM		PCI	TDM				VDDIO
Y6	TDM4TSYN/PCI_AD12		TDM		PCI	TDM				VDDIO
Y7	UTP_TPRTY/RC14	RC14	UTOPIA							VDDIO
Y8	UTP_TEN/PCI_PAR		UTOPIA	PCI	UTOPIA				VDDIO	
Y9	Reserved ¹									VDDIO
Y10	GND									GND
Y11	VDDM3									VDDM3
Y12	GND									GND
Y13	VDDM3									VDDM3
Y14	GND									GND
Y15	VDDM3									VDDM3
Y16	GND									GND
Y17	VDDM3									VDDM3
Y18	GND									GND
Y19	VDDM3									VDDM3
Y20	GND									GND
Y21	GND									GND
Y22	VDDDDR									VDDDDR
Y23	MDQ13									VDDDDR
Y24	VDDDDR									VDDDDR
Y25	GND									GND
Y26	MDQ9									VDDDDR
Y27	VDDDDR									VDDDDR
Y28	MDQ8									VDDDDR
AA1	Reserved ¹									—
AA2	UTP_TD13/PCI_CBE3		UTOPIA	PCI	UTOPIA				VDDIO	
AA3	TDM5RSYN/PCI_AD15/ GPIO10 ^{3, 6}		TDM/GPIO		PCI	TDM/GPIO			VDDIO	
AA4	TDM5TDAT, AT/PCI_AD17/ GPIO11 ⁶		TDM/GPIO		PCI	TDM/GPIO			VDDIO	
AA5	TDM5RCLK/PCI_AD13/ GPIO28 ^{3, 6}		TDM/GPIO		PCI	TDM/GPIO			VDDIO	
AA6	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AA7	TDM4TCLK/PCI_AD10		TDM			PCI	TDM			V _{DDIO}
AA8	TDM4TDAT/PCI_AD11		TDM			PCI	TDM			V _{DDIO}
AA9	V _{DDIO}									V _{DDIO}
AA10	V _{DDM3}									V _{DDM3}
AA11	GND									GND
AA12	V _{DDM3}									V _{DDM3}
AA13	GND									GND
AA14	V _{DDM3}									V _{DDM3}
AA15	GND									GND
AA16	V _{DDM3}									V _{DDM3}
AA17	GND									GND
AA18	V _{DDM3}									V _{DDM3}
AA19	GND									GND
AA20	V _{DDM3}									V _{DDM3}
AA21	GND									GND
AA22	GND									GND
AA23	MDQ15									V _{DDDDR}
AA24	MDQ14									V _{DDDDR}
AA25	MDM1									V _{DDDDR}
AA26	MDQ12									V _{DDDDR}
AA27	MDQS ¹									V _{DDDDR}
AA28	MDQS1									V _{DDDDR}
AB1	Reserved ¹									-
AB2	UTP_TSOC/RC15	RC15	UTOPIA							V _{DDIO}
AB3	V _{DDIO}									V _{DDIO}
AB4	TDM6RDAT/PCI_AD20/ GPIO5/IRQ11 ^{3, 6}		TDM/GPIO/IRQ			PCI	TDM/GPIO/IRQ			V _{DDIO}
AB5	TDM5RDAT/PCI_AD14/ GPIO9 ^{3, 6}		TDM/GPIO			PCI	TDM/GPIO			V _{DDIO}
AB6	TDM6TSYN/PCI_AD24/ GPIO8/IRQ14 ^{3, 6}		TDM/GPIO/IRQ			PCI	TDM/GPIO/IRQ			V _{DDIO}
AB7	TDM6RCLK/PCI_AD19/ GPIO4/IRQ10 ^{3, 6}		TDM/GPIO/IRQ			PCI	TDM/GPIO/IRQ			V _{DDIO}
AB8	TDM4RSYN/PCI_AD9		TDM			PCI	TDM			V _{DDIO}
AB9	TDM4RDAT/PCI_AD8		TDM			PCI	TDM			V _{DDIO}
AB10	GND									GND
AB11	V _{DDM3}									V _{DDM3}
AB12	GND									GND
AB13	V _{DDM3}									V _{DDM3}
AB14	GND									GND
AB15	V _{DDM3}									V _{DDM3}
AB16	GND									GND
AB17	V _{DDM3}									V _{DDM3}
AB18	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AB19	V _{DDM3}									V _{DDM3}
AB20	GND									GND
AB21	GND									GND
AB22	V _{DDDDR}									V _{DDDDR}
AB23	MECC7									V _{DDDDR}
AB24	MECC1									V _{DDDDR}
AB25	MECC4									V _{DDDDR}
AB26	MECC5									V _{DDDDR}
AB27	MECC2									V _{DDDDR}
AB28	ECC_MDQS									V _{DDDDR}
AC1	Reserved ¹									—
AC2	UTP_RD9/RC13	RC13	UTOPIA							V _{DDIO}
AC3	UTP_RD8/RC12	RC12	UTOPIA							V _{DDIO}
AC4	TDM6TCLK/PCI_AD22		TDM		PCI		TDM			V _{DDIO}
AC5	TDM6RSYN/PCI_AD21/ GPIO6/IRQ12 ^{3,6}		TDM/GPIO/IRQ		PCI		TDM/GPIO/IRQ			V _{DDIO}
AC6	V _{DDIO}									V _{DDIO}
AC7	TDM3TSYN/RC11	RC11	TDM							V _{DDIO}
AC8	PCI_AD23/GPIO7/IRQ13/ TDM6TDAT ^{3,6} /UTP_RMOD		TDM/GPIO/IRQ		PCI		TDM/GPIO/IRQ		UTOPIA	V _{DDIO}
AC9	TDM7TSYN/PCI_AD4		TDM		PCI		reserved			V _{DDIO}
AC10	V _{DDM3IO}									V _{DDM3IO}
AC11	GND									GND
AC12	V _{DDM3}									V _{DDM3}
AC13	GND									GND
AC14	V _{DDM3}									V _{DDM3}
AC15	GND									GND
AC16	V _{DDM3}									V _{DDM3}
AC17	GND									GND
AC18	V _{DDM3}									V _{DDM3}
AC19	GND									GND
AC20	V _{DDM3IO}									V _{DDM3IO}
AC21	Reserved ¹									—
AC22	MECC6									V _{DDDDR}
AC23	MECC3									V _{DDDDR}
AC24	ECC_MDM									V _{DDDDR}
AC25	V _{DDDDR}									V _{DDDDR}
AC26	MECC0									V _{DDDDR}
AC27	V _{DDDDR}									V _{DDDDR}
AC28	ECC_MDQS									V _{DDDDR}
AD1	Reserved ¹									—
AD2	GPIO1 ^{3,6}		GPIO							V _{DDIO}
AD3	TMR0/GPIO13		TIMER/GPIO							V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AD4	GPIO2 ^{3, 6}		GPIO							V _{DDIO}
AD5	GND									GND
AD6	TDM1TCLK		TDM							V _{DDIO}
AD7	TDM3TDAT/RC10	RC10	TDM							V _{DDIO}
AD8	TDM3RSYN/RC9	RC9	TDM							V _{DDIO}
AD9	TDM3RDAT/RC8	RC8	TDM							V _{DDIO}
AD10	GND									GND
AD11	V _{25M3}									V _{25M3}
AD12	GND									GND
AD13	V _{DDM3}									V _{DDM3}
AD14	GND									GND
AD15	V _{25M3}									V _{25M3}
AD16	GND									GND
AD17	V _{DDM3}									V _{DDM3}
AD18	GND									GND
AD19	V _{25M3}									V _{25M3}
AD20	GND									GND
AD21	Reserved ¹									—
AD22	V _{DDDDR}									V _{DDDDR}
AD23	GND									GND
AD24	V _{DDDDR}									V _{DDDDR}
AD25	GND									GND
AD26	V _{DDDDR}									V _{DDDDR}
AD27	GND									GND
AD28	V _{DDDDR}									V _{DDDDR}
AE1	Reserved ¹									—
AE2	GPIO0 ^{3, 6}		GPIO							V _{DDIO}
AE3	GPIO3 ^{3, 6}		GPIO							V _{DDIO}
AE4	TDM1RCLK		TDM							V _{DDIO}
AE5	TDM1TSYN/RC3	RC3	TDM							V _{DDIO}
AE6	TDM1TDAT/RC2	RC2	TDM							V _{DDIO}
AE7	TDM1RSYN/RC1	RC1	TDM							V _{DDIO}
AE8	TDM3RCLK/RC16	RC16	TDM							V _{DDIO}
AE9	TDM3TCLK		TDM							V _{DDIO}
AE10	TDM2TDAT/RC6	RC6	TDM							V _{DDIO}
AE11	GPIO21/ $\overline{\text{IRQ1}}$ ^{3, 6} /SPICKL		GPIO/IRQ/SPI							V _{DDIO}
AE12	GND									GND
AE13	Reserved ¹									—
AE14	GND									GND
AE15	Reserved ¹									—
AE16	Reserved ¹									—
AE17	Reserved ¹									—
AE18	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AE19	GND									GND
AE20	V _{DDM3IO}									V _{DDM3IO}
AE21	Reserved ¹									—
AE22	GND									GND
AE23	GND									GND
AE24	GND									GND
AE25	V _{DDDDR}									V _{DDDDR}
AE26	GND									GND
AE27	V _{DDDDR}									V _{DDDDR}
AE28	GND									GND
AF1	Reserved ¹									—
AF2	V _{DDIO}									V _{DDIO}
AF3	GND									GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM							V _{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM							V _{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM							V _{DDIO}
AF7	V _{DDIO}									V _{DDIO}
AF8	GND									GND
AF9	TDM2RDAT/RC4	RC4	TDM							V _{DDIO}
AF10	TDM2TCLK		TDM							V _{DDIO}
AF11	GPIO22/ $\overline{\text{IRQ}}4^{3, 6}$ /SPIMOSI		GPIO/IRQ/SPI							V _{DDIO}
AF12	GND									GND
AF13	GND									GND
AF14	V _{DDM3IO}									V _{DDM3IO}
AF15	GND									GND
AF16	GND									GND
AF17	Reserved ¹									—
AF18	V _{DDM3IO}									V _{DDM3IO}
AF19	GND									GND
AF20	Reserved ¹									—
AF21	Reserved ¹									—
AF22	$\overline{\text{M3_RESET}}$									V _{DDM3IO}
AF23	GND									GND
AF24	V _{DDDDR}									V _{DDDDR}
AF25	GND									GND
AF26	V _{DDDDR}									V _{DDDDR}
AF27	GND									GND
AF28	V _{DDDDR}									V _{DDDDR}
AG1	Reserved ¹									—
AG2	GPIO16/ $\overline{\text{IRQ}}0^{3, 6}$		GPIO/IRQ							V _{DDIO}
AG3	TDM0TCLK		TDM							V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AG4	TDM0RSYN/RCW_SRC0	RCW_SRC0	TDM							V _{DDIO}
AG5	TDM0RCLK		TDM							V _{DDIO}
AG6	TDM0TDAT/RCW_SRC1	RCW_SRC1	TDM							V _{DDIO}
AG7	TDM2TSYN/RC7	RC7	TDM							V _{DDIO}
AG8	TDM2RCLK		TDM							V _{DDIO}
AG9	TDM2RSYN/RC5	RC5	TDM							V _{DDIO}
AG10	GPIO24/IRQ6 ^{3, 6} /SPISEL		GPIO/IRQ/SPI							V _{DDIO}
AG11	GPIO23/IRQ5 ^{3, 6} /SPIMISO		GPIO/IRQ/SPI							V _{DDIO}
AG12	Reserved ¹									—
AG13	GND									GND
AG14	GND									GND
AG15	GND									GND
AG16	GND									GND
AG17	Reserved ¹									—
AG18	Reserved ¹									—
AG19	GND									GND
AG20	GND									GND
AG21	V _{DDM3IO}									V _{DDM3IO}
AG22	GND									GND
AG23	GND									GND
AG24	GND									GND
AG25	V _{DDDDR}									V _{DDDDR}
AG26	GND									GND
AG27	V _{DDDDR}									V _{DDDDR}
AG28	GND									GND
AH1	Reserved ¹									—
AH2	Reserved ¹									—
AH3	Reserved ¹									—
AH4	Reserved ¹									—
AH5	Reserved ¹									—
AH6	Reserved ¹									—
AH7	Reserved ¹									—
AH8	Reserved ¹									—
AH9	Reserved ¹									—
AH10	Reserved ¹									—
AH11	Reserved ¹									—
AH12	Reserved ¹									—
AH13	Reserved ¹									—
AH14	Reserved ¹									—
AH15	Reserved ¹									—
AH16	Reserved ¹									—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
AH17	Reserved ¹										—
AH18	Reserved ¹										—
AH19	Reserved ¹										—
AH20	Reserved ¹										—
AH21	Reserved ¹										—
AH22	Reserved ¹										—
AH23	Reserved ¹										—
AH24	Reserved ¹										—
AH25	Reserved ¹										—
AH26	Reserved ¹										—
AH27	Reserved ¹										—
AH28	Reserved ¹										—

Notes:

- Reserved signals should be disconnected for compatibility with future revisions of the device.
- For signals with same functionality in all modes the appropriate cells are empty.
- The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23, GPIO** in the *MSC8144 Reference Manual*.
- Open-drain signal.
- Internal 20 K Ω pull-up resistor.
- For signals with GPIO functionality, the open-drain and internal 20 K Ω pull-up resistor can be configured by GPIO register programming. See **Chapter 23, GPIO** of the *MSC8144 Reference Manual* for configuration details.