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Technical Data

MPC8241 Integrated Processor Hardware Specifications

The MPC8241 combines a PowerPC™ MPC603E core with a PCI bridge so that system designers can rapidly design systems using peripherals designed for PCI and other standard interfaces. Also, a high-performance memory controller supports various types of ROM and SDRAM. The MPC8241 is the second of a family of products that provide system-level support for industry-standard interfaces with an MPC603e processor core.

This hardware specification describes pertinent electrical and physical characteristics of the MPC8241, which is based on the MPC8245 design. For functional characteristics of the processor, refer to the *MPC8245 Integrated Processor Reference Manual* (MPC8245UM).

For published errata or updates to this document, visit the web site listed on the back cover of the document.

Contents

1 Overview

The MPC8241 integrated processor is composed of a peripheral logic block and a 32-bit superscalar MPC603e core, as shown in Figure 1.
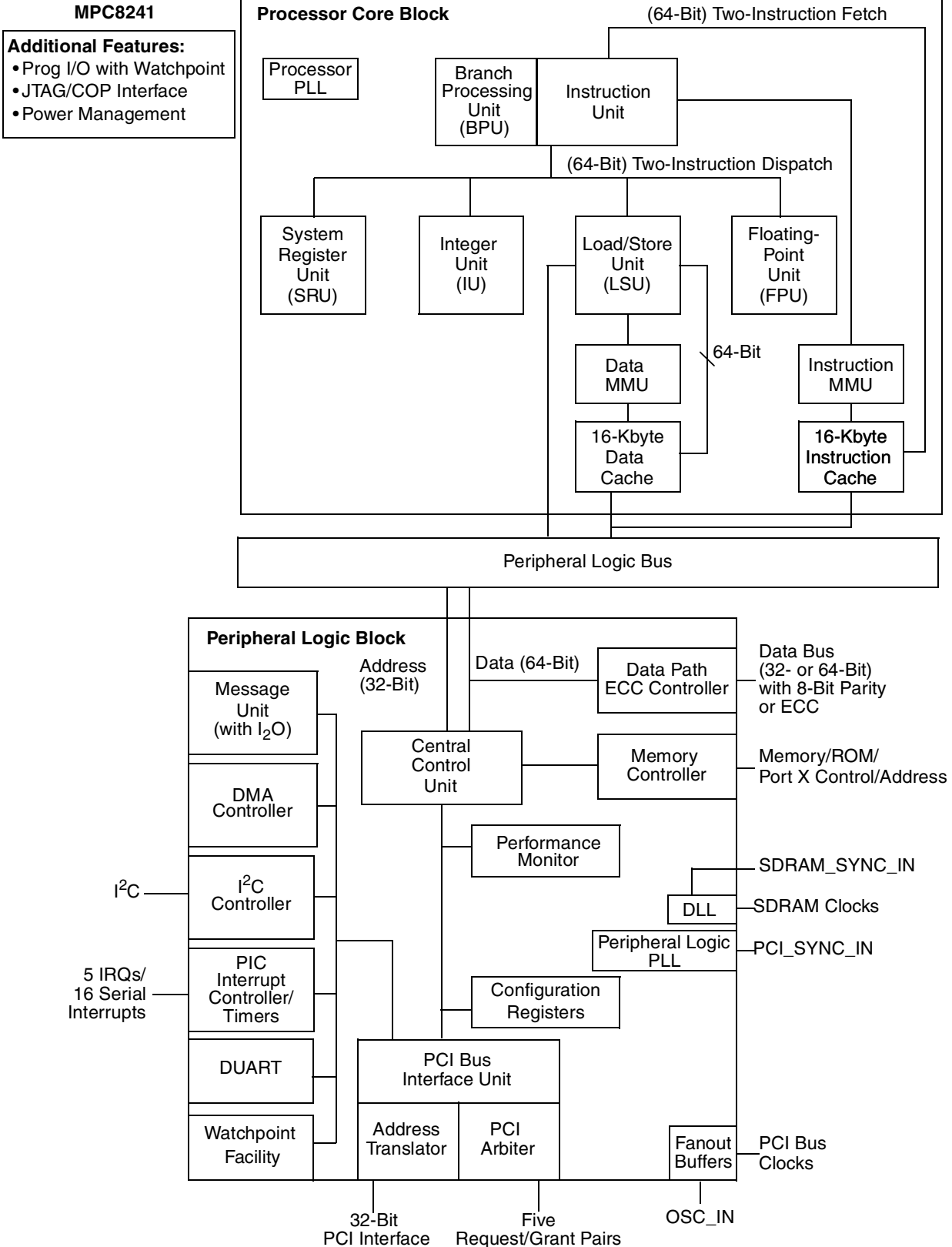
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Figure 1. MPC8241 Block Diagram

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I$_2$O interface), and an I^{2}C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL, allowing the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8241 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8241 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8241 are as follows:

- Processor core
  - High-performance, superscalar processor core
  - Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
  - 16-Kbyte instruction cache
  - 16-Kbyte data cache
  - Lockable L1 caches—entire cache or on a per-way basis up to three of four ways
  - Dynamic power management—supports 60x nap, doze, and sleep modes
- Peripheral logic
  - Peripheral logic bus
    - Various operating frequencies and bus divider ratios
    - 32-bit address bus, 64-bit data bus
    - Full memory coherency
    - Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - Store gathering on peripheral logic bus-to-PCI writes
  - Memory interface
    - Up to 2 Gbytes of SDRAM memory
    - High-bandwidth data bus (32- or 64-bit) to SDRAM
    - Programmable timing for SDRAM
    - One to 8 banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

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- – Write buffering for PCI and processor accesses
- – Normal parity, read-modify-write (RMW), or ECC
- – Data-path buffering between memory interface and processor
- – Low-voltage TTL logic (LVTTL) interfaces
- – 272 Mbytes of base and extended ROM/Flash/PortX space
- – Base ROM space for 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- – Extended ROM space for 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- – PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects

— 32-bit PCI interface

- – Operates up to 66 MHz
- – PCI 2.2-compatible
- – PCI 5.0-V tolerance
- – Dual address cycle (DAC) for 64-bit PCI addressing (master only)
- – PCI locked accesses to memory
- – Accesses to PCI memory, I/O, and configuration spaces
- – Selectable big- or little endian operation
- – Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- – Memory prefetching of PCI read accesses
- – Selectable hardware-enforced coherency
- – PCI bus arbitration unit (five request/grant pairs)
- – PCI agent mode capability
- – Address translation with two inbound and outbound units (ATU)
- – Internal configuration registers accessible from PCI

— Two-channel integrated DMA controller (writes to ROM/PortX not supported)

- – Direct mode or chaining mode (automatic linking of DMA transfers)
- – Scatter gathering—read or write discontinuous memory
- – 64-byte transfer queue per channel
- – Interrupt on completed segment, chain, and error
- – Local-to-local memory
- – PCI-to-PCI memory
- – Local-to-PCI memory
- – PCI memory-to-local memory

— Message unit

- – Two doorbell registers
- – Two inbound and two outbound messaging registers
- – I$_2$O message interface

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- — I^{2}C controller with full master/slave support that accepts broadcast messages
- — Programmable interrupt controller (PIC)
  - – Five hardware interrupts (IRQs) or 16 serial interrupts
  - – Four programmable timers with cascade
- — Two (dual) universal asynchronous receiver/transmitters (UARTs)
- — Integrated PCI bus and SDRAM clock generation
- — Programmable PCI bus and memory interface output drivers
- System level performance monitor facility
- Debug features
  - — Memory attribute and PCI attribute signals
  - — Debug address signals
  - — $\overline{\text{MIV}}$ signal—marks valid address and data bus cycles on the memory bus
  - — Programmable input and output signals with watchpoint capability
  - — Error injection/capture on data path
  - — IEEE Std. 1149.1 (JTAG)/test interface

3   General Parameters

The following list summarizes the general parameters of the MPC8241:

Technology	0.25 µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully static
Packages	Surface-mount 357 (thick substrate and thick mold cap) plastic ball grid array (PBGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 2 for details and recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8241.

4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other characteristics.

4.1.1 Absolute Maximum Ratings

This section describes the MPC8241 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	−0.3 to 2.1	V
Supply voltage—memory bus drivers, PCI and standard I/O buffers	$GV_{DD\_}OV_{DD}$	−0.3 to 3.6	V
Supply voltage—PLLs	$AV_{DD}/AV_{DD}2$	−0.3 to 2.1	V
Supply voltage—PCI reference	LV_{DD}	−0.3 to 5.4	V
Input voltage [2]	V_{in}	−0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105	•C
Storage temperature range	T_{stg}	−55 to 150	•C

Notes:

1. Table 2 provides functional and tested operating conditions. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	1.8 ± 100 mV	V	2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers		$GV_{DD\_}OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage		AV_{DD}	1.8 ± 100 mV		2
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8 ± 100 mV	V	2
PCI reference		LV_{DD}	5.0 ± 5%	V	4, 5, 6
			3.3 ± 0.3	V	5, 6, 7
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	•C	

Notes:

1. Freescale has tested these operating conditions and recommends them. Proper device operation outside of these conditions is not guaranteed.
2. **Caution:** $GV_{DD\_}OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD\_}OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD\_}OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD\_}OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD\_}OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

Figure 2 shows supply voltage sequencing and separation cautions.
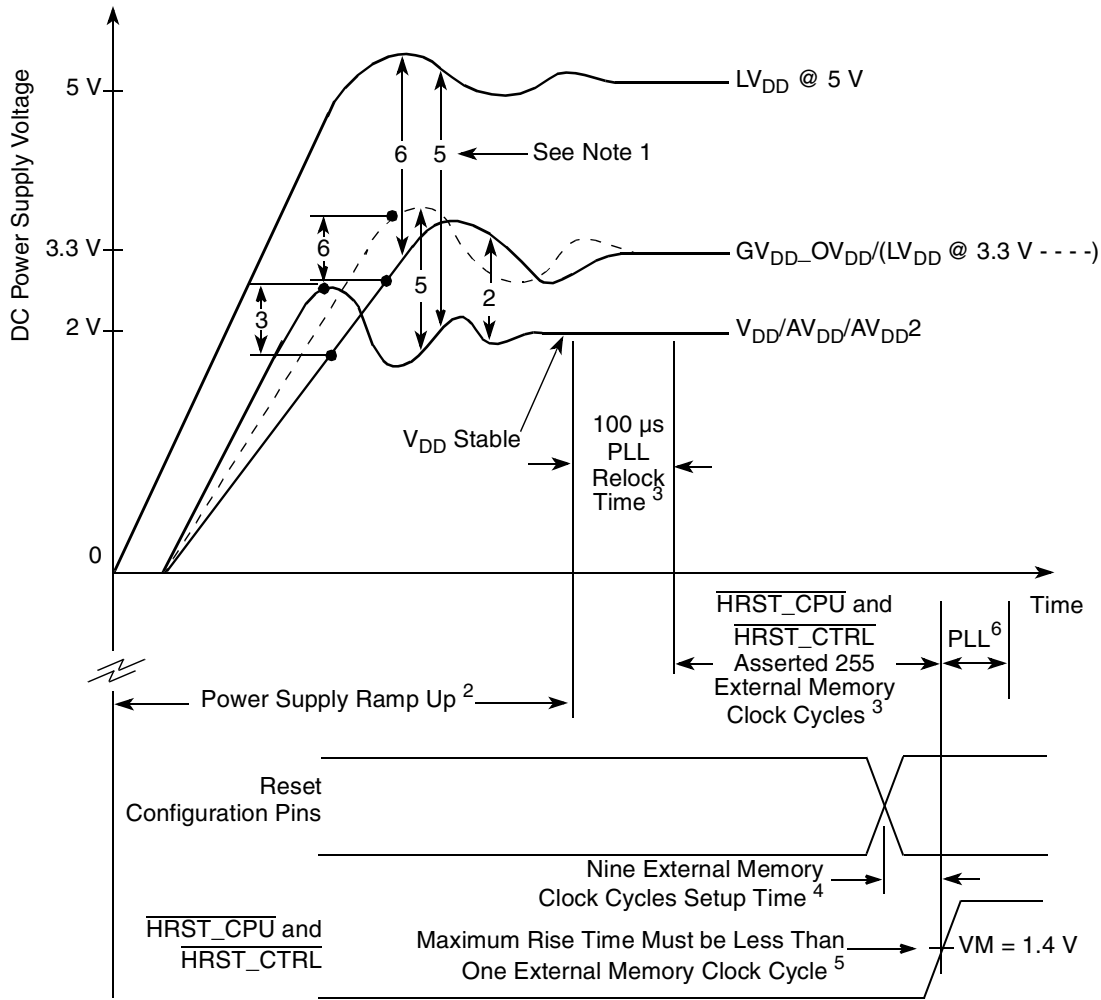
Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. Refer to Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for details on reset configuration pin setup timing requirements.
5. $\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{HRST\_CTRL}$ and $\overline{HRST\_CPU}$ negate in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the memory interface.
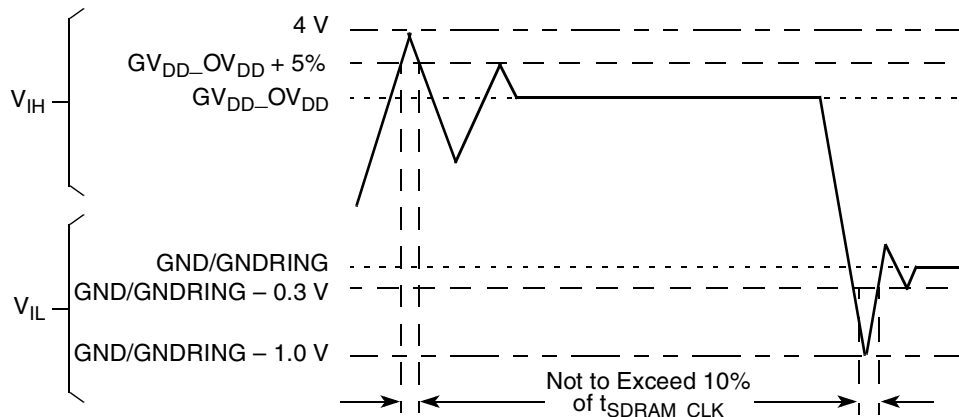

Figure 3. Overshoot/Undershoot Voltage

Figure 4 and Figure 5 show the undershoot and overshoot voltage of the PCI interface for the 3.3- and 5-V signals, respectively.
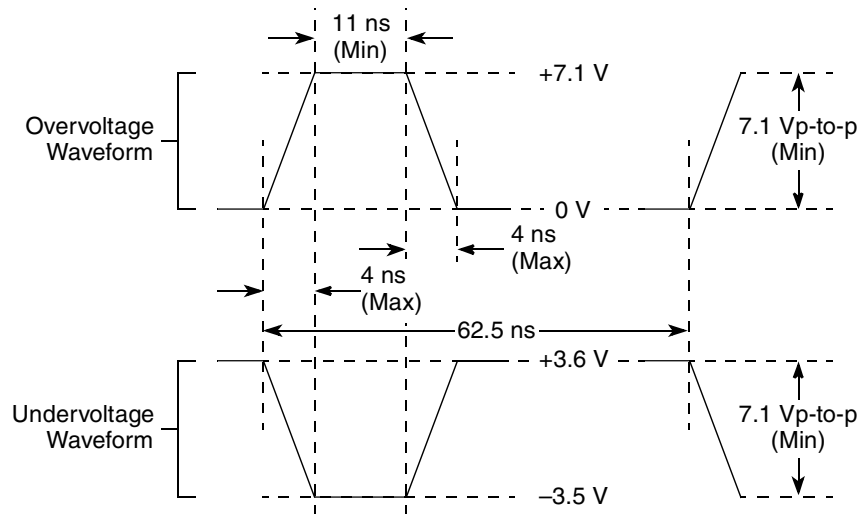

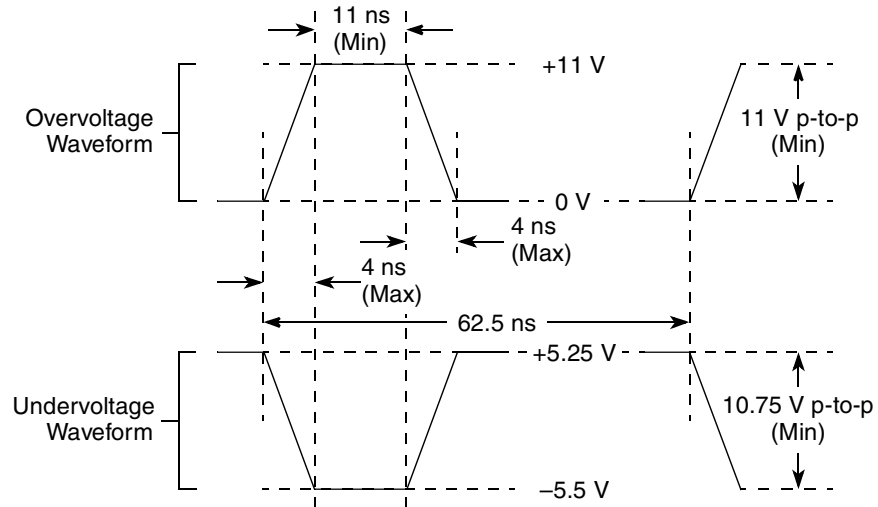**Figure 4. Maximum AC Waveforms for 3.3-V Signaling**

Figure 5. Maximum AC Waveforms for 5-V Signaling

4.2 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8241 at recommended operating conditions.

Table 3. DC Electrical Specifications

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Input high voltage	PCI only, except PCI_SYNC_IN	V_{IH}	$0.65 \times GV_{DD}\_OV_{DD}$	LV_{DD}	V	1
Input low voltage	PCI only, except PCI_SYNC_IN	V_{IL}	—	$0.3 \times GV_{DD}\_OV_{DD}$	V	
Input high voltage	All other pins, including PCI_SYNC_IN ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{IH}	2.0	3.3	V	
Input low voltage	All inputs, including PCI_SYNC_IN	V_{IL}	GND/GNDRING	0.8	V	2
Input leakage current for pins using DRV_PCI driver	$0.5\ V \le V_{in} \le 2.7\ V$ @ LV_{DD} = 4.75 V	I_L	—	±70	µA	3
Input leakage current all others	LV_{DD} = 3.6 V $GV_{DD}\_OV_{DD} \le 3.465\ V$	I_L	—	±10	µA	3
Output high voltage	I_{OH} = driver dependent ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{OH}	2.4	—	V	4
Output low voltage	I_{OL} = driver dependent ($GV_{DD}\_OV_{DD}$ = 3.3 V)	V_{OL}	—	0.4	V	4

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Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:

1. See Table 16 for pins with internal pull-up resistors.

2. All grounded pins are connected together.

3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal $GV_{DD}\_OV_{DD}/LV_{DD}$ and V_{DD} or both $GV_{DD}\_OV_{DD}/LV_{DD}$ and V_{DD} must vary in the same direction.

4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	$GV_{DD}\_OV_{DD}$ = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:

1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × $GV_{DD}\_OV_{DD}$ ($GV_{DD}\_OV_{DD}$ = 3.3 V) where table entry voltage = $GV_{DD}\_OV_{DD}$ – PCI V_{OH}.

2. For all others with $GV_{DD}\_OV_{DD}$ = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = $GV_{DD}\_OV_{DD}$ – V_{OH}.

3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × $GV_{DD}\_OV_{DD}$ ($GV_{DD}\_OV_{DD}$ = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.

4. For all others with $GV_{DD}\_OV_{DD}$ = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.

5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.

6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

4.3 Power Characteristics

Table 5 provides preliminary estimated power consumption data for the MPC8241.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)							Unit	Notes
	33/66/133	33/66/166	33/66/200	33/100/200	66/100/200	66/66/ 266	66/133/ 266		
Typical	0.7	0.8	1.0	1.0	1.0	1.5	1.8	W	1, 5
Max—CFP	0.8	1.0	1.2	1.3	1.3	1.9	2.1	W	1, 2
Max—INT	0.8	0.9	1.0	1.2	1.2	1.6	1.8	W	1, 3
Doze	0.5	0.6	0.7	0.8	0.8	1.0	1.3	W	1, 4, 6
Nap	0.2	0.2	0.3	0.4	0.4	0.4	0.7	W	1, 4, 6
Sleep	0.2	0.2	0.2	0.2	0.3	0.2	0.4	W	1, 4, 6
I/O Power Supplies [7]									
Mode	Minimum			Maximum				Unit	Notes
$GV_{DD}\_OV_{DD}$	500			1130				mW	8

Notes:

1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power.

2. Maximum—FP power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.

3. Maximum—INT power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.

4. Power saving mode maximums are measured at V_{DD} = 1.9 V while the device is in doze, nap, or sleep mode.

5. Typical power is measured at V_{DD} = AV_{DD} = 1.8 V, $GV_{DD}\_OV_{DD}$ = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.

6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.

7. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW, guaranteed by design, but not tested.

8. The typical maximum $GV_{DD}\_OV_{DD}$ value resulted from the MPC8241 operating at the fastest frequency combination of 66:133:266 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory and on 64-bit boundaries to local memory.

4.4   Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8241. For details, see Section 7.7, "Thermal Management."

Table 6. Thermal Characterization Data

Rating	Thermal Test Board Description	Symbol	Value [7] (166- and 200-MHz Parts)	Value [7] (266-MHz Part)	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	38	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JMA}$	25	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	31	22	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	22	17	°C/W	1, 3
Junction-to-board (bottom)	Four-layer board (2s2p)	$R_{\theta JB}$	17	11	°C/W	4
Junction-to-case (top)	Single-layer board (1s)	$R_{\theta JC}$	8	7	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	2	°C/W	6

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2. Per SEMI G38-87 and EIA/JESD51-2 with the board horizontal.

3. Per EIA/JESD51-6 with the board horizontal.

4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.

7. Note that the 166- and 200-MHz parts are in a two-layer package and the 266-MHz part is in a four-layer package, which causes the two package types to have different thermal characterization data.

4.5   AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 8, "Ordering Information."

Table 7 provides the operating frequency information for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V.

Table 7. Operating Frequency

Characteristic	166 MHz		200 MHz		266 MHz		Unit
	$V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 ± 100 mV						
	Min	Max	Min	Max	Min	Max	
Processor frequency (CPU)	100	166	100	200	100	266	MHz
Memory bus frequency	33	83	33	100	33	133	MHz
PCI input frequency	25–66						MHz

Caution: The PCI_SYNC_IN frequency and PLL_CFG[0:4] settings must be chosen such that the resulting peripheral logic/memory bus frequency and CPU (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 6, "PLL Configuration," for valid PLL_CFG[0:4] settings and PCI_SYNC_IN frequencies.

4.5.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications at recommended operating conditions, as defined in Section 4.5.2, "Input AC Timing Specifications." These specifications are for the default driver strengths indicated in Table 4. Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
1	Frequency of operation (PCI_SYNC_IN)	25	66	MHz	
2, 3	PCI_SYNC_IN rise and fall times	—	2.0	ns	1
4	PCI_SYNC_IN duty cycle measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN pulse width high measured at 1.4 V	6	9	ns	2
5b	PCI_SYNC_IN pulse width low measured at 1.4 V	6	9	ns	2
7	PCI_SYNC_IN jitter	—	200	ps	
8a	PCI_CLK[0:4] skew (pin-to-pin)	—	250	ps	
8b	SDRAM_CLK[0:3] skew (pin-to-pin)	—	190	ps	3
10	Internal PLL relock time	—	100	µs	2, 4, 5
15	DLL lock range with DLL_EXTEND = 0 (disabled) and normal tap delay; (default DLL mode)	See Figure 7		ns	6
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	

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Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 through 2.4 V.

2. Specification value at maximum frequency of operation.

3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.

4. Relock time is guaranteed by design and characterization. Relock time is not tested.

5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.

6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines,* for details on MPC8241 memory clock design.

7. Rise and fall times for the OSC_IN input are guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram, and Figure 7 through Figure 10 show the DLL locking range loop delay versus frequency of operation.
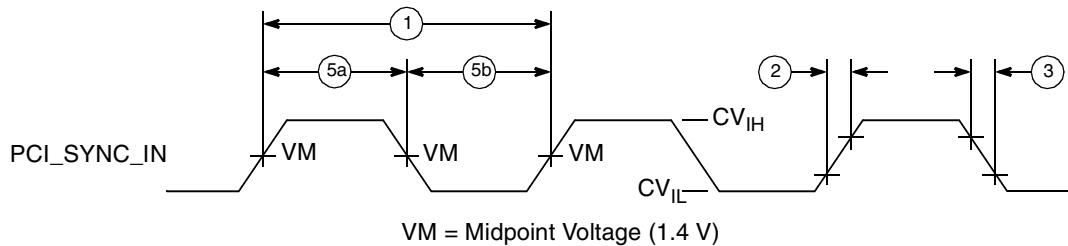
Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL if the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Keeping a DLL mode locked below tap point decimal 12 is not recommended.
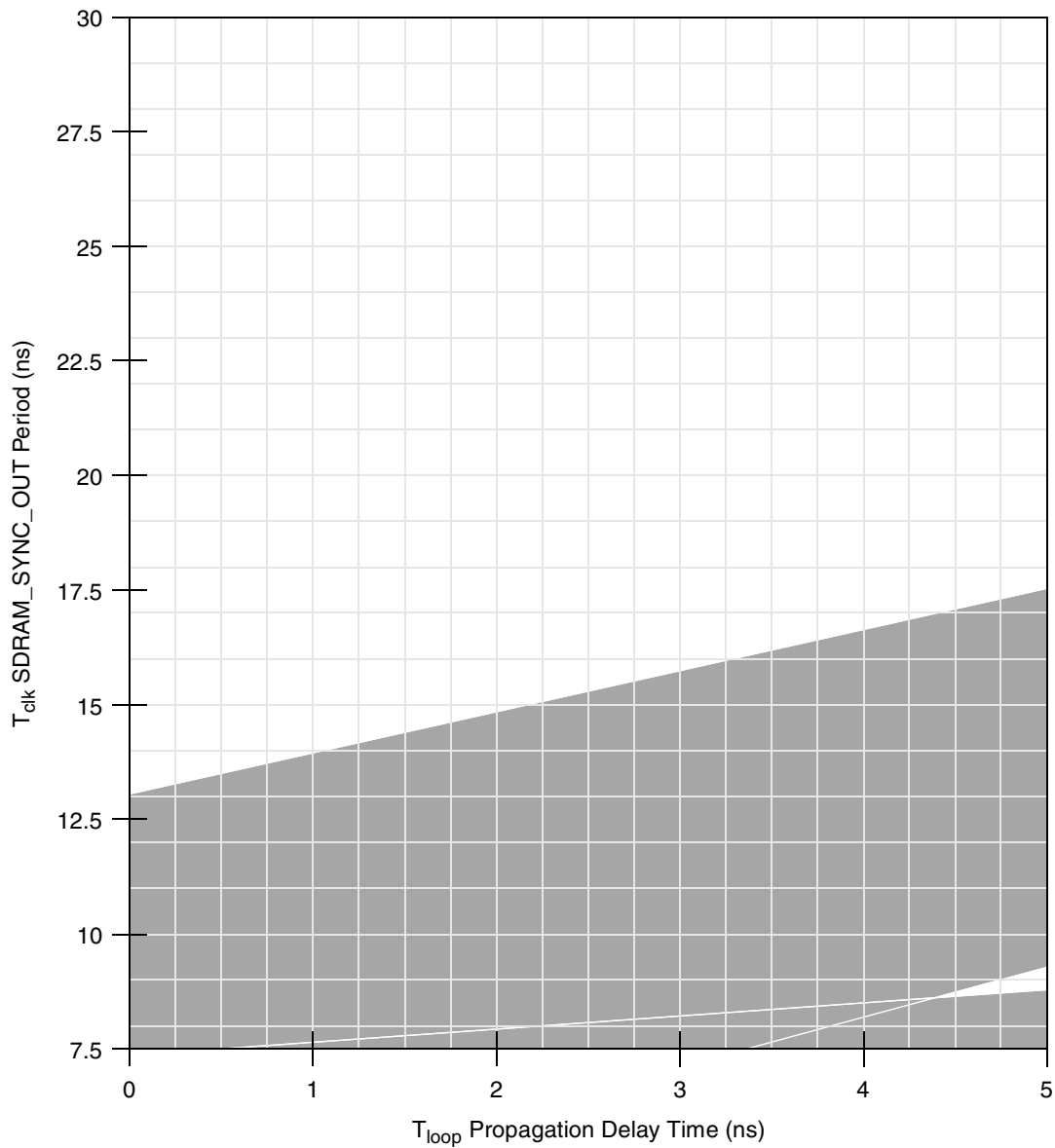
Figure 7. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Normal Tap Delay
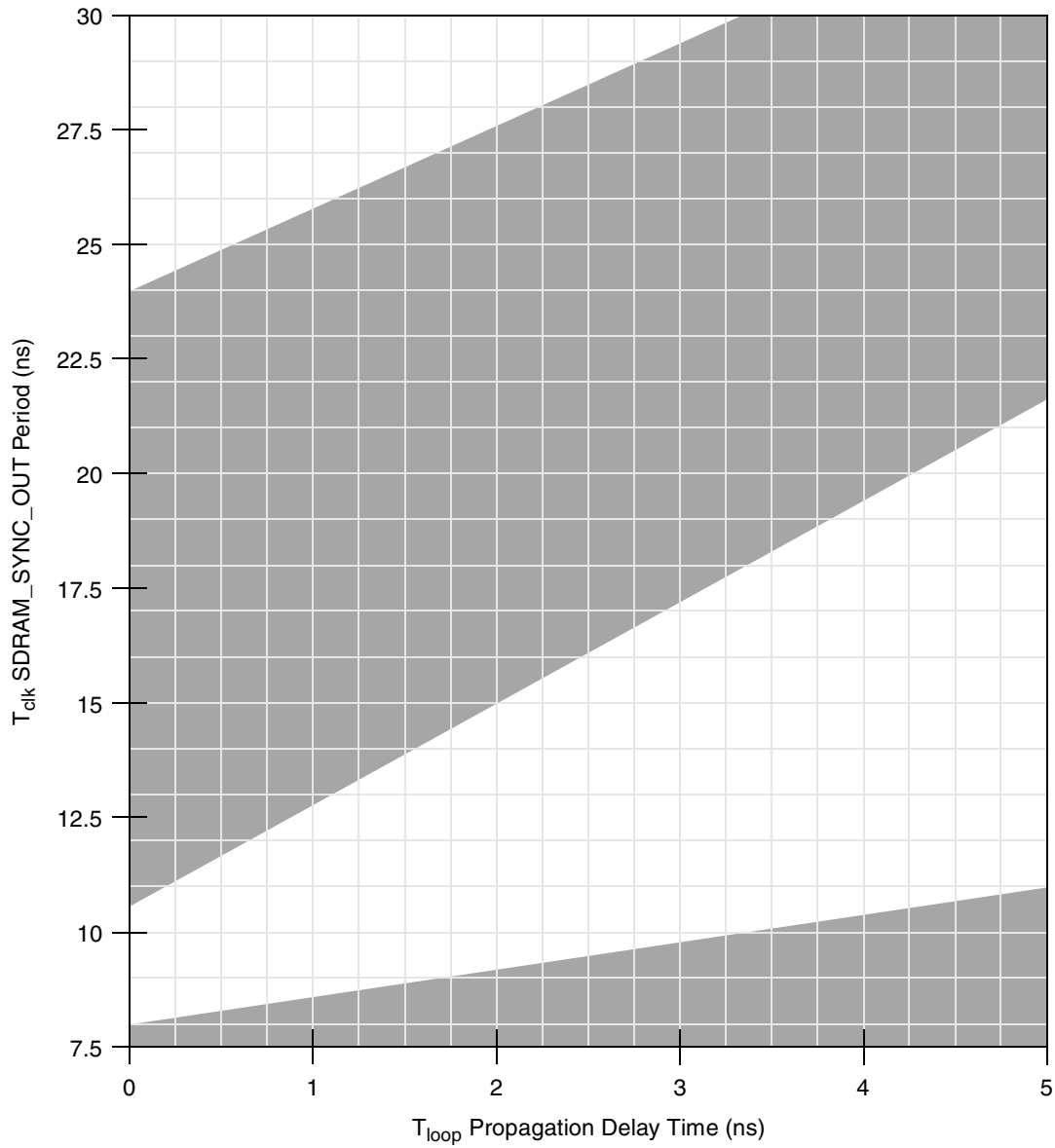
Figure 8. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay
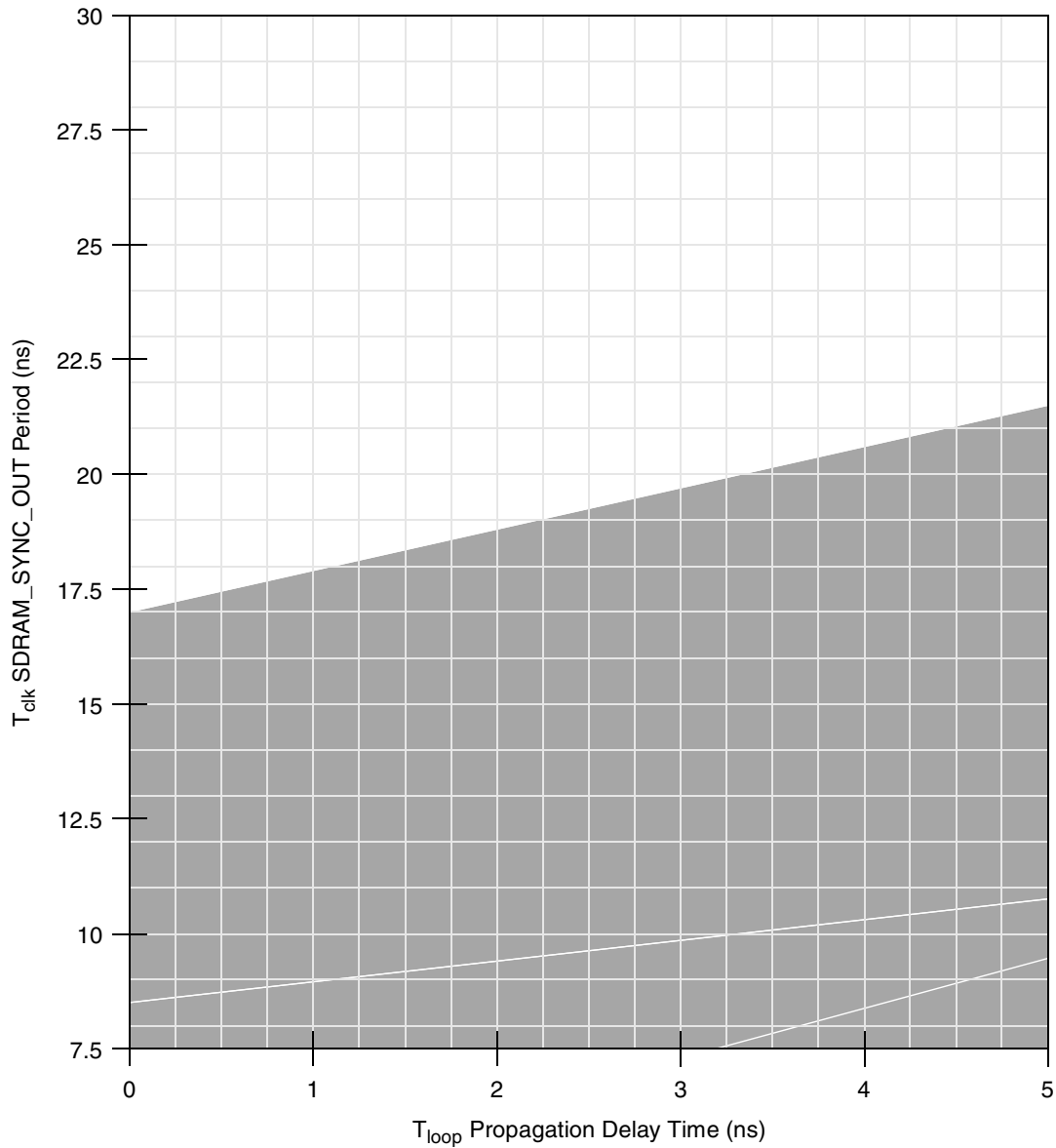
Figure 9. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Max Tap Delay
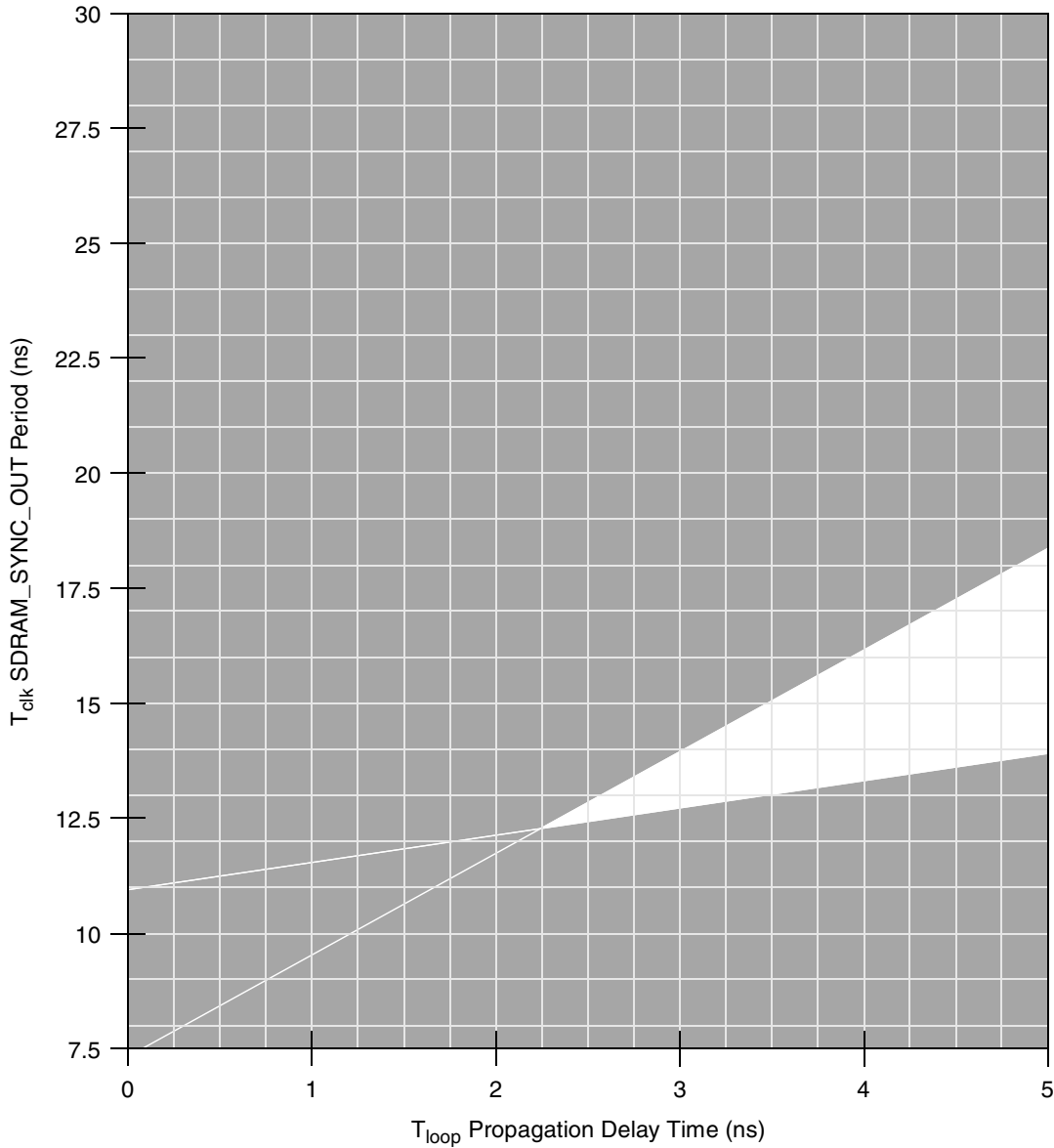
Figure 10. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Max Tap Delay

4.5.2 Input AC Timing Specifications

Table 10 provides the input AC timing specifications at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. See Figure 11 and Figure 12.

Table 10. Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b	Memory input signals valid to *sys_logic_clk* (input setup)				

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Table 10. Input AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
10b0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	0.5	—		
10c	PIC miscellaneous debug input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10d	I^{2}C input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.4	1.0	ns	7
11a	*sys_logic_clk* to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	2.1	—		
11b	$\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:

1. All PCI signals are measured from GV_{DD}_OV_{DD}/2 of the rising edge of PCI_SYNC_IN to $0.4 \times GV_{DD}$_OV_{DD} of the signal in question for 3.3-V PCI signaling levels. See Figure 12.

2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock. *sys_logic_clk*. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.

3. Input timings are measured at the pin.

4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.

5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ signal. See Figure 13.

6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5:4 of register offset <0x77> to select the desired input setup and hold times.

7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. The feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened to accommodate this range relative to the SDRAM clock output trace lengths to maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*. It is recommended that the length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN be shortened by 0.7 ns because that is the midpoint of the range of T_{os} and allows the impact from the range of T_{os} to be reduced. Additional analyses of trace lengths and SDRAM loading must be performed to optimize timing. For details on trace measurements and the T_{os} problem, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*.
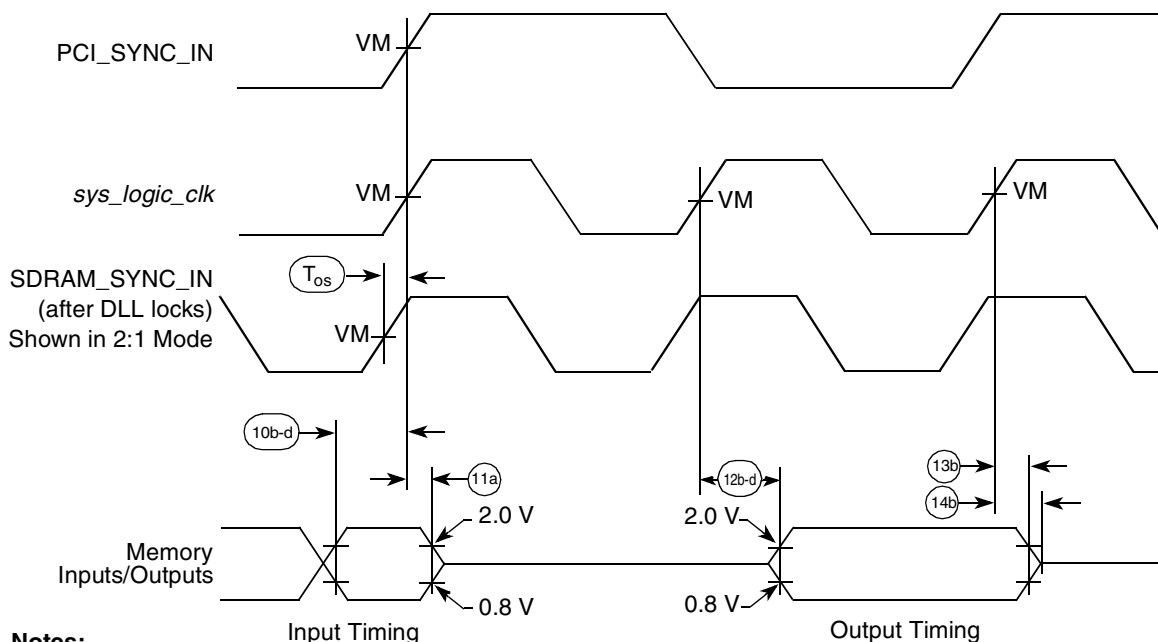
Notes:

VM = Midpoint voltage (1.4 V).

10b-d = Input signals valid timing.

11a = Input hold time of SDRAM_SYNC_IN to memory.

12b-d = *sys_logic_clk* to output valid timing.

13b = Output hold time for non-PCI signals.

14b = SDRAM-SYNC_IN to output high-impedance timing for non-PCI signals.

T_{os} = Offset timing required to align *sys_logic_clk* with SDRAM_SYNC_IN. The SDRAM_SYNC_IN signal is adjusted by the DLL to accommodate for internal delay. This causes SDRAM_SYNC_IN to appear before *sys_logic_clk* once the DLL locks.

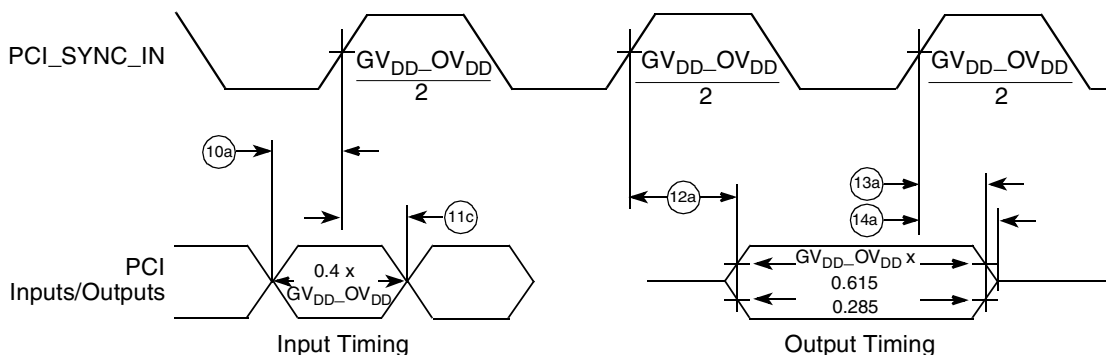**Figure 11. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN**

Figure 12. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

Figure 13 shows the input timing diagram for mode select signals.
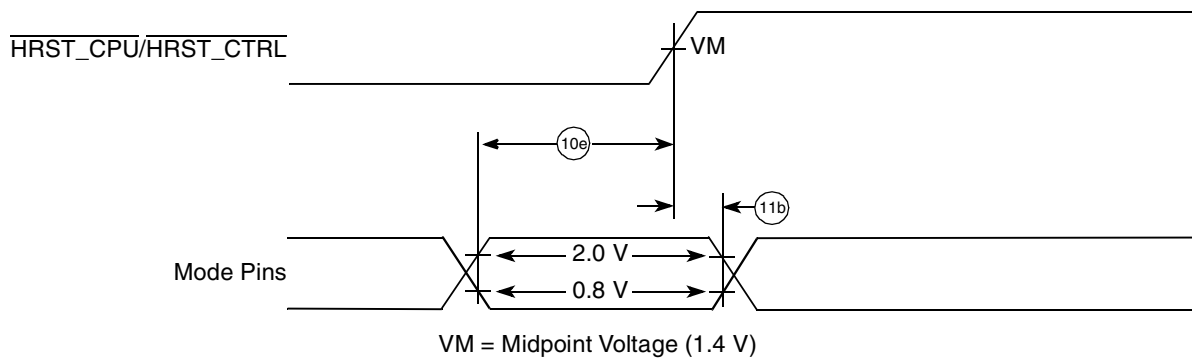

VM = Midpoint Voltage (1.4 V)

Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V (see Figure 11). All output timings assume a purely resistive 50-Ω load (see Figure 14). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths that Table 4 indicates.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{MCP}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{MCP}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{MCP}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{MCP}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory address, control, and data signals)	—	4.5	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I²C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/Port X)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{MCP}$,CKE] = 11, 66 MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{MCP}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{MCP}$,CKE] = 01, 33 MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{MCP}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 11. Output AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
14b	*sys_logic_clk* to output high impedance (for all others)	—	4.0	ns	2

Notes:

1. All PCI signals are measured from $GV_{DD}\_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times GV_{DD}\_OV_{DD}$ or $0.615 \times GV_{DD}\_OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.

2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk* to the TTL level (0.8 or 2.0 V) of the signal in question. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.

3. PCI bused signals are composed of the following signals: $\overline{LOCK}$, $\overline{IRDY}$, $\overline{C/BE}$[3:0], PAR, $\overline{TRDY}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$, AD[31:0], $\overline{REQ}$[4:0], $\overline{GNT}$[4:0], $\overline{IDSEL}$, and $\overline{INTA}$.

4. To meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8241 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{MCP}$ and CKE reset configuration signals; the values on these two signals are inverted and subsequently stored as the initial settings of PCI_HOLD_DEL = PMCR2[5, 4] (power management configuration register 2 <0x72>), respectively. Because $\overline{MCP}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Additional output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. See Figure 15 for PCI_HOLD_DEL effect on output valid and hold time.
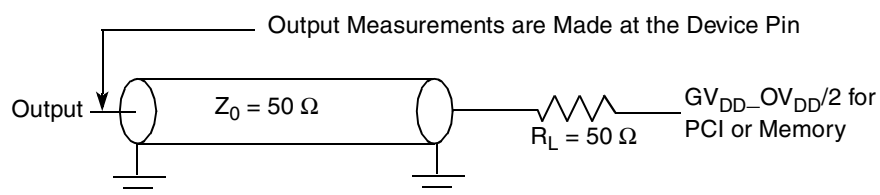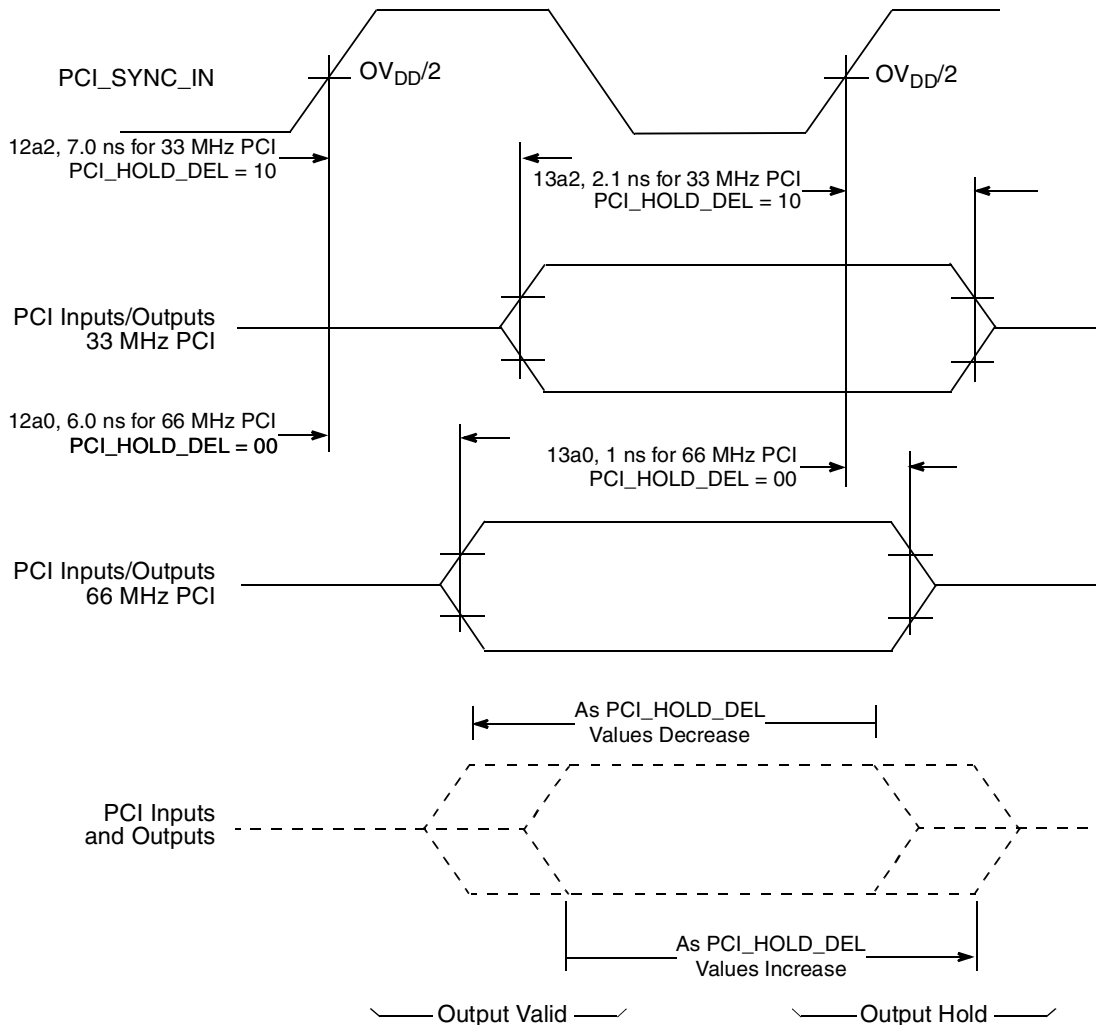
Figure 14 provides the AC test load for the MPC8241.

Figure 14. AC Test Load for the MPC8241

Note: Diagram not to scale.

Figure 15. PCI_HOLD_DEL Effect on Output Valid and Hold Time

4.6 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8241.

4.6.1 I²C DC Electrical Characteristics

Table 12 provides the DC electrical characteristics for the I²C interfaces.

Table 12. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	−0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

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