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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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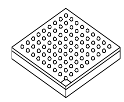
MSC7118

Low-Cost 16-bit DSP with DDR Controller



MAP-BGA–400
17 mm × 17 mm

- StarCore® SC1400 DSP extended core with one SC1400 DSP core, 256 Kbyte of internal SRAM M1 memory, 16 way 16 Kbyte instruction cache (ICache), four-entry write buffer, programmable interrupt controller (PIC), and low-power Wait and Stop processing modes.
- 192 Kbyte M2 memory for critical data and temporary data buffering.
- 8 Kbyte boot ROM.
- AHB-Lite crossbar switch that allows parallel data transfers between four master ports and six slave ports, where each port connects to an AHB-Lite bus; fixed or round robin priority programmable at each slave port; programmable bus parking at each slave port; low power mode.
- Internal PLL generates up to 300 MHz clock for the SC1400 core and up to 150 MHz for the crossbar switch, DMA channels, M2 memory, and other peripherals.
- Clock synthesis module provides predivision of PLL input clock; independent clocking of the internal timers and DDR module; programmable operation in the SC1400 low power Stop mode; independent shutdown of different regions of the device.
- Enhanced 16-bit wide host interface (HDI16) provides a glueless connection to industry-standard microcomputers, microprocessors, and DSPs and can also operate with an 8-bit host data bus, making if fully compatible with the DSP56300 HI08 from the external host side.
- DDR memory controller that supports byte enables for up to a 32-bit data bus; glueless interface to 150 MHz 14-bit page mode DDR-RAM; 14-bit external address bus supporting up to 1 Gbyte; and 16-bit or 32-bit external data bus.
- Programmable memory interface with independent read buffers, programmable predictive read feature for each buffer, and a write buffer.
- System control unit performs software watchdog timer function; includes programmable bus time-out monitors on AHB-Lite slave buses; includes bus error detection and programmable time-out monitors on AHB-Lite master buses; and has address out-of-range detection on each crossbar switch buses.
- Event port collects and counts important signal events including DMA and interrupt requests and trigger events such as interrupts, breakpoints, DMA transfers, or wake-up events; units operate independently, in sequence, or triggered externally; can be used standalone or with the OCE10.
- Multi-channel DMA controller with 32 time-multiplexed unidirectional channels, priority-based time-multiplexing between channels using 32 internal priority levels, fixed- or round-robin-priority operation, major-minor loop structure, and $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol from requesting units.
- Two independent TDM modules with independent receive and transmit, programmable sharing of frame sync and clock, programmable word size (8 or 16-bit), hardware-base A-law/μ-law conversion, up to 50 Mbps data rate per TDM, up to 128 channels, with glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses.
- UART with full-duplex operation up to 5.0 Mbps.
- Up to 41 general-purpose input/output (GPIO) ports.
- I^2C interface that allows booting from EEPROM devices up to 1 Mbyte.
- Two quad timer modules, each with sixteen configurable 16-bit timers.
- fieldBIST™ unit detects and provides visibility into unlikely field failures for systems with high availability to ensure structural integrity, that the device operates at the rated speed, is free from reliability defects, and reports diagnostics for partial or complete device inoperability.
- Standard JTAG interface allows easy integration to system firmware and internal on-chip emulation (OCE10) module.
- Optional booting external host via 8-bit or 16-bit access through the HDI16, I^2C, or SPI using in the boot ROM to access serial SPI Flash/EEPROM devices; different clocking options during boot with the PLL on or off using a variety of input frequency ranges.

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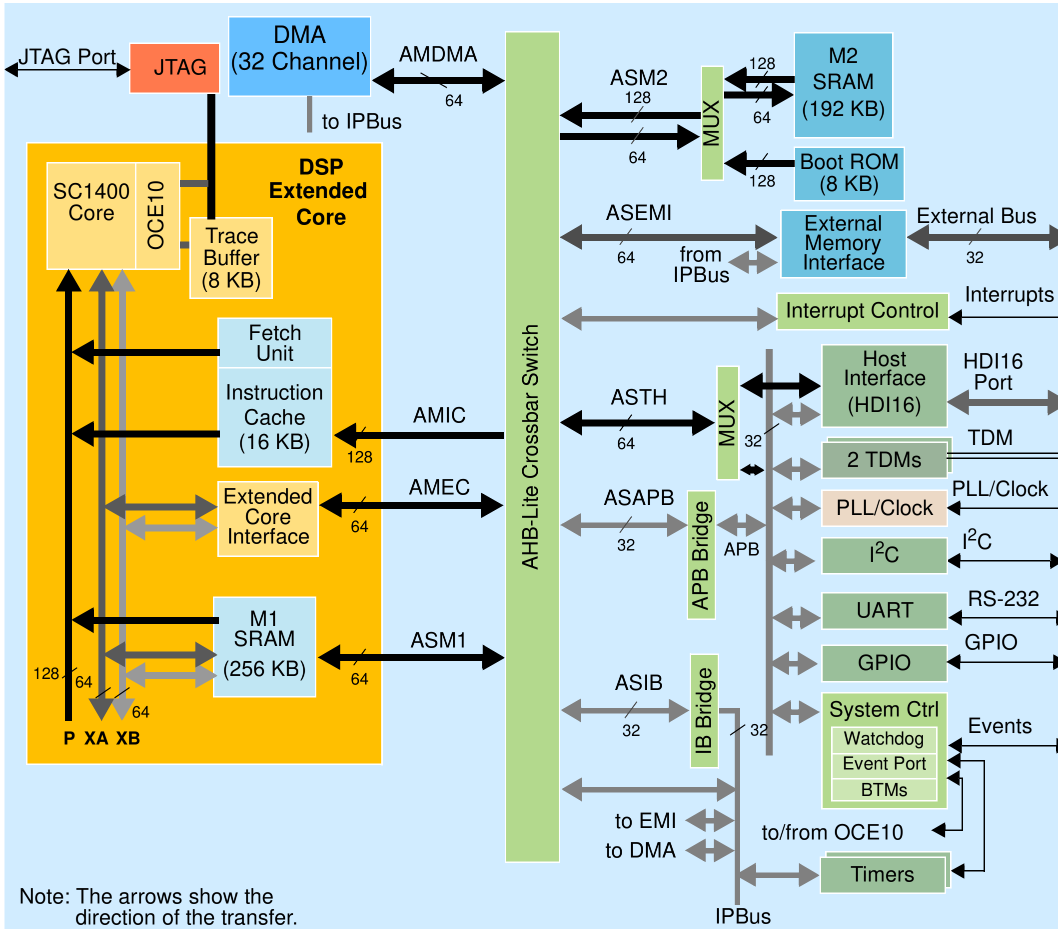

Figure 1. MSC7118 Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC7118 package ball grid array layouts and pinout allocation tables.

1.1 MAP-BGA Ball Layout Diagrams

Top and bottom views of the MAP-BGA package are shown in **Figure 2** and **Figure 3** with their ball location index numbers.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	DQM1	DQS2	CK	$\overline{CK}$	HD15	HD12	HD10	HD7	HD6	HD4	HD1	HD0	GND	BM3	NC	NC	NC	NC
B	V_{DDM}	NC	$\overline{CS0}$	DQM2	DQS3	DQS0	CKE	$\overline{WE}$	HD14	HD11	HD8	HD5	HD2	NC	BM2	NC	NC	NC	NC	NC
C	D24	D30	D25	$\overline{CS1}$	DQM3	DQM0	DQS1	$\overline{RAS}$	$\overline{CAS}$	HD13	HD9	HD3	NC	NC	NC	NC	NC	NC	NC	NC
D	V_{DDM}	D28	D27	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
E	GND	D26	D31	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
F	V_{DDM}	D15	D29	V_{DDC}	V_{DDC}	V_{DDC}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
G	GND	D13	GND	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
H	D14	D12	D11	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	HA2	HA1
J	D10	V_{DDM}	D9	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	HA3	$\overline{HACK}$	$\overline{HREQ}$
K	D0	GND	D8	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	HA0	HDDS	$\overline{HDS}$
L	D1	GND	D3	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{HCS2}$	$\overline{HCS1}$	HRW
M	D2	V_{DDM}	D5	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDC}	V_{DDC}	SDA	UTXD	URXD
N	D4	D6	V_{REF}	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	CLKIN	SCL	V_{SSPLL}
P	D7	D17	D16	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{PORESET}$	TPSEL	V_{DDPLL}
R	GND	D19	D18	V_{DDM}	V_{DDM}	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	GND	GND	V_{DDIO}	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	TDO	EE0	TEST0
T	V_{DDM}	D20	D22	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	MDIO	TMS	$\overline{HRESET}$
U	GND	D21	D23	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	COL	TCK	$\overline{TRST}$
V	V_{DDM}	NC	A13	A11	A10	A5	A2	BA0	NC	EVNT0	EVNT4	T0TCK	T1RFS	T1TD	TX_ER	RXD2	RXD0	TX_EN	CRS	TDI
W	GND	V_{DDM}	A12	A8	A7	A6	A3	NC	EVNT1	EVNT2	T0RFS	T0TFS	T1RD	T1TFS	TXD2	RXD3	TXD1	TXCLK	RX_ER	MDC
Y	V_{DDM}	GND	A9	A1	A0	A4	BA1	$\overline{NMI}$	EVNT3	T0RCK	T0RD	T0TD	T1RCK	T1TCK	TXD3	RXCLK	TXD0	RXD1	GND	RX_DV

Figure 2. MSC7118 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Bottom View

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	BM3	GND	HD0	HD1	HD4	HD6	HD7	HD10	HD12	HD15	$\overline{CK}$	CK	DQS2	DQM1	GND	GND
B	NC	NC	NC	NC	NC	BM2	NC	HD2	HD5	HD8	HD11	HD14	$\overline{WE}$	CKE	DQS0	DQS3	DQM2	$\overline{CS0}$	NC	V_{DDM}
C	NC	NC	NC	NC	NC	NC	NC	NC	HD3	HD9	HD13	$\overline{CAS}$	$\overline{RAS}$	DQS1	DQM0	DQM3	$\overline{CS1}$	D25	D30	D24
D	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	GND	D27	D28	V_{DDM}
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	V_{DDM}	D31	D26	GND
F	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DD}	V_{DD}	V_{DD}	D29	D15	V_{DDM}
G	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	GND	D13	GND
H	HA1	HA2	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D11	D12	D14
J	$\overline{HREQ}$	$\overline{HACK}$	HA3	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D9	V_{DDM}	D10
K	$\overline{HDS}$	HDDS	HA0	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D8	GND	D0
L	HRW	$\overline{HCS1}$	$\overline{HCS2}$	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D3	GND	D1
M	URXD	UTXD	SDA	V_{DD}	V_{DD}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D5	V_{DDM}	D2
N	V_{SSPLL}	SCL	CLKIN	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{REF}	D6	D4
P	V_{DDPLL}	TPSEL	$\overline{PORESET}$	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D16	D17	D7
R	TEST0	EE0	TDO	V_{DD}	V_{DDIO}	V_{DDIO}	GND	V_{DDIO}	GND	GND	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	V_{DDM}	V_{DDM}	D18	D19	GND
T	$\overline{HRESET}$	TMS	MDIO	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	D22	D20	V_{DDM}
U	$\overline{TRST}$	TCK	COL	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	D23	D21	GND
V	TDI	CRS	TX_EN	RXD0	RXD2	TX_ER	T1TD	T1RFS	T0TCK	EVNT4	EVNT0	NC	BA0	A2	A5	A10	A11	A13	NC	V_{DDM}
W	MDC	RX_ER	TXCLK	TXD1	RXD3	TXD2	T1TFS	T1RD	T0TFS	T0RFS	EVNT2	EVNT1	NC	A3	A6	A7	A8	A12	V_{DDM}	GND
Y	RX_DV	GND	RXD1	TXD0	RXCLK	TXD3	T1TCK	T1RCK	TOTD	T0RD	T0RCK	EVNT3	$\overline{NMI}$	BA1	A4	A0	A1	A9	GND	V_{DDM}

Figure 3. MSC7118 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7118 Signals by Ball Designator

<table>
<tr><th rowspan="3">Number</th><th colspan="6">Signal Names</th></tr>
<tr><th rowspan="2">End of Reset</th><th colspan="3">Software Controlled</th><th colspan="2">Hardware Controlled</th></tr>
<tr><th>GPI Enabled (Default)</th><th>Interrupt Enabled</th><th>GPO Enabled</th><th>Primary</th><th>Alternate</th></tr>
<tr><td>A1</td><td colspan="6">GND</td></tr>
<tr><td>A2</td><td colspan="6">GND</td></tr>
<tr><td>A3</td><td colspan="6">DQM1</td></tr>
<tr><td>A4</td><td colspan="6">DQS2</td></tr>
<tr><td>A5</td><td colspan="6">CK</td></tr>
<tr><td>A6</td><td colspan="6">$\overline{CK}$</td></tr>
<tr><td>A7</td><td colspan="3">GPIC7</td><td>GPOC7</td><td colspan="2">HD15</td></tr>
<tr><td>A8</td><td colspan="3">GPIC4</td><td>GPOC4</td><td colspan="2">HD12</td></tr>
<tr><td>A9</td><td colspan="3">GPIC2</td><td>GPOC2</td><td colspan="2">HD10</td></tr>
<tr><td>A10</td><td colspan="4">reserved</td><td colspan="2">HD7</td></tr>
<tr><td>A11</td><td colspan="4">reserved</td><td colspan="2">HD6</td></tr>
<tr><td>A12</td><td colspan="4">reserved</td><td colspan="2">HD4</td></tr>
<tr><td>A13</td><td colspan="4">reserved</td><td colspan="2">HD1</td></tr>
<tr><td>A14</td><td colspan="4">reserved</td><td colspan="2">HD0</td></tr>
<tr><td>A15</td><td colspan="6">GND</td></tr>
<tr><td>A16</td><td>BM3</td><td colspan="2">GPID8</td><td>GPOD8</td><td colspan="2">reserved</td></tr>
<tr><td>A17</td><td colspan="6">NC</td></tr>
<tr><td>A18</td><td colspan="6">NC</td></tr>
<tr><td>A19</td><td colspan="6">NC</td></tr>
<tr><td>A20</td><td colspan="6">NC</td></tr>
<tr><td>B1</td><td colspan="6">V_{DDM}</td></tr>
<tr><td>B2</td><td colspan="6">NC</td></tr>
<tr><td>B3</td><td colspan="6">$\overline{CS0}$</td></tr>
<tr><td>B4</td><td colspan="6">DQM2</td></tr>
<tr><td>B5</td><td colspan="6">DQS3</td></tr>
<tr><td>B6</td><td colspan="6">DQS0</td></tr>
<tr><td>B7</td><td colspan="6">CKE</td></tr>
<tr><td>B8</td><td colspan="6">$\overline{WE}$</td></tr>
<tr><td>B9</td><td colspan="3">GPIC6</td><td>GPOC6</td><td colspan="2">HD14</td></tr>
<tr><td>B10</td><td colspan="3">GPIC3</td><td>GPOC3</td><td colspan="2">HD11</td></tr>
<tr><td>B11</td><td colspan="3">GPIC0</td><td>GPOC0</td><td colspan="2">HD8</td></tr>
<tr><td>B12</td><td colspan="4">reserved</td><td colspan="2">HD5</td></tr>
<tr><td>B13</td><td colspan="4">reserved</td><td colspan="2">HD2</td></tr>
</table>

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
B14	NC					
B15	BM2	GPID7		GPOD7	reserved	
B16	NC					
B17	NC					
B18	NC					
B19	NC					
B20	NC					
C1	D24					
C2	D30					
C3	D25					
C4	$\overline{CS1}$					
C5	DQM3					
C6	DQM0					
C7	DQS1					
C8	$\overline{RAS}$					
C9	$\overline{CAS}$					
C10	GPIC5			GPOC5	HD13	
C11	GPIC1			GPOC1	HD9	
C12	reserved				HD3	
C13	NC					
C14	NC					
C15	NC					
C16	NC					
C17	NC					
C18	NC					
C19	NC					
C20	NC					
D1	V_{DDM}					
D2	D28					
D3	D27					
D4	GND					
D5	V_{DDM}					
D6	V_{DDM}					
D7	V_{DDM}					
D8	V_{DDM}					
D9	V_{DDM}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D10	V_{DDM}					
D11	V_{DDIO}					
D12	V_{DDIO}					
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					
F11	V_{DDM}					
F12	GND					
F13	GND					
F14	GND					
F15	V_{DDIO}					
F16	V_{DDC}					
F17	V_{DDC}					
F18	NC					
F19	NC					
F20	NC					
G1	GND					
G2	D13					
G3	GND					
G4	V_{DDM}					
G5	V_{DDM}					
G6	GND					
G7	GND					
G8	GND					
G9	GND					
G10	GND					
G11	GND					
G12	GND					
G13	GND					
G14	GND					
G15	V_{DDIO}					
G16	V_{DDIO}					
G17	V_{DDC}					
G18	NC					
G19	NC					
G20	NC					
H1	D14					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H2	D12					
H3	D11					
H4	V_{DDM}					
H5	V_{DDM}					
H6	GND					
H7	GND					
H8	GND					
H9	GND					
H10	GND					
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
J18	GPIC11			GPOC11	HA3	
J19	reserved				$\overline{HACK}$/HACK or $\overline{HRRQ}$/HRRQ	
J20	HDSP	reserved			$\overline{HREQ}$/HREQ or $\overline{HTRQ}$/HTRQ	
K1	D0					
K2	GND					
K3	D8					
K4	V_{DDC}					
K5	V_{DDM}					
K6	GND					
K7	GND					
K8	GND					
K9	GND					
K10	GND					
K11	GND					
K12	GND					
K13	GND					
K14	GND					
K15	V_{DDIO}					
K16	V_{DDIO}					
K17	V_{DDC}					
K18	reserved				HA0	
K19	reserved				HDDS	
K20	reserved				$\overline{HDS}$/HDS or $\overline{HWR}$/HWR	
L1	D1					
L2	GND					
L3	D3					
L4	V_{DDC}					
L5	V_{DDM}					
L6	GND					
L7	GND					
L8	GND					
L9	GND					
L10	GND					
L11	GND					
L12	GND					
L13	GND					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
L14	V_{DDIO}					
L15	V_{DDIO}					
L16	V_{DDIO}					
L17	V_{DDC}					
L18	GPIB11			GPOB11	$\overline{HCS2}$/HCS2	
L19	reserved				$\overline{HCS1}$/HCS1	
L20	reserved				HRW or $\overline{HRD}$/HRD	
M1	D2					
M2	V_{DDM}					
M3	D5					
M4	V_{DDM}					
M5	V_{DDM}					
M6	GND					
M7	GND					
M8	GND					
M9	GND					
M10	GND					
M11	GND					
M12	GND					
M13	GND					
M14	GND					
M15	GND					
M16	V_{DDC}					
M17	V_{DDC}					
M18	GPIA14		$\overline{IRQ15}$	GPOA14	SDA	
M19	GPIA12		$\overline{IRQ3}$	GPOA12	UTXD	
M20	GPIA13		$\overline{IRQ2}$	GPOA13	URXD	
N1	D4					
N2	D6					
N3	V_{REF}					
N4	V_{DDM}					
N5	V_{DDM}					
N6	V_{DDM}					
N7	GND					
N8	GND					
N9	GND					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$	GPOA15	SCL	
N20	V_{SSPLL}					
P1	D7					
P2	D17					
P3	D16					
P4	V_{DDM}					
P5	V_{DDM}					
P6	V_{DDM}					
P7	GND					
P8	GND					
P9	GND					
P10	GND					
P11	GND					
P12	GND					
P13	GND					
P14	GND					
P15	V_{DDIO}					
P16	V_{DDIO}					
P17	V_{DDC}					
P18	$\overline{PORESET}$					
P19	TPSEL					
P20	V_{DDPLL}					
R1	GND					
R2	D19					
R3	D18					
R4	V_{DDM}					
R5	V_{DDM}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
R6	V_{DDM}					
R7	GND					
R8	V_{DDM}					
R9	GND					
R10	V_{DDM}					
R11	GND					
R12	GND					
R13	V_{DDIO}					
R14	GND					
R15	V_{DDIO}					
R16	V_{DDIO}					
R17	V_{DDC}					
R18	TDO					
R19	reserved				EE0/DBREQ	
R20	TEST0					
T1	V_{DDM}					
T2	D20					
T3	D22					
T4	V_{DDM}					
T5	V_{DDM}					
T6	V_{DDC}					
T7	V_{DDM}					
T8	V_{DDM}					
T9	V_{DDC}					
T10	V_{DDM}					
T11	V_{DDM}					
T12	V_{DDIO}					
T13	V_{DDIO}					
T14	V_{DDIO}					
T15	V_{DDIO}					
T16	V_{DDC}					
T17	V_{DDC}					
T18	reserved				MDIO	
T19	TMS					
T20	$\overline{HRESET}$					
U1	GND					

Table 1. MSC7118 Signals by Ball Designator (continued)

<table>
<tr><th rowspan="3">Number</th><th colspan="6">Signal Names</th></tr>
<tr><th rowspan="2">End of Reset</th><th colspan="3">Software Controlled</th><th colspan="2">Hardware Controlled</th></tr>
<tr><th>GPI Enabled (Default)</th><th>Interrupt Enabled</th><th>GPO Enabled</th><th>Primary</th><th>Alternate</th></tr>
<tr><td>U2</td><td colspan="6">D21</td></tr>
<tr><td>U3</td><td colspan="6">D23</td></tr>
<tr><td>U4</td><td colspan="6">V_{DDM}</td></tr>
<tr><td>U5</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U6</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U7</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U8</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U9</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U10</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U11</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U12</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U13</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U14</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U15</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U16</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U17</td><td colspan="6">V_{DDC}</td></tr>
<tr><td>U18</td><td colspan="4">reserved</td><td colspan="2">COL</td></tr>
<tr><td>U19</td><td colspan="6">TCK</td></tr>
<tr><td>U20</td><td colspan="6">$\overline{TRST}$</td></tr>
<tr><td>V1</td><td colspan="6">V_{DDM}</td></tr>
<tr><td>V2</td><td colspan="6">NC</td></tr>
<tr><td>V3</td><td colspan="6">A13</td></tr>
<tr><td>V4</td><td colspan="6">A11</td></tr>
<tr><td>V5</td><td colspan="6">A10</td></tr>
<tr><td>V6</td><td colspan="6">A5</td></tr>
<tr><td>V7</td><td colspan="6">A2</td></tr>
<tr><td>V8</td><td colspan="6">BA0</td></tr>
<tr><td>V9</td><td colspan="6">NC</td></tr>
<tr><td>V10</td><td colspan="4">reserved</td><td colspan="2">EVNT0</td></tr>
<tr><td>V11</td><td>SWTE</td><td>GPIA16</td><td>$\overline{IRQ12}$</td><td>GPOA16</td><td colspan="2">EVNT4</td></tr>
<tr><td>V12</td><td colspan="2">GPIA8</td><td>$\overline{IRQ6}$</td><td>GPOA8</td><td colspan="2">T0TCK</td></tr>
<tr><td>V13</td><td colspan="2">GPIA4</td><td>$\overline{IRQ1}$</td><td>GPOA4</td><td colspan="2">T1RFS</td></tr>
<tr><td>V14</td><td colspan="2">GPIA0</td><td>$\overline{IRQ11}$</td><td>GPOA0</td><td colspan="2">T1TD</td></tr>
<tr><td>V15</td><td colspan="2">GPIA28</td><td>$\overline{IRQ17}$</td><td>GPOA28</td><td>TX_ER</td><td>reserved</td></tr>
<tr><td>V16</td><td colspan="3">GPID6</td><td>GPOD6</td><td>RXD2</td><td>reserved</td></tr>
<tr><td>V17</td><td colspan="2">GPIA22</td><td>$\overline{IRQ22}$</td><td>GPOA22</td><td colspan="2">RXD0</td></tr>
</table>

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
V18	GPIA24		$\overline{IRQ24}$	GPOA24	TX_EN	
V19	reserved				CRS	
V20	TDI					
W1	GND					
W2	V_{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{IRQ13}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{IRQ5}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{IRQ7}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{IRQ8}$	GPOA3	T1RD	
W14	GPIA1		$\overline{IRQ10}$	GPOA1	T1TFS	
W15	GPID4			GPOD4	TXD2	reserved
W16	GPIA27		$\overline{IRQ18}$	GPOA27	RXD3	reserved
W17	GPIA19		$\overline{IRQ19}$	GPOA19	TXD1	
W18	GPIA23		$\overline{IRQ23}$	GPOA23	TXCLK or REFCLK	
W19	GPIA26		$\overline{IRQ26}$	GPOA26	RX_ER	
W20	H8BIT	reserved			MDC	
Y1	V_{DDM}					
Y2	GND					
Y3	A9					
Y4	A1					
Y5	A0					
Y6	A4					
Y7	BA1					
Y8	reserved		$\overline{NMI}$	reserved		
Y9	BM1	GPIC15		GPOC15	EVNT3	
Y10	GPIA11		$\overline{IRQ4}$	GPOA11	T0RCK	
Y11	GPIA9			GPOA9	T0RD	
Y12	GPIA6			GPOA6	T0TD	
Y13	GPIA5		$\overline{IRQ0}$	GPOA5	T1RCK	

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
Y14	GPIA2		$\overline{\text{IRQ9}}$	GPOA2	T1TCK	
Y15	GPIA29		$\overline{\text{IRQ16}}$	GPOA29	TXD3	reserved
Y16	GPID5			GPOD5	RXCLK	reserved
Y17	GPIA20		$\overline{\text{IRQ20}}$	GPOA20	TXD0	
Y18	GPIA21		$\overline{\text{IRQ21}}$	GPOA21	RXD1	
Y19	GND					
Y20	GPIA25		$\overline{\text{IRQ25}}$	GPOA25	RX_DV or CRS_DV	

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC711x Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC7118.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.5	V
Memory supply voltage	V_{DDM}	4.0	V
PLL supply voltage	V_{DDPLL}	1.5	V
I/O supply voltage	V_{DDIO}	–0.2 to 4.0	V
Input voltage	V_{IN}	(GND – 0.2) to 4.0	V
Reference voltage	V_{REF}	4.0	V
Maximum operating temperature	T_J	105	°C
Minimum operating temperature	T_A	–40	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.1**, *Thermal Design Considerations* includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.14 to 1.26	V
Memory supply voltage	V_{DDM}	2.38 to 2.63	V
PLL supply voltage	V_{DDPLL}	1.14 to 1.26	V
I/O supply voltage	V_{DDIO}	3.14 to 3.47	V
Reference voltage	V_{REF}	1.19 to 1.31	V
Operating temperature range	T_J T_A	maximum: 105 minimum: –40	°C °C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7118 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	23	20	°C/W
Junction-to-board[4]	$R_{\theta JB}$	12		°C/W
Junction-to-case[5]	$R_{\theta JC}$	7		°C/W
Junction-to-package-top[6]	Ψ_{JT}	2		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC7118.

Note: The leakage current is measured for nominal voltage values must vary in the same direction (for example, both V_{DDIO} and V_{DDC} vary by +2 percent or both vary by –2 percent).

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Core and PLL voltage	V_{DDC} V_{DDPLL}	1.14	1.2	1.26	V
DRAM interface I/O voltage[1]	V_{DDM}	2.375	2.5	2.625	V
I/O voltage	V_{DDIO}	3.135	3.3	3.465	V
DRAM interface I/O reference voltage[2]	V_{REF}	$0.49 \times V_{DDM}$	1.25	$0.51 \times V_{DDM}$	V
DRAM interface I/O termination voltage[3]	VTT	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input high CLKIN voltage	V_{IHCLK}	2.4	3.0	3.465	V
DRAM interface input high I/O voltage	V_{IHM}	$V_{REF} + 0.28$	V_{DDM}	$V_{DDM} + 0.3$	V
DRAM interface input low I/O voltage	V_{ILM}	–0.3	GND	$V_{REF} - 0.18$	V
Input leakage current, $V_{IN} = V_{DDIO}$	I_{IN}	–1.0	0.09	1	μA
V_{REF} input leakage current	I_{VREF}	—	—	5	μA

Table 5. DC Electrical Characteristics (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDIO}$	I_{OZ}	–1.0	0.09	1	μA
Signal low input current, $V_{IL} = 0.4$ V	I_L	–1.0	0.09	1	μA
Signal high input current, $V_{IH} = 2.0$ V	I_H	–1.0	0.09	1	μA
Output high voltage, $I_{OH} = –2$ mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, $I_{OL}= 5$ mA	V_{OL}	—	0	0.4	V
Typical power at 300 MHz[5]	P	—	324.0	—	mW

Notes:
1. The value of V_{DDM} at the MSC7118 device must remain within 50 mV of V_{DDM} at the DRAM device at all times.
2. V_{REF} must be equal to 50% of V_{DDM} and track V_{DDM} variations as measured at the receiver. Peak-to-peak noise must not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the MSC7118 device. It is the level measured at the far end signal termination. It should be equal to V_{REF}. This rail should track variations in the DC level of V_{REF}.
4. Output leakage for the memory interface is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ V_{DDM}.
5. The core power values were measured.using a standard EFR pattern at typical conditions (25°C, 300 MHz, 1.2 V core).

Table 6 lists the DDR DRAM capacitance.

Table 6. DDR DRAM Capacitance

Parameter/Condition	Symbol	Max	Unit
Input/output capacitance: DQ, DQS	C_{IO}	30	pF
Delta input/output capacitance: DQ, DQS	C_{DIO}	30	pF

Note: These values were measured under the following conditions:
- $V_{DDM} = 2.5$ V ± 0.125 V
- f = 1 MHz
- $T_A = 25$°C
- $V_{OUT} = V_{DDM}/2$
- V_{OUT} (peak to peak) = 0.2 V

2.5 AC Timings

This section presents timing diagrams and specifications for individual signals and parallel I/O outputs and inputs. All AC timings are based on a 30 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, use the following equations to compute the delay:

— Standard interface: $2.45 + (0.054 \times C_{load})$ ns

— DDR interface: $1.6 + (0.002 \times C_{load})$ ns

2.5.1 Clock and Timing Signals

The following tables describe clock signal characteristics. **Table 6** shows the maximum frequency values for internal (core, reference, and peripherals) and external (CLKO) clocks. You must ensure that maximum frequency values are not exceeded (see **Section 2.5.2** for the allowable ranges when using the PLL).

Table 6. Maximum Frequencies

Characteristic	Maximum in MHz
Core clock frequency (CLOCK)	300
External output clock frequency (CLKO)	75
Memory clock frequency (CK, $\overline{CK}$)	150
TDM clock frequency (TxRCK, TxTCK)	50

Table 7. Clock Frequencies in MHz

Characteristic	Symbol	Min	Max
CLKIN frequency	F_{CLKIN}	10	100
CLOCK frequency	F_{CORE}	—	300
CK, $\overline{CK}$ frequency	F_{CK}	—	150
TDMxRCK, TDMxTCK frequency	F_{TDMCK}	—	50
CLKO frequency	F_{CKO}	—	75
AHB/IPBus/APB clock frequency	F_{BCK}	—	150
Note: The rise and fall time of external clocks should be 5 ns maximum			

Table 8. System Clock Parameters

Characteristic	Min	Max	Unit
CLKIN frequency	10	100	MHz
CLKIN slope	—	5	ns
CLKIN frequency jitter (peak-to-peak)	—	1000	ps
CLKO frequency jitter (peak-to-peak)	—	150	ps

2.5.2 Configuring Clock Frequencies

This section describes important requirements for configuring clock frequencies in the MSC7118 device when using the PLL block. To configure the device clocking, you must program four fields in the Clock Control Register (CLKCTL):

- *PLLDVF field*. Specifies the PLL division factor (PLLDVF + 1) to divide the input clock frequency F_{CLKIN}. The output of the divider block is the input to the multiplier block.
- *PLLMLTF field*. Specifies the PLL multiplication factor (PLLMLTF + 1). The output from the multiplier block is the loop frequency F_{LOOP}.
- *RNG field*. Selects the available PLL frequency range for F_{VCO}, either F_{LOOP} when the RNG bit is set (1) or $F_{LOOP}/2$ when the RNG bit is cleared (0).
- *CKSEL field*. Selects F_{CLKIN}, F_{VCO}, or $F_{VCO}/2$ as the source for the core clock.

There are restrictions on the frequency range permitted at the beginning of the multiplication portion of the PLL that affect the allowable values for the PLLDVF and PLLMLTF fields. The following sections define these restrictions and provide guidelines to configure the device clocking when using the PLL. Refer to the Clock and Power Management chapter in the *MSC711x Reference Manual* for details on the clock programming model.

2.5.2.1 PLL Multiplier Restrictions

There are two restrictions for correct usage of the PLL block:

- The input frequency to the PLL multiplier block (that is, the output of the divider) must be in the range 10–25 MHz.
- The output frequency of the PLL multiplier must be in the range 266–532 MHz.

When programming the PLL for a desired output frequency using the PLLDVF, PLLMLTF, and RNG fields, you must meet these constraints.

2.5.2.2 Input Division Factors and Corresponding CLKIN Frequency Range

The value of the PLLDVF field determines the allowable CLKIN frequency range, as shown in **Table 9**.

Table 9. CLKIN Frequency Ranges by Divide Factor Value

PLLDVF Field Value	Input Divide Factor	CLKIN Frequency Range	Comments
0x00	1	10 to 25 MHz	Input Division by 1
0x01	2	20 to 50 MHz	Input Division by 2
0x02	3	30 to 75 MHz	Input Division by 3
0x03	4	40 to 100 MHz	Input Division by 4
0x04	5	50 to 100 MHz	Input Division by 5
0x05	6	60 to 100 MHz	Input Division by 6
0x06	7	70 to 100 MHz	Input Division by 7
0x07	8	80 to 100 MHz	Input Division by 8
0x08	9	90 to 100 MHz	Input Division by 9
0x09	10	100 MHz	Input Division by 10
Note: The maximum CLKIN frequency is 100 MHz. Therefore, the PLLDVF value must be in the range from 1–10.			

2.5.2.3 Multiplication Factor Range

The multiplier block output frequency ranges depend on the divided input clock frequency as shown in **Table 10**.

Table 10. PLLMLTF Ranges

Multiplier Block (Loop) Output Range	Minimum PLLMLTF Value	Maximum PLLMLTF Value
266 ≤ [Divided Input Clock × (PLLMLTF + 1)] ≤ 532 MHz	266/Divided Input Clock	532/Divided Input Clock
Note: This table results from the allowed range for F_{Loop}. The minimum and maximum multiplication factors are dependent on the frequency of the Divided Input Clock.		

2.5.2.4 Allowed Core Clock Frequency Range

The frequency delivered to the core, extended core, and peripherals depends on the value of the CLKCTRL[RNG] bit as shown in **Table 11**.

Table 11. F_{VCO} Frequency Ranges

CLKCTRL[RNG] Value	Allowed Range of F_{VCO}
1	$266 \le F_{VCO} \le 532$ MHz
0	$133 \le F_{VCO} \le 266$ MHz
Note: This table results from the allowed range for F_{VCO}, which is F_{Loop} modified by CLKCTRL[RNG].	

This bit along with the CKSEL determines the frequency range of the core clock.

Table 12. Resulting Ranges Permitted for the Core Clock

CLKCTRL[CKSEL]	CLKCTRL[RNG]	Resulting Division Factor	Allowed Range of Core Clock	Comments
11	1	1	266 ≤ core clock ≤ 300 MHz	Limited by maximum core frequency
11	0	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	1	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	0	4	66.5 ≤ core clock ≤ 133 MHz	Limited by range of PLL
Note: This table results from the allowed range for F_{OUT}, which depends on clock selected via CLKCTRL[CKSEL].				

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 13** summarizes this restriction.

Table 13. Core Clock Ranges When Using DDR

DDR Type	Allowed Frequency Range for DDR CK	Corresponding Range for the Core Clock	Comments
DDR 200 (PC-1600)	83–100 MHz	166 ≤ core clock ≤ 200 MHz	Core limited to 2 × maximum DDR frequency
DDR 266 (PC-2100)	83–133 MHz	166 ≤ core clock ≤ 266 MHz	Core limited to 2 × maximum DDR frequency
DDR 333 (PC-2600)	83–150 MHz	166 ≤ core clock ≤ 300 MHz	Core limited to 2 × maximum DDR frequency

2.5.3 Reset Timing

The MSC7118 device has several inputs to the reset logic. All MSC7118 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 14** describes the reset sources.

Table 14. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7118 and configures various attributes of the MSC7118. On PORESET, the entire MSC7118 device is reset. SPLL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7118. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7118 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7118 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 15 summarizes the reset actions that occur as a result of the different reset sources.

Table 15. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)
	External only	External or Internal (Software Watchdog or Bus Monitor)	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to **Section 2.5.3.1** for details).	Yes	No	No
PLL and clock synthesis states Reset	Yes	No	No
HRESET Driven	Yes	Yes	No
Software watchdog and bus time-out monitor registers	Yes	Yes	Yes
Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset	Yes	Yes	Yes
Extended core reset	Yes	Yes	Yes
Peripheral modules reset	Yes	Yes	Yes

2.5.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7118 reaches at least 2/3 V_{DD}.

2.5.3.2 Reset Configuration

The MSC7118 has two mechanisms for writing the reset configuration:

- From a host through the host interface (HDI16)
- From memory through the I^2C interface

Five signal levels (see **Chapter 1** for signal description details) are sampled on PORESET deassertion to define the boot and operating conditions:

- BM[0–1]
- SWTE
- H8BIT
- HDSP

2.5.3.3 Reset Timing Tables

Table 16 and **Figure 4** describe the reset timing for a reset configuration write.

Table 16. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Unit
1	Required external PORESET duration minimum	$16/F_{CLKIN}$	clocks
2	Delay from PORESET deassertion to HRESET deassertion	$521/F_{CLKIN}$	clocks
Note:	Timings are not tested, but are guaranteed by design.		

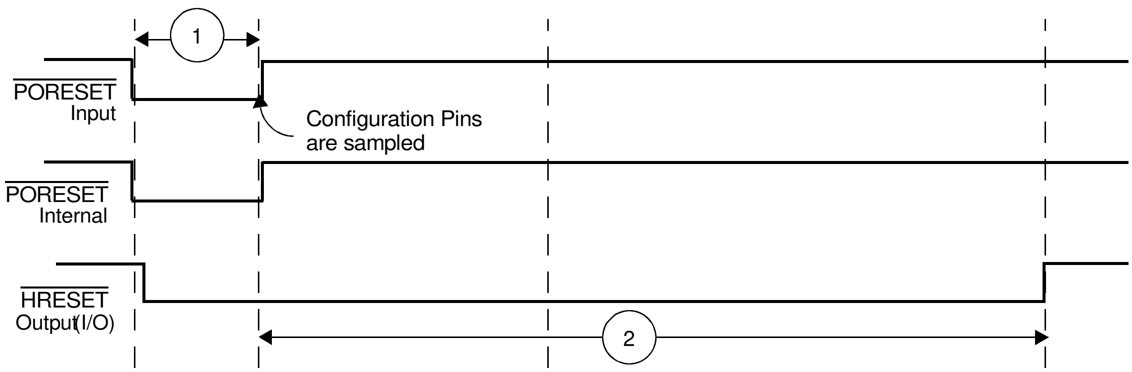

Figure 4. Timing Diagram for a Reset Configuration Write