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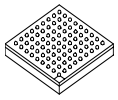
MSC8122



FC PBGA–431
20 mm × 20 mm

Quad Digital Signal Processor

- Four StarCore™ SC140 DSP extended cores, each with an SC140 DSP core, 224 Kbyte of internal SRAM M1 memory (1436 Kbyte total), 16 way 16 Kbyte instruction cache (ICache), four-entry write buffer, external cache support, programmable interrupt controller (PIC), local interrupt controller (LIC), and low-power Wait and Stop processing modes.
- 475 Kbyte M2 memory for critical data and temporary data buffering.
- 4 Kbyte boot ROM.
- M2-accessible multi-core MQBus connecting the M2 memory with all four cores, operating at the core frequency, with data bus access of up to 128-bit reads and up to 64-bit writes, central efficient round-robin arbiter for core access to the bus, and atomic operation control of M2 memory access by the cores and the local bus.
- Internal PLL configured are reset by configuration signal values.
- 60x-compatible system bus with 64 or 32 bit data and 32-bit address bus, support for multi-master designs, four-beat burst transfers (eight-beat in 32-bit data mode), port size of 64/32/16/8 bits controlled by the internal memory controller,.access to external memory or peripherals, access by an external host to internal resources, slave support with direct access to internal resources including M1 and M2 memories, and on-device arbitration for up to four master devices.
- Direct slave interface (DSI) using a 32/64-bit slave host interface with 21–25 bit addressing and 32/64-bit data transfers, direct access by an external host to internal and external resources, synchronous or asynchronous accesses with burst capability in synchronous mode, dual or single strobe mode, write and read buffers to improve host bandwidth, byte enable signals for 1/2/4/8-byte write granularity, sliding window mode for access using a reduced number of address pins, chip ID decoding to allow one $\overline{\text{CS}}$ signal to control multiple DSPs, broadcast mode to write to multiple DSPs, and big-endian/little-endian/munged support.
- Three mode signal multiplexing: 64-bit DSI and 32-bit system bus, 32-bit DSI and 64-bit system bus, or 32-bit DSI and 32-bit system bus.
- Flexible memory controller with three UPMs, a GPCM, a page-mode SDRAM machine, glueless interface to a variety of memories and devices, byte enables for 64- or 32-bit bus widths, 8 memory banks for external memories, and 2 memory banks for IPBus peripherals and internal memories.
- Multi-channel DMA controller with 16 time-multiplexed single channels, up to four external peripherals, $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol for two external peripherals,.service for up to 16 internal requests from up to 8 internal FIFOs per channel, FIFO generated watermarks and hungry requests, priority-based time-multiplexing between channels using 16 internal priority levels or round-robin time-multiplexing between channels, flexible channel configuration with connection to local bus or system bus, and flyby transfer support that bypasses the FIFO.
- Up to four independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/μ-law conversion, up to 128 Mbps data rate for all channels, with glueless interface to E1 or T1 framers, and can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.
- Ethernet controller with support for 10/100 Mbps MII/RMII/SMII including full- and half-duplex operation, full-duplex flow controls, out-of-sequence transmit queues, programmable maximum frame length including jumbo frames and VLAN tags and priority, retransmission after collision, CRC generation and verification of inbound/outbound packets, address recognition (including exact match, broadcast address, individual hash check, group hash check, and promiscuous mode), pattern matching, insertion with expansion or replacement for transmit frames, VLAN tag insertion, RMON statistics, local bus master DMA for descriptor fetching and buffer access, and optional multiplexing with GPIO (MII/RMII/SMII) or DSI/system bus signals lines (MII/RMII).
- UART with full-duplex operation up to 6.25 Mbps.
- Up to 32 general-purpose input/output (GPIO) ports.
- I^2C interface that allows booting from EEPROM devices.
- Two timer modules, each with sixteen configurable 16-bit timers.
- Eight programmable hardware semaphores.
- Global interrupt controller (GIC) with interrupt consolidation and routing to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and the cores; thirty-two virtual maskable interrupts (8 per core) and four virtual $\overline{\text{NMI}}$ (one per core) that can be generated by a simple write access.
- Optional booting external memory, external host, UART, TDM, or I^2C.

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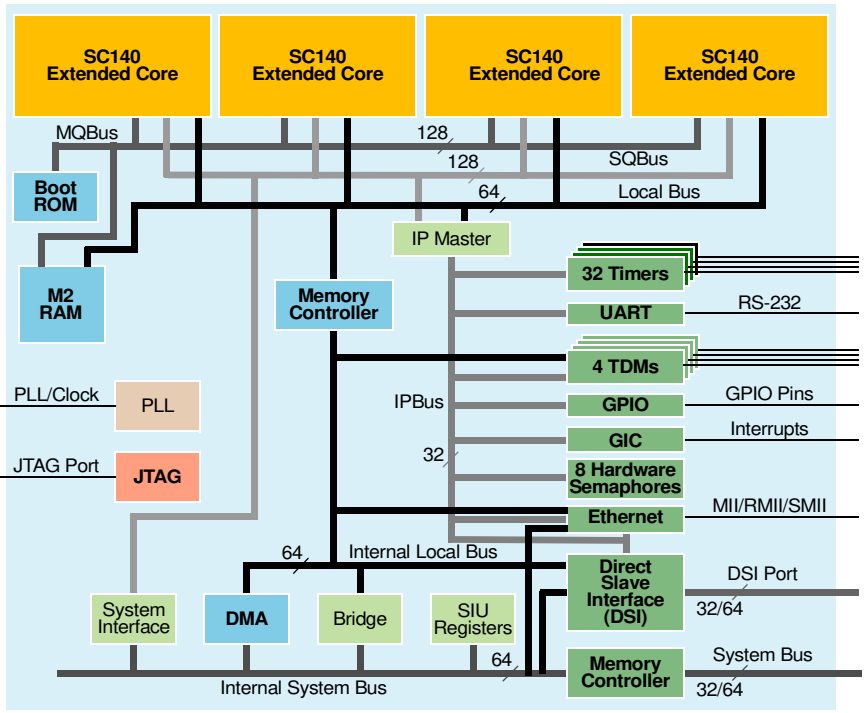
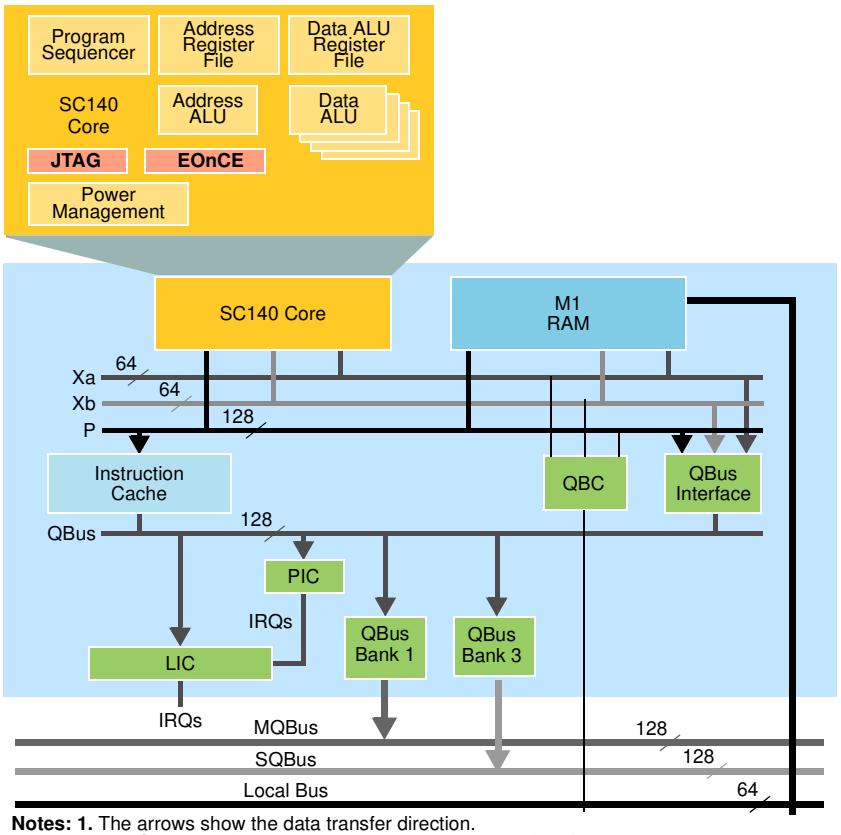


Figure 1. MSC8122 Block Diagram



Notes: **1.** The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. StarCore SC140 DSP Extended Core Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC8122 package ball grid array layouts and pinout allocation tables.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Top View

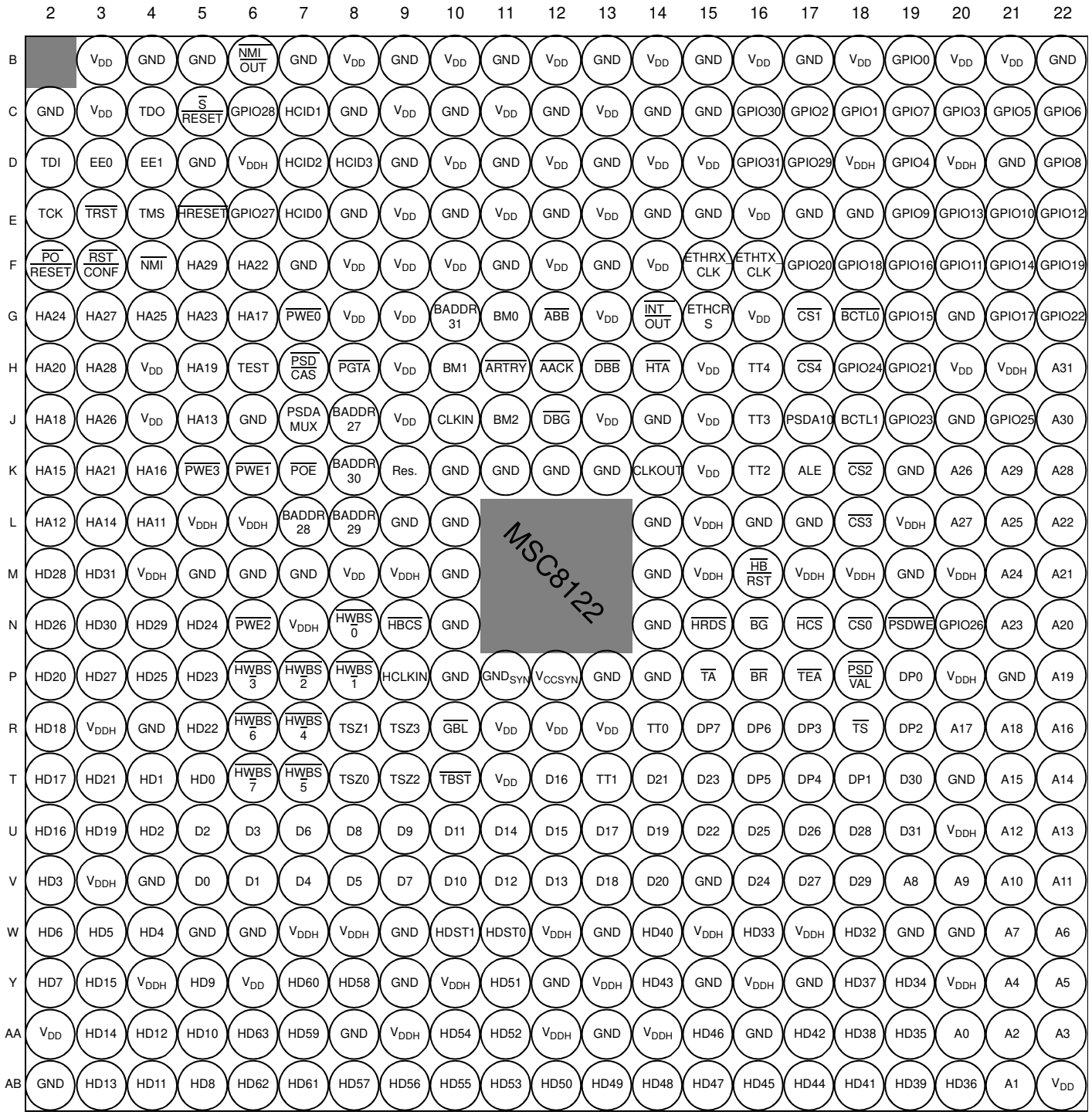


Figure 3. MSC8122 Package, Top View

Bottom View

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
B	GND	V_{DD}	V_{DD}	GPIO0	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	$\overline{NMI\ OUT}$	GND	GND	V_{DD}	
C	GPIO6	GPIO5	GPIO3	GPIO7	GPIO1	GPIO2	GPIO30	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID1	GPIO28	$\overline{S\ RESET}$	TDO	V_{DD}	GND
D	GPIO8	GND	V_{DDH}	GPIO4	V_{DDH}	GPIO29	GPIO31	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID3	HCID2	V_{DDH}	GND	EE1	EE0	TDI
E	GPIO12	GPIO10	GPIO13	GPIO9	GND	GND	V_{DD}	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID0	GPIO27	$\overline{HRESET}$	TMS	$\overline{TRST}$	TCK
F	GPIO19	GPIO14	GPIO11	GPIO16	GPIO18	GPIO20	ETHTX_CLK	ETHRX_CLK	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}	V_{DD}	GND	HA22	HA29	$\overline{NMI}$	$\overline{RST\ CONF}$	$\overline{PO\ RESET}$
G	GPIO22	GPIO17	GND	GPIO15	$\overline{BCTL0}$	$\overline{CS1}$	V_{DD}	ETHCRS	$\overline{INT\ OUT}$	V_{DD}	$\overline{ABB}$	BM0	BADDR31	V_{DD}	V_{DD}	$\overline{PWE0}$	HA17	HA23	HA25	HA27	HA24
H	A31	V_{DDH}	V_{DD}	GPIO21	GPIO24	$\overline{CS4}$	TT4	V_{DD}	$\overline{HTA}$	$\overline{DBB}$	$\overline{AACK}$	$\overline{ARTRY}$	BM1	V_{DD}	$\overline{PGTA}$	$\overline{PSD\ CAS}$	TEST	HA19	V_{DD}	HA28	HA20
J	A30	GPIO25	GND	GPIO23	BCTL1	PSDA10	TT3	V_{DD}	GND	V_{DD}	$\overline{DBG}$	BM2	CLKIN	V_{DD}	BADDR27	PSDA MUX	GND	HA13	V_{DD}	HA26	HA18
K	A28	A29	A26	GND	$\overline{CS2}$	ALE	TT2	V_{DD}	CLKOUT	GND	GND	GND	GND	Res.	BADDR30	$\overline{POE}$	$\overline{PWE1}$	$\overline{PWE3}$	HA16	HA21	HA15
L	A22	A25	A27	V_{DDH}	$\overline{CS3}$	GND	GND	V_{DDH}	GND	MSC8122			GND	GND	BADDR29	BADDR28	V_{DDH}	V_{DDH}	HA11	HA14	HA12
M	A21	A24	V_{DDH}	GND	V_{DDH}	V_{DDH}	$\overline{HB\ RST}$	V_{DDH}	GND				GND	V_{DDH}	V_{DD}	GND	GND	GND	V_{DDH}	HD31	HD28
N	A20	A23	GPIO26	$\overline{PSDWE}$	$\overline{CS0}$	$\overline{HCS}$	$\overline{BG}$	$\overline{HRDS}$	GND				GND	$\overline{HBCS}$	$\overline{HWBS\ 0}$	V_{DDH}	$\overline{PWE2}$	HD24	HD29	HD30	HD26
P	A19	GND	V_{DDH}	DP0	$\overline{PSD\ VAL}$	$\overline{TEA}$	$\overline{BR}$	$\overline{TA}$	GND	GND	V_{CCSYN}	GND_{SYN}	GND	HCLKIN	$\overline{HWBS\ 1}$	$\overline{HWBS\ 2}$	$\overline{HWBS\ 3}$	HD23	HD25	HD27	HD20
R	A16	A18	A17	DP2	$\overline{TS}$	DP3	DP6	DP7	TT0	V_{DD}	V_{DD}	V_{DD}	$\overline{GBL}$	TSZ3	TSZ1	$\overline{HWBS\ 4}$	$\overline{HWBS\ 6}$	HD22	GND	V_{DDH}	HD18
T	A14	A15	GND	D30	DP1	DP4	DP5	D23	D21	TT1	D16	V_{DD}	$\overline{TBST}$	TSZ2	TSZ0	$\overline{HWBS\ 5}$	$\overline{HWBS\ 7}$	HD0	HD1	HD21	HD17
U	A13	A12	V_{DDH}	D31	D28	D26	D25	D22	D19	D17	D15	D14	D11	D9	D8	D6	D3	D2	HD2	HD19	HD16
V	A11	A10	A9	A8	D29	D27	D24	GND	D20	D18	D13	D12	D10	D7	D5	D4	D1	D0	GND	V_{DDH}	HD3
W	A6	A7	GND	GND	HD32	V_{DDH}	HD33	V_{DDH}	HD40	GND	V_{DDH}	HDST0	HDST1	GND	V_{DDH}	V_{DDH}	GND	GND	HD4	HD5	HD6
Y	A5	A4	V_{DDH}	HD34	HD37	GND	V_{DDH}	GND	HD43	V_{DDH}	GND	HD51	V_{DDH}	GND	HD58	HD60	V_{DD}	HD9	V_{DDH}	HD15	HD7
AA	A3	A2	A0	HD35	HD38	HD42	GND	HD46	V_{DDH}	GND	V_{DDH}	HD52	HD54	V_{DDH}	GND	HD59	HD63	HD10	HD12	HD14	V_{DD}
AB	V_{DD}	A1	HD36	HD39	HD41	HD44	HD45	HD47	HD48	HD49	HD50	HD53	HD55	HD56	HD57	HD61	HD62	HD8	HD11	HD13	GND

Figure 4. MSC8122 Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents signal list sorted by ball number. -

Table 1. MSC8122 Signal Listing by Ball Designator

Des.	Signal Name	Des.	Signal Name
B3	V_{DD}	C18	GPIO1/TIMER0/CHIP_ID1/$\overline{IRQ5}$/ETHTXD1
B4	GND	C19	GPIO7/TDM3RCLK/$\overline{IRQ5}$/ETHTXD3
B5	GND	C20	GPIO3/TDM3TSYN/$\overline{IRQ1}$/ETHTXD2
B6	$\overline{NMI\_OUT}$	C21	GPIO5/TDM3TDAT/$\overline{IRQ3}$/ETHRXD3
B7	GND	C22	GPIO6/TDM3RSYN/$\overline{IRQ4}$/ETHRXD2
B8	V_{DD}	D2	TDI
B9	GND	D3	EE0
B10	V_{DD}	D4	EE1
B11	GND	D5	GND
B12	V_{DD}	D6	V_{DDH}
B13	GND	D7	HCID2
B14	V_{DD}	D8	HCID3/HA8
B15	GND	D9	GND
B16	V_{DD}	D10	V_{DD}
B17	GND	D11	GND
B18	V_{DD}	D12	V_{DD}
B19	GPIO0/CHIP_ID0/$\overline{IRQ4}$/ETHTXD0	D13	GND
B20	V_{DD}	D14	V_{DD}
B21	V_{DD}	D15	V_{DD}
B22	GND	D16	GPIO31/TIMER3/SCL
C2	GND	D17	GPIO29/CHIP_ID3/ETHTX_EN
C3	V_{DD}	D18	V_{DDH}
C4	TDO	D19	GPIO4/TDM3TCLK/$\overline{IRQ2}$/ETHTX_ER
C5	$\overline{SRESET}$	D20	V_{DDH}
C6	GPIO28/UTXD/DREQ2	D21	GND
C7	HCID1	D22	GPIO8/TDM3RDAT/$\overline{IRQ6}$/ETHCOL
C8	GND	E2	TCK
C9	V_{DD}	E3	$\overline{TRST}$
C10	GND	E4	TMS
C11	V_{DD}	E5	$\overline{HRESET}$
C12	GND	E6	GPIO27/URXD/DREQ1
C13	V_{DD}	E7	HCID0
C14	GND	E8	GND
C15	GND	E9	V_{DD}
C16	GPIO30/TIMER2/TMCLK/SDA	E10	GND
C17	GPIO2/TIMER1/CHIP_ID2/$\overline{IRQ6}$	E11	V_{DD}

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
E12	GND	G6	HA17
E13	V_{DD}	G7	PWE0/PSDDQM0/PBS0
E14	GND	G8	V_{DD}
E15	GND	G9	V_{DD}
E16	V_{DD}	G10	IRQ3/BADDR31
E17	GND	G11	BM0/TC0/BNKSEL0
E18	GND	G12	ABB/IRQ4
E19	GPIO9/TDM2TSYN/IRQ7/ETHMDIO	G13	V_{DD}
E20	GPIO13/TDM2RCLK/IRQ11/ETHMDC	G14	IRQ7/INT_OUT
E21	GPIO10/TDM2TCLK/IRQ8/ETHRX_DV/ETHCRS_DV/NC	G15	ETHCRS/ETHRXD
E22	GPIO12/TDM2RSYN/IRQ10/ETHRXD1/ETHSYNC	G16	V_{DD}
F2	PORESET	G17	CS1
F3	RSTCONF	G18	BCTL0
F4	NMI	G19	GPIO15/TDM1TSYN/DREQ1
F5	HA29	G20	GND
F6	HA22	G21	GPIO17/TDM1TDAT/DACK1
F7	GND	G22	GPIO22/TDM0TCLK/DONE2/DRACK2
F8	V_{DD}	H2	HA20
F9	V_{DD}	H3	HA28
F10	V_{DD}	H4	V_{DD}
F11	GND	H5	HA19
F12	V_{DD}	H6	TEST
F13	GND	H7	PSDCAS/PGPL3
F14	V_{DD}	H8	PGTA/PUPMWAIT/PGPL4/PPBS
F15	ETHRX_CLK/ETHSYNC_IN	H9	V_{DD}
F16	ETHTX_CLK/ETHREF_CLK/ETHCLOCK	H10	BM1/TC1/BNKSEL1
F17	GPIO20/TDM1RDAT	H11	ARTRY
F18	GPIO18/TDM1RSYN/DREQ2	H12	AACK
F19	GPIO16/TDM1TCLK/DONE1/DRACK1	H13	DBB/IRQ5
F20	GPIO11/TDM2TDAT/IRQ9/ETHRX_ER/ETHTXD	H14	HTA
F21	GPIO14/TDM2RDAT/IRQ12/ETHRXD0/NC	H15	V_{DD}
F22	GPIO19/TDM1RCLK/DACK2	H16	TT4/CS7
G2	HA24	H17	CS4
G3	HA27	H18	GPIO24/TDM0RSYN/IRQ14
G4	HA25	H19	GPIO21/TDM0TSYN
G5	HA23	H20	V_{DD}

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/$\overline{CS5}$
J2	HA18	K17	ALE
J3	HA26	K18	$\overline{CS2}$
J4	V_{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V_{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V_{DDH}
J12	$\overline{DBG}$	L6	V_{DDH}
J13	V_{DD}	L7	BADDR28
J14	GND	L8	$\overline{IRQ5}$/BADDR29
J15	V_{DD}	L9	GND
J16	TT3/$\overline{CS6}$	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	$\overline{BCTL1}$/$\overline{CS5}$	L15	V_{DDH}
J19	GPIO23/TDM0TDAT/$\overline{IRQ13}$	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/$\overline{IRQ15}$	L18	$\overline{CS3}$
J22	A30	L19	V_{DDH}
K2	HA15	L20	A27
K3	HA21	L21	A25
K4	HA16	L22	A22
K5	$\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$	M2	HD28
K6	$\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$	M3	HD31
K7	$\overline{POE}$/$\overline{PSDRAS}$/PGPL2	M4	V_{DDH}
K8	$\overline{IRQ2}$/BADDR30	M5	GND
K9	Reserved	M6	GND
K10	GND	M7	GND
K11	GND	M8	V_{DD}
K12	GND	M9	V_{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{HBRST}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{TA}$
M19	GND	P16	$\overline{BR}$
M20	V_{DDH}	P17	$\overline{TEA}$
M21	A24	P18	$\overline{PSDVAL}$
M22	A21	P19	DP0/DREQ1/$\overline{EXT\_BR2}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{PWE2}$/$\overline{PSDDQM2}$/$\overline{PBS2}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{HWBS0}$/$\overline{HDBS0}$/$\overline{HWBE0}$/$\overline{HDBE0}$	R5	HD22
N9	$\overline{HBCS}$	R6	$\overline{HWBS6}$/$\overline{HDBS6}$/$\overline{HWBE6}$/$\overline{HDBE6}$/$\overline{PWE6}$/$\overline{PSDDQM6}$/$\overline{PBS6}$
N10	GND	R7	$\overline{HWBS4}$/$\overline{HDBS4}$/$\overline{HWBE4}$/$\overline{HDBE4}$/$\overline{PWE4}$/$\overline{PSDDQM4}$/$\overline{PBS4}$
N14	GND	R8	TSZ1
N15	$\overline{HRDS}$/HRW/$\overline{HRDE}$	R9	TSZ3
N16	$\overline{BG}$	R10	$\overline{IRQ1}$/$\overline{GBL}$
N17	$\overline{HCS}$	R11	V_{DD}
N18	$\overline{CS0}$	R12	V_{DD}
N19	$\overline{PSDWE}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{IRQ7}$/DP7/DREQ4
N22	A20	R16	$\overline{IRQ6}$/DP6/DREQ3
P2	HD20	R17	$\overline{IRQ3}$/DP3/DREQ2/$\overline{EXT\_BR3}$
P3	HD27	R18	$\overline{TS}$
P4	HD25	R19	$\overline{IRQ2}$/DP2/$\overline{DACK2}$/$\overline{EXT\_DBG2}$
P5	HD23	R20	A17
P6	$\overline{HWBS3}$/$\overline{HDBS3}$/$\overline{HWBE3}$/$\overline{HDBE3}$	R21	A18
P7	$\overline{HWBS2}$/$\overline{HDBS2}$/$\overline{HWBE2}$/$\overline{HDBE2}$	R22	A16
P8	$\overline{HWBS1}$/$\overline{HDBS1}$/$\overline{HWBE1}$/$\overline{HDBE1}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
T6	HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7	U21	A12
T7	HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5	U22	A13
T8	TSZ0	V2	HD3/MODCK1
T9	TSZ2	V3	V_{DDH}
T10	TBST	V4	GND
T11	V_{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	IRQ5/DP5/DACK4/EXT_BG3	V10	D10
T17	IRQ4/DP4/DACK3/EXT_DBG3	V11	D12
T18	IRQ1/DP1/DACK1/EXT_BG2	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
W15	V_{DDH}	AA9	V_{DDH}
W16	HD33/D33/reserved	AA10	HD54/D54/ETHTX_EN
W17	V_{DDH}	AA11	HD52/D52
W18	HD32/D32/reserved	AA12	V_{DDH}
W19	GND	AA13	GND
W20	GND	AA14	V_{DDH}
W21	A7	AA15	HD46/D46/ETHTXT0
W22	A6	AA16	GND
Y2	HD7	AA17	HD42/D42/ETHRXD2/reserved
Y3	HD15	AA18	HD38/D38/reserved
Y4	V_{DDH}	AA19	HD35/D35/reserved
Y5	HD9	AA20	A0
Y6	V_{DD}	AA21	A2
Y7	HD60/D60/ETHCOL/reserved	AA22	A3
Y8	HD58/D58/ETHMDC	AB2	GND
Y9	GND	AB3	HD13
Y10	V_{DDH}	AB4	HD11
Y11	HD51/D51	AB5	HD8
Y12	GND	AB6	HD62/D62
Y13	V_{DDH}	AB7	HD61/D61
Y14	HD43/D43/ETHRXD3/reserved	AB8	HD57/D57/ETHRX_ER
Y15	GND	AB9	HD56/D56/ETHRX_DV/ETHCRS_DV
Y16	V_{DDH}	AB10	HD55/D55/ETHTX_ER/reserved
Y17	GND	AB11	HD53/D53
Y18	HD37/D37/reserved	AB12	HD50/D50
Y19	HD34/D34/reserved	AB13	HD49/D49/ETHTXD3/reserved
Y20	V_{DDH}	AB14	HD48/D48/ETHTXD2/reserved
Y21	A4	AB15	HD47/D47/ETHTXD1
Y22	A5	AB16	HD45/D45
AA2	V_{DD}	AB17	HD44/D44
AA3	HD14	AB18	HD41/D41/ETHRXD1
AA4	HD12	AB19	HD39/D39/reserved
AA5	HD10	AB20	HD36/D36/reserved
AA6	HD63/D63	AB21	A1
AA7	HD59/D59/ETHMDIO	AB22	V_{DD}
AA8	GND		

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8122 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8122.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core and PLL supply voltage	V_{DD}	–0.2 to 1.6	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	–0.2 to 4.0	V
Maximum operating temperature: • Standard range • Extended range	T_J	 90 105	 °C °C
Minimum operating temperature • Standard range • Extended range	T_J	 0 –40	 °C °C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core and PLL supply voltage: • Standard — 400 MHz — 500 MHz • Reduced (300 and 400 MHz)	V_{DD} V_{CCSYN}	 1.14 to 1.26 1.16 to 1.24 1.07 to 1.13	 V V V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range: • Standard • Extended	 T_J T_J	 0 to 90 –40 to 105	 °C °C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8122 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8122

Characteristic	Symbol	FC-PBGA 20 × 20 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	26	21	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	19	15	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	9		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.9		°C/W
Junction-to-package-top[6]	Ψ_{JT}	1		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8122. The measurements in **Table 5** assume the following system conditions:

- T_A = 25 °C
- V_{DD} =
  - — 300/400 MHz 1.1 V nominal = 1.07–1.13 V_{DC}
  - — 400 MHz 1.2 V nominal = 1.14–1.26 V_{DC}
  - — 500 MHz 1.2 V nominal = 1.16–1.24 V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD}.

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	—	3.465	V
Input low voltage[1]	V_{IL}	GND	0	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.8	V
Input leakage current, V_{IN} = V_{DDH}	I_{IN}	–1.0	0.09	1	µA
Tri-state (high impedance off state) leakage current, V_{IN} = V_{DDH}	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, V_{IL} = 0.8 V[2]	I_L	–1.0	0.09	1	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–1.0	0.09	1	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0	0.4	V
V_{CCSYN} PLL supply current	I_{VCCSYN}	—	2	4	mA
Internal supply current: • Wait mode • Stop mode	 I_{DDW} I_{DDS}	 — —	 375[3] 290[3]	 — —	 mA mA
Typical power 400 MHz at 1.2 V[4]	P	—	1.15	—	W

Notes:
1. See **Figure 5** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.2 V core at 25°C junction temperature.
4. The typical power values were measured using an EFR code with the device running at a junction temperature of 25°C. No peripherals were enabled and the ICache was not enabled. The source code was optimized to use all the ALUs and AGUs and all four cores. It was created using CodeWarrior® 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Chapter 4** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

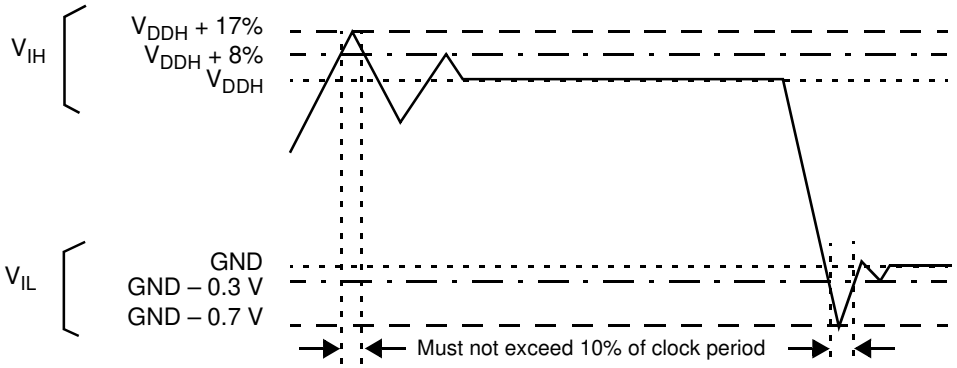


Figure 5. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.1 Output Buffer Impedances

Table 6. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	50
Memory controller	50
Parallel I/O	50
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8122 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 11** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DD} levels and then the V_{DDH} levels (see **Figure 7**).
- CLKIN should start toggling at least 16 cycles (starting after V_{DDH} reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 6** and **Figure 7**).
- CLKIN must not be pulled high during V_{DDH} power-up. CLKIN can toggle during this period.

Note: See **Section 3.1** for start-up sequencing recommendations and **Section 3.2** for power supply design recommendations.

The following figures show acceptable start-up sequence examples. **Figure 6** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 7** shows a sequence in which V_{DDH} is raised after V_{DD} and CLKIN begins to toggle as V_{DDH} rises.

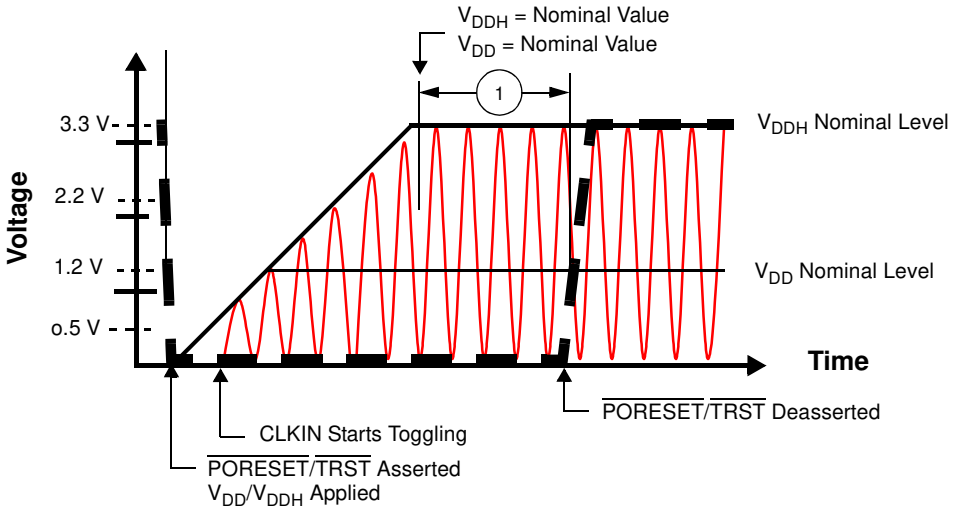


Figure 6. Start-Up Sequence: V_{DD} and V_{DDH} Raised Together

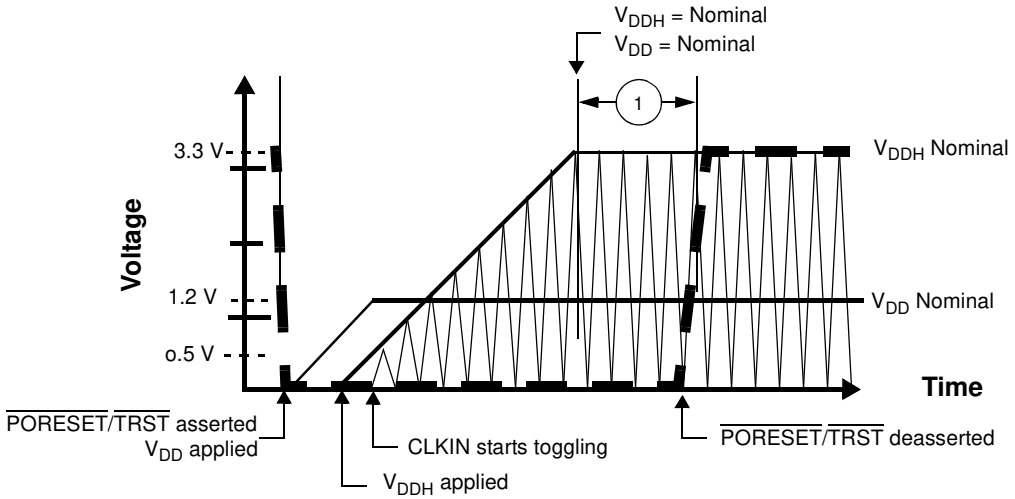


Figure 7. Start-Up Sequence: V_{DD} Raised Before V_{DDH} with CLKIN Started with V_{DDH}

In all cases, the power-up sequence must follow the guidelines shown in **Figure 8**.

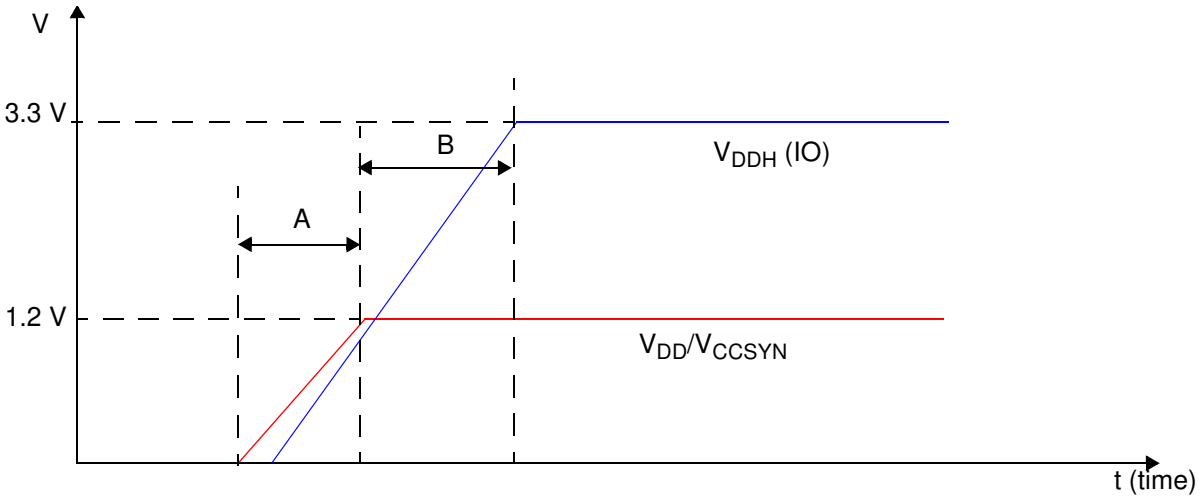


Figure 8. Power-Up Sequence for V_{DDH} and V_{DD}/V_{CCSYN}

The following rules apply:

1. During time interval A, V_{DDH} should always be equal to or less than the V_{DD}/V_{CCSYN} voltage level. The duration of interval A should be kept below 10 ms.
2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz
Core frequency	300/400/500
Reference frequency (REFCLK)	100/133/166
Internal bus frequency (BLCK)	100/133/166
DSI clock frequency (HCLKIN) • Core frequency = 300 MHz • Core frequency = 400/500 MHz	 HCLKIN ≤ (min{70 MHz, CLKOUT}) HCLKIN ≤ (min{100 MHz, CLKOUT})
External clock frequency (CLKIN or CLKOUT)	100/133/166

Table 8. Clock Frequencies

Characteristics	Symbol	300 MHz Device		400 MHz Device		500 MHz Device	
		Min	Max	Min	Max	Min	Max
CLKIN frequency	F_{CLKIN}	20	100	20	133.3	20	166.7
BCLK frequency	F_{BCLK}	40	100	40	133.3	40	166.7
Reference clock (REFCLK) frequency	F_{REFCLK}	40	100	40	133.3	40	166.7
Output clock (CLKOUT) frequency	F_{CLKOUT}	40	100	40	133.3	40	166.7
SC140 core clock frequency	F_{CORE}	200	300	200	400	200	500
Note: The rise and fall time of external clocks should be 3 ns maximum							

Table 9. System Clock Parameters

Characteristic	Min	Max	Unit
Phase jitter between BCLK and CLKIN	—	0.3	ns
CLKIN frequency	20	see **Table 8**	MHz
CLKIN slope	—	3	ns
CLKIN period jitter[1]	—	150	ps
CLKIN jitter spectrum	150	—	KHz
PLL input clock (after predivider)	20	100	MHz
PLL output frequency (VCO output) • 300 MHz core • 400 MHz core • 500 MHz core	800	 1200 1600 2000	MHz MHz MHz MHz
CLKOUT frequency jitter[1]	—	200	ps
CLKOUT phase jitter[1] with CLKIN phase jitter of ±100 ps.	—	500	ps

Notes: **1.** Peak-to-peak.
2. Not tested. Guaranteed by design.

2.5.4 Reset Timing

The MSC8122 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8122 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.

Table 10. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8122 and configures various attributes of the MSC8122. On $\overline{\text{PORESET}}$, the entire MSC8122 device is reset. SPLL states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when $\overline{\text{PORESET}}$ is asserted.
External hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8122. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigured. These features are defined in the 32-bit hard reset configuration word described in *Hard Reset Configuration Word* section of the *Reset* chapter in the *MSC8122 Reference Manual*.
External soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8122 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8122 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the SC140 extended cores are reset, and system configuration is maintained.
Software watchdog reset	Internal	When the MSC8122 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC8122 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.

Table 11 summarizes the reset actions that occur as a result of the different reset sources.

Table 11. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog or Bus Monitor)	External	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.5.4.1** for details).	Yes	No	No	No
SPLL state reset	Yes	No	No	No
System reset configuration write through the DSI	Yes	No	No	No
System reset configuration write though the system bus	Yes	Yes	No	No
HRESET driven	Yes	Yes	No	No
SIU registers reset	Yes	Yes	No	No
IPBus modules reset (TDM, UART, Timers, DSI, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
SRESET driven	Yes	Yes	Yes	Depends on command
SC140 extended cores reset	Yes	Yes	Yes	Yes
MQBS reset	Yes	Yes	Yes	Yes

2.5.4.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after V_{DD} and V_{DDH} are both at their nominal levels.

2.5.4.2 Reset Configuration

The MSC8122 has two mechanisms for writing the reset configuration:

- Through the direct slave interface (DSI)
- Through the system bus. When the reset configuration is written through the system bus, the MSC8122 acts as a configuration master or a configuration slave. If configuration slave is selected, but no special configuration word is written, a default configuration word is applied.

Fourteen signal levels (see **Chapter 1** for signal description details) are sampled on PORESET deassertion to define the Reset Configuration Mode and boot and operating conditions:

- RSTCONF
- CNFGS
- DSISYNC
- DSI64
- CHIP_ID[0–3]
- BM[0–2]
- SWTE
- MODCK[1–2]

2.5.4.3 Reset Timing Tables

Table 12 and **Figure 9** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

Table 12. Timing for a Reset Configuration Write through the DSI or System Bus

No.	Characteristics	Expression	Min	Max	Unit
1	Required external PORESET duration minimum • CLKIN = 20 MHz • CLKIN = 100 MHz (300 MHz core) • CLKIN = 133 MHz (400 MHz core) • CLKIN = 166 MHz (500 MHz core)	16/CLKIN	 800 160 120 96	 — — — —	 ns ns ns ns
2	Delay from deassertion of external PORESET to deassertion of internal PORESET • CLKIN = 20 MHz to 166 MHz	1024/CLKIN	 6.17	 51.2	 µs
3	Delay from de-assertion of internal PORESET to SPLL lock • CLKIN = 20 MHz (RDF = 1) • CLKIN = 100 MHz (RDF = 1) (300 MHz core) • CLKIN = 133 MHz (RDF = 2) (400 MHz core) • CLKIN = 166 MHz (RDF = 2) (500 MHz core)	6400/(CLKIN/RDF) (PLL reference clock-division factor)	 320 64 96 77	 320 64 96 77	 µs µs µs µs
5	Delay from SPLL to HRESET deassertion • REFCLK = 40 MHz to 166 MHz	512/REFCLK	3.08	12.8	µs
6	Delay from SPLL lock to SRESET deassertion • REFCLK = 40 MHz to 166 MHz	515/REFCLK	3.10	12.88	µs
7	Setup time from assertion of RSTCONF, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2] before deassertion of PORESET		3	—	ns
8	Hold time from deassertion of PORESET to deassertion of RSTCONF, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2]		5	—	ns
Note:	Timings are not tested, but are guaranteed by design.				

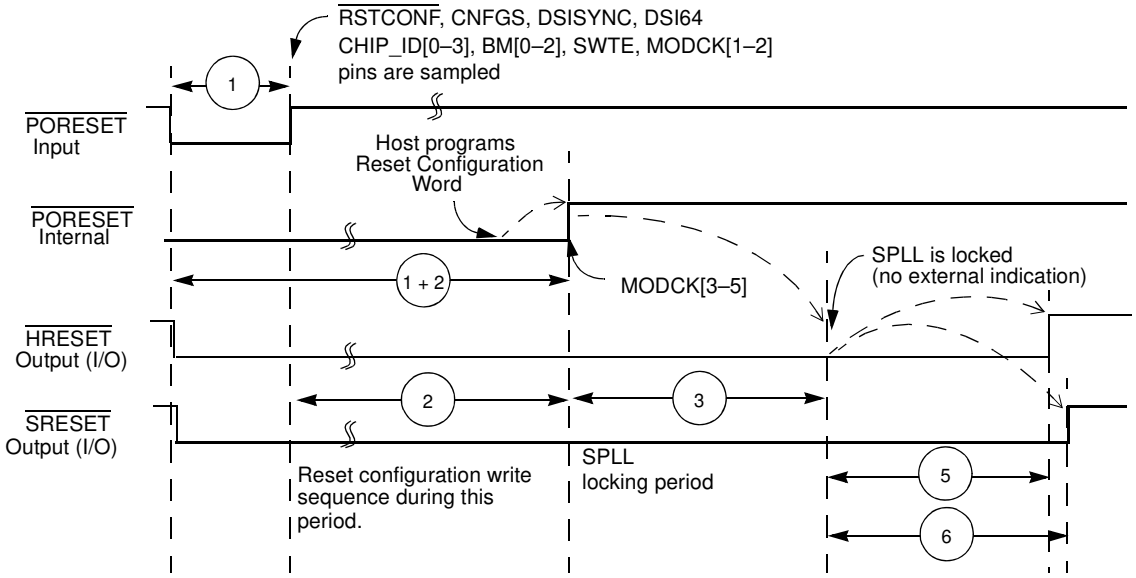


Figure 9. Timing Diagram for a Reset Configuration Write

2.5.5 System Bus Access Timing

2.5.5.1 Core Data Transfers

Generally, all MSC8122 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 13** shows.

Table 13. Tick Spacing for Memory Controller Signals

BCLK/SC140 clock	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:4, 1:6, 1:8, 1:10	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:3	1/6 REFCLK	1/2 REFCLK	4/6 REFCLK
1:5	2/10 REFCLK	1/2 REFCLK	7/10 REFCLK

Figure 10 is a graphical representation of **Table 13**.

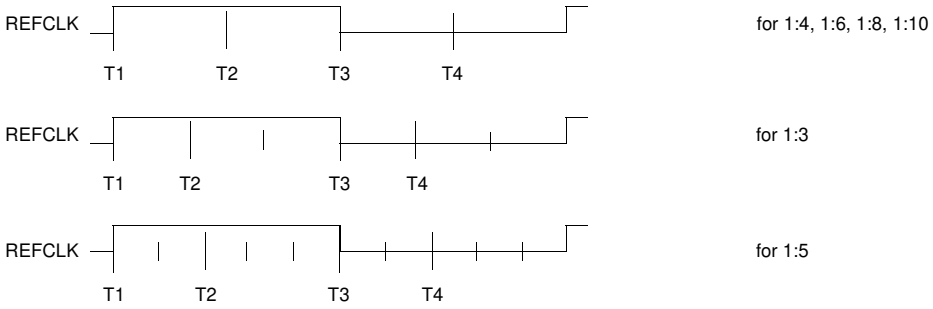


Figure 10. Internal Tick Spacing for Memory Controller Signals

The UPM machine and GPCM machine outputs change on the internal tick selected by the memory controller configuration. The AC timing specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

Table 14. AC Timing for SIU Inputs

No.	Characteristic	Value for Bus Speed in MHz				Units
		Ref = CLKIN			Ref = CLKOUT	
		1.1 V	1.2 V	1.2 V	1.2 V	
		100/ 133	133	166	133	
10	Hold time for all signals after the 50% level of the REFCLK rising edge	0.5	0.5	0.5	0.5	ns
11a	$\overline{\text{ARTRY}}$/$\overline{\text{ABB}}$ set-up time before the 50% level of the REFCLK rising edge	3.1	3.0	3.0	3.0	ns
11b	$\overline{\text{DBG}}$/$\overline{\text{DBB}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{TC}}$ set-up time before the 50% level of the REFCLK rising edge	3.6	3.3	3.3	3.3	ns
11c	$\overline{\text{AACK}}$ set-up time before the 50% level of the REFCLK rising edge	3.0	2.9	2.9	2.9	ns
11d	$\overline{\text{TA}}$/$\overline{\text{TEA}}$/$\overline{\text{PSDVAL}}$ set-up time before the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 3.5 4.4	 3.4 4.0	 3.4 4.0	 3.4 4.0	 ns ns
12	Data bus set-up time before REFCLK rising edge in Normal mode • Data-pipeline mode • Non-pipeline mode	 1.9 4.2	 1.8 4.0	 1.7 4.0	 1.8 4.0	 ns ns
13[1]	Data bus set-up time before the 50% level of the REFCLK rising edge in ECC and PARITY modes • Data-pipeline mode • Non-pipeline mode	 2.0 8.2	 2.0 7.3	 2.0 7.3	 2.0 7.3	 ns ns
14[1]	DP set-up time before the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 2.0 7.9	 2.0 6.1	 2.0 6.1	 2.0 6.1	 ns ns
15a	$\overline{\text{TS}}$ and Address bus set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 4.2 5.5	 3.8 5.0	 3.8 5.0	 3.8 5.0	 ns ns
15b	Address attributes: TT/$\overline{\text{TBST}}$/TSZ/$\overline{\text{GBL}}$ set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 3.7 4.8	 3.5 4.4	 3.5 4.4	 3.5 4.4	 ns ns
16	PUPMWAIT signal set-up time before the 50% level of the REFCLK rising edge	3.7	3.7	3.7	3.7	ns
17	$\overline{\text{IRQx}}$ setup time before the 50% level; of the REFCLK rising edge[3]	4.0	4.0	4.0	4.0	ns
18	$\overline{\text{IRQx}}$ minimum pulse width[3]	6.0 + T_{REFCLK}	6.0 + T_{REFCLK}	6.0 + T_{REFCLK}	6.0 + T_{REFCLK}	ns

Notes:
1. Timings specifications 13 and 14 in non-pipeline mode are more restrictive than MSC8102 timings.
2. Values are measured from the 50% TTL transition level relative to the 50% level of the REFCLK rising edge.
3. Guaranteed by design.

Table 15. AC Timing for SIU Outputs

No.	Characteristic	Value for Bus Speed in MHz[3]				Units
		Ref = CLKIN			Ref = CLKOUT	
		1.1 V	1.2 V	1.2 V	1.2 V	
		100/133	133	166	100/133	
30[2]	Minimum delay from the 50% level of the REFCLK for all signals	0.9	0.8	0.8	1.0	ns
31	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ max delay from the 50% level of the REFCLK rising edge	6.0	4.9	4.9	5.8	ns
32a	Address bus max delay from the 50% level of the REFCLK rising edge • Multi-master mode (SIUBCR[EBM] = 1) • Single-master mode (SIUBCR[EBM] = 0)	 6.4 5.3	 5.5 4.2	 5.5 3.9	 6.4 5.1	 ns ns
32b	Address attributes: TT[0–1]/$\overline{\text{TBST}}$/TSZ/$\overline{\text{GBL}}$ max delay from the 50% level of the REFCLK rising edge	6.4	5.1	5.1	6.0	ns
32c	Address attributes: TT[2–4]/TC max delay from the 50% level of the REFCLK rising edge	6.9	5.7	5.7	6.6	ns
32d	BADDR max delay from the 50% level of the REFCLK rising edge	5.2	4.2	4.2	5.1	ns
33a	Data bus max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 4.8 7.1	 3.9 6.1	 3.7 6.1	 4.8 7.0	 ns ns
33b	DP max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 6.0 7.5	 5.3 6.5	 5.3 6.5	 6.2 7.4	 ns ns
34	Memory controller signals/ALE/$\overline{\text{CS}}$[0–4] max delay from the 50% level of the REFCLK rising edge	5.1	4.2	3.9	5.1	ns
35a	$\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{DBB}}$ max delay from the 50% level of the REFCLK rising edge	6.0	4.7	4.7	5.6	ns
35b	$\overline{\text{AACK}}/\overline{\text{ABB}}/\overline{\text{TS}}/\overline{\text{CS}}$[5–7] max delay from the 50% level of the REFCLK rising edge	5.5	4.5	4.5	5.4	ns

Notes:

1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level and assume a 20 pF load except where otherwise specified.
2. Except for specification 30, which is specified for a 10 pF load, all timings in this table are specified for a 20 pF load. Decreasing the load results in a timing decrease at the rate of 0.3 ns per 5 pF decrease in load. Increasing the load results in a timing increase at the rate of 0.15 ns per 5 pF increase in load.
3. The maximum bus frequency depends on the mode:
   • In 60x-compatible mode connected to another MSC8122 device, the frequency is determined by adding the input and output longest timing values, which results in the total delay for 20 pF output capacitance. You must also account for other influences that can affect timing, such as on-board clock skews, on-board noise delays, and so on.
   • In single-master mode, the frequency depends on the timing of the devices connected to the MSC8122.
   • To achieve maximum performance on the bus in single-master mode, disable the $\overline{\text{DBB}}$ signal by writing a 1 to the SIUMCR[BDD] bit. See the SIU chapter in the *MSC8122 Reference Manual* for details.

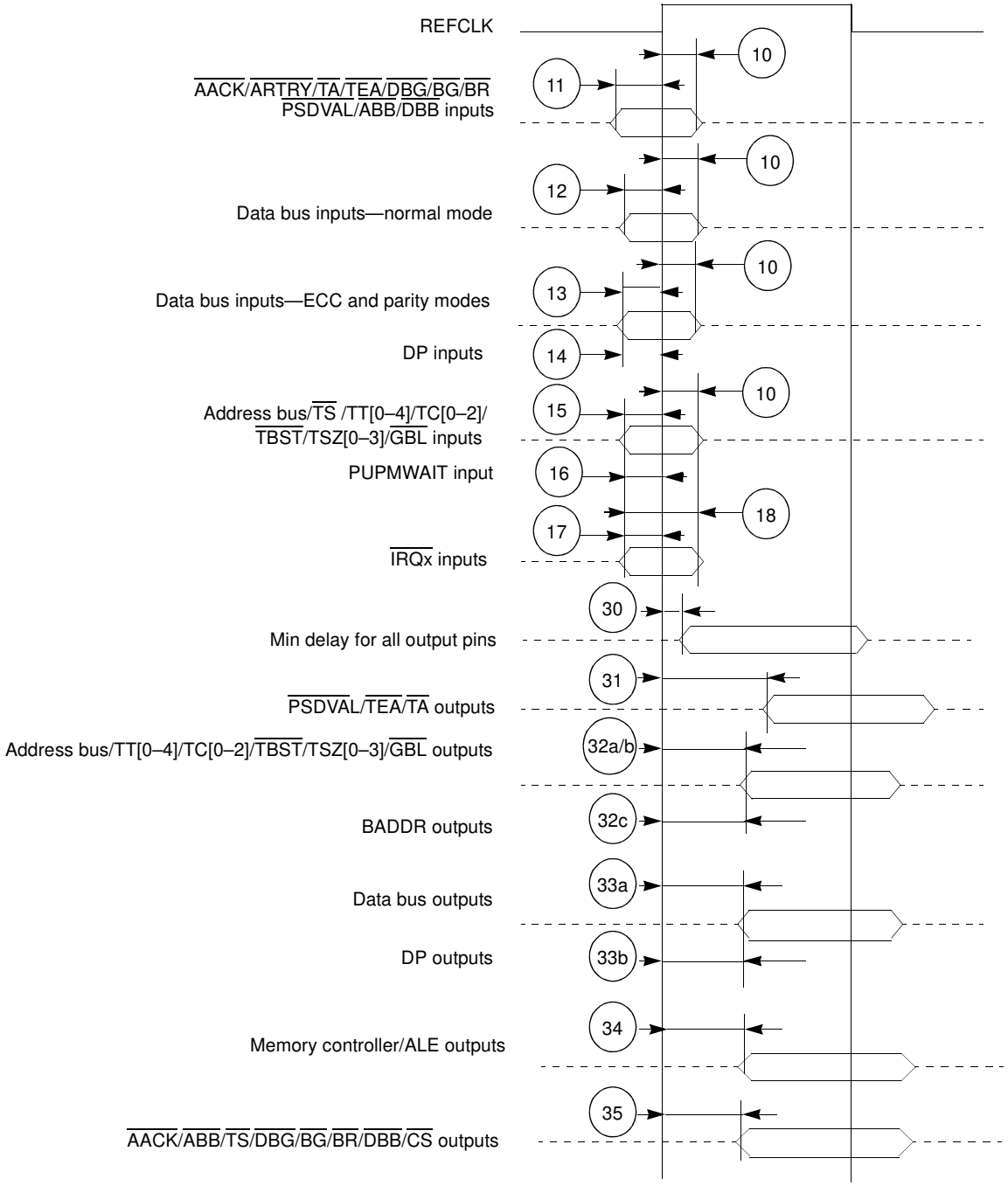


Figure 11. SIU Timing Diagram