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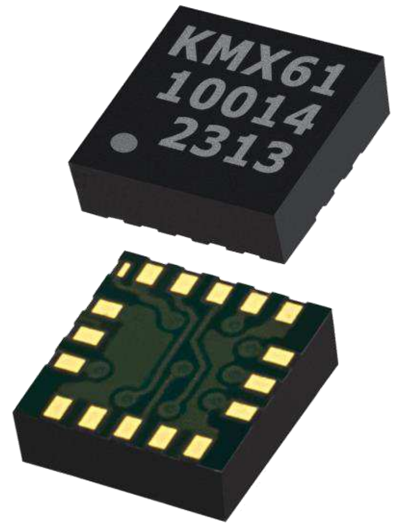
	Digital Tri-axis Magnetometer/ Tri-axis Accelerometer Specifications	**PART NUMBER:** **KMX61-1021** **Rev. 1.0** **July 14**

Product Description



KMX61 is a 6 Degrees-of-Freedom inertial sensor system that features 14-bit digital outputs accessed through I^2C communication. The KMX61 sensor consists of a tri-axial magnetometer plus a tri-axial accelerometer coupled with an ASIC. It is packaged in a 3x3x0.9mm Land Grid Array (LGA) package. The ASIC is realized in standard 0.18um CMOS technology and features flexible user programmable ±2g/±4g/±8g full scale range for the accelerometer. Accelerometer and Magnetometer data can be accumulated in an internal 512 byte FIFO buffer and transmitted to the application processor.

Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias and sensitivity adjustment, as well as temperature compensation.

Magnetic sensing is based on the principle of magnetic impedance. The magnetic sensor detects very small magnetic fields by passing an electric pulse through a special electron spin aligned amorphous wire. Due to the high Curie temperature of the wire, the sensor's thermal performance shows excellent stability.

Noise performance is excellent with bias stability over temperature. Bias errors resulting from assembly can be trimmed digitally by the user. These sensors can accept supply voltages between 1.8V and 3.3V, and digital communication voltages between 1.8 and 3.3V.

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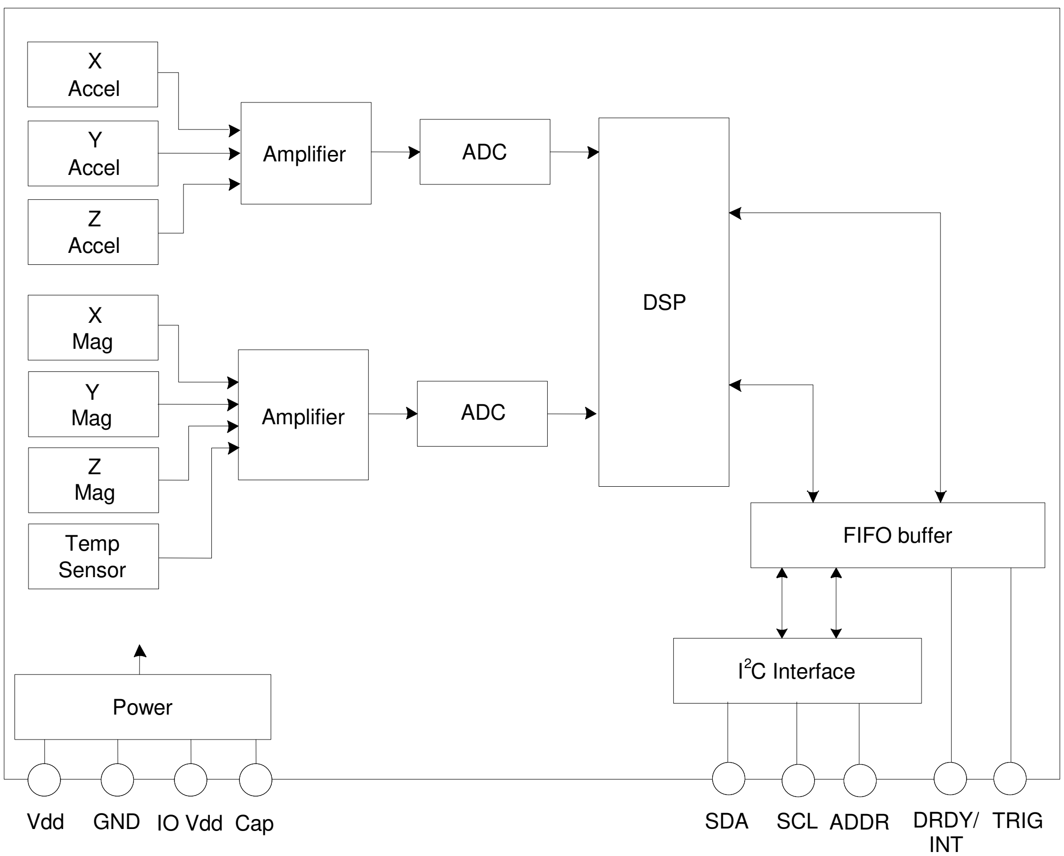
Functional Diagram



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Product Specifications

Note: Specifications are for operation at Vdd = 2.5V and T = 25ºC unless stated otherwise

Table 1. Magnetometer

Parameters	Units	Value
Operating Temperature Range	ºC	-40 to 85
Full Scale Range	± μT	1200
Digital Bit Depth	bits	14
Offset at Zero Magnetic Field	± μT	0
Offset Temperature Coefficient	± μT/ºC	0.3
Magnetic Sensitivity	± μT/LSB	0.146
Sensitivity Temperature Coefficient.	± %/ºC	0.05
Integral Non-Linearity	% of FS	0.5
Noise[1] (at 50Hz ODR)	μT (RMS)	0.4
Cross Axis Sensitivity	% of FS	-1.1 (S_{xy}) 3.6 (S_{xz}) 2.1 (S_{yx}) 0.3 (S_{yz}) 0.8 (S_{zx}) -1.7 (S_{zy})
Maximum Exposed Field[2]	μT	1,000,000

Notes:

1. See plot below for noise performance over ODR for all three axes.
2. No permanent effect on Zero Magnetic Field Offset.

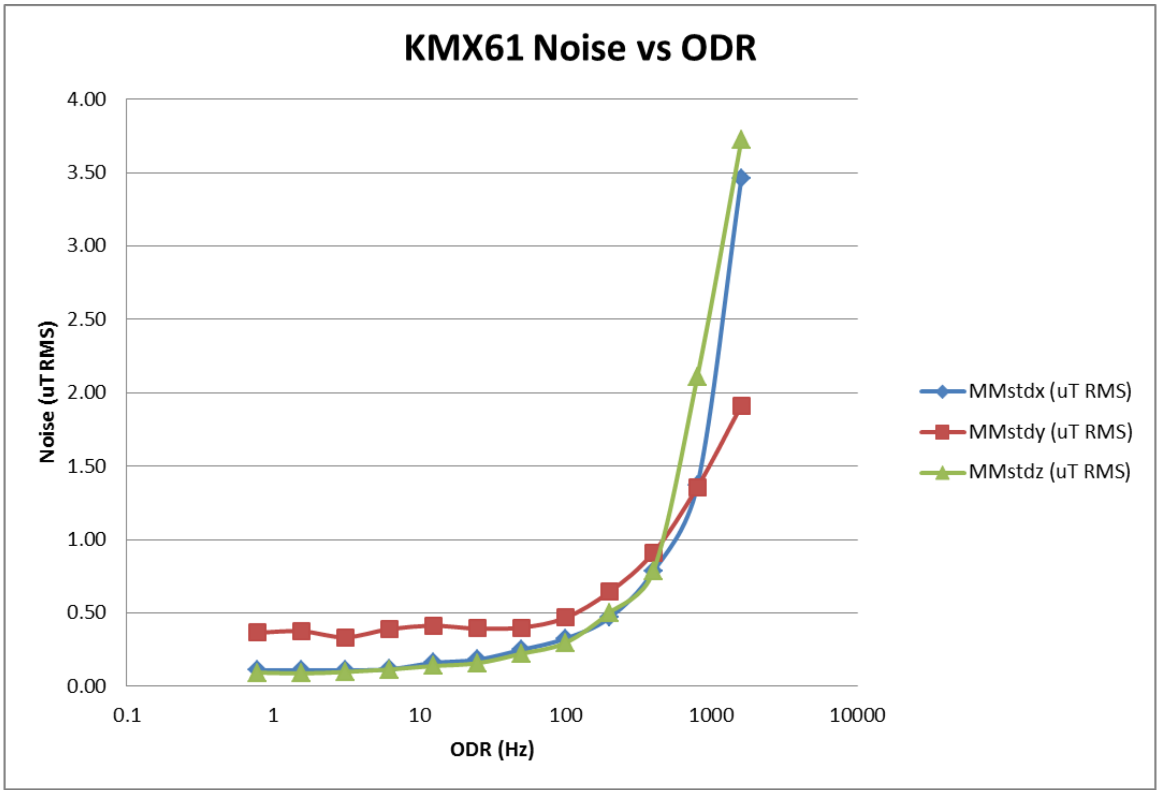

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Table 2. Accelerometer

Parameters		Units	Value
Operating Temperature Range		ºC	-40 to 85
Full Scale Range	GSEL1=0, GSEL=0	g	± 2
	GSEL1=0, GSEL0=1		± 4
	GSEL1=1, GSEL0=0		± 8
Digital Bit Depth[4]			12 or 14
Zero-g Offset		mg	±25
Zero-g Offset Temperature Coefficient		± mg/ºC	0.25
Sensitivity	GSEL1=0, GSEL=0 (± 2g)	mg/LSB	0.98
	GSEL1=0, GSEL0=1 (± 4g)		1.95
	GSEL1=1, GSEL0=0 (± 8g)		3.91
Sensitivity Temperature Coefficient		± %/ºC	0.03
Positive Self Test Output change on Activation		g	1.4 (x) 0.7 (y) 0.6 (z)
Negative Self Test Output change on Activation		g	-0.15 (x) -0.4 (y) -0.4 (z)
Sensor Mechanical Resonance (-3dB)[1]		Hz	3500 (xy) 1800 (z)
Integral Non-Linearity		% of FS	1
Cross Axis Sensitivity[2]		± %	0.5 (S_{xy}) -0.4 (S_{xz}) 0.2 (S_{yx}) -0.2 (S_{yz}) 0.2 (S_{zx}) 0.7 (S_{zy})
Noise[3] (at 50Hz)		mg (RMS)	1.25

Notes:
1. Resonance as defined by the dampened mechanical sensor.
2. As measured in a test socket. The cross axis sensitivity that is measured is the by-product of positional inaccuracies at all stages of test and assembly.
3. See plot below for noise performance over ODR for all three axes.
4. 14 bit depth for 8g mode available, and 12 bit depth for 2g, 4g, and 8g

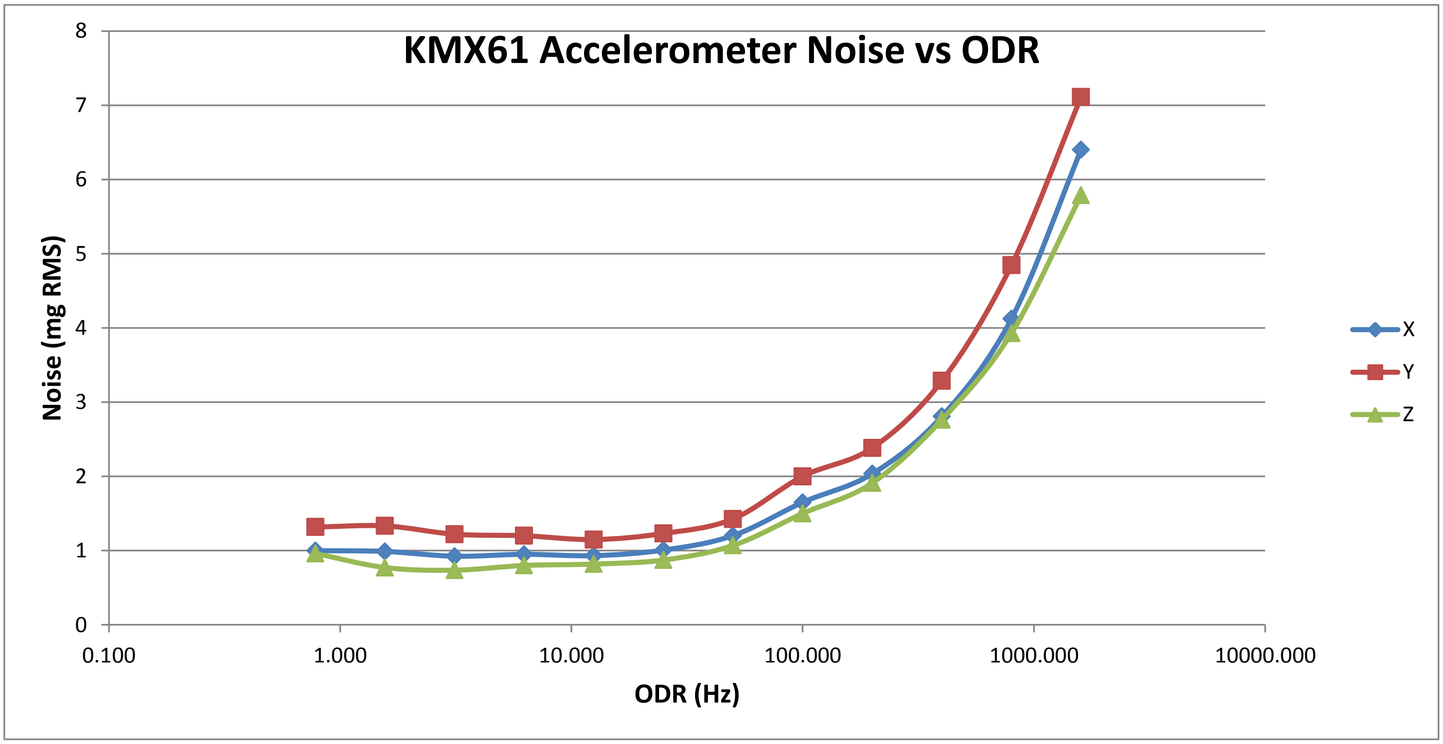
KMX61 Accelerometer Noise vs ODR
Noise (mg RMS)
ODR (Hz)
0
1
2
3
4
5
6
7
8
0.100
1.000
10.000
100.000
1000.000
10000.000
X
Y
Z

Table 3. Electrical

Parameters		Units	Min	Typical	Max
Supply Voltage (Vdd)	Operating	V	1.8	2.5	3.3
I/O Pads Supply Voltage (Vio)		V	1.7		Vdd
Current Consumption	Operating (mag + accel)	µA		400	
	Magnetometer only			300	
	Accelerometer only			150	
	Standby			1	5
Output Low Voltage[1]		V	-	-	0.3 * Vio
Output High Voltage		V	0.9 * Vio	-	-
Input Low Voltage		V	-	-	0.2 * Vio
Input High Voltage		V	0.8 * Vio	-	-
I^2C Communication Rate[2,3]		MHz	0.1	0.4	3.4
Output Data Rate		Hz	0.781	100	1600
Filter -3dB Cutoff[4]		Hz		ODR/2	
Internal Oscillator Tolerance		%	-10		10

Notes:
1. Assuming I^2C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA.
2. Assuming max bus capacitance load of 20pF.
3. The I^2C bus supports Standard-Mode, Fast-Mode and High Speed Mode.
4. User selectable via ODR control register setting

KMX61 Transition Timing Diagram

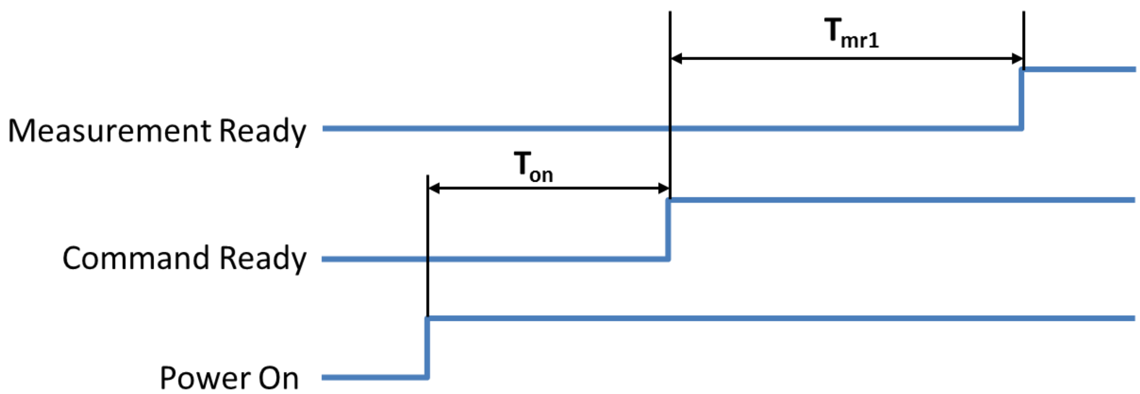

Table 4. Transition Timing

Symbol	Description	Units	Min	Typ	Max
T_{on}	Power On to Ready State (Power on Reset Time)	ms		10	
T_{mr1}	Inactive to Active State (Measurement Ready varies by ODR)	ms		Table 5	

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KMX61 Start Up Time

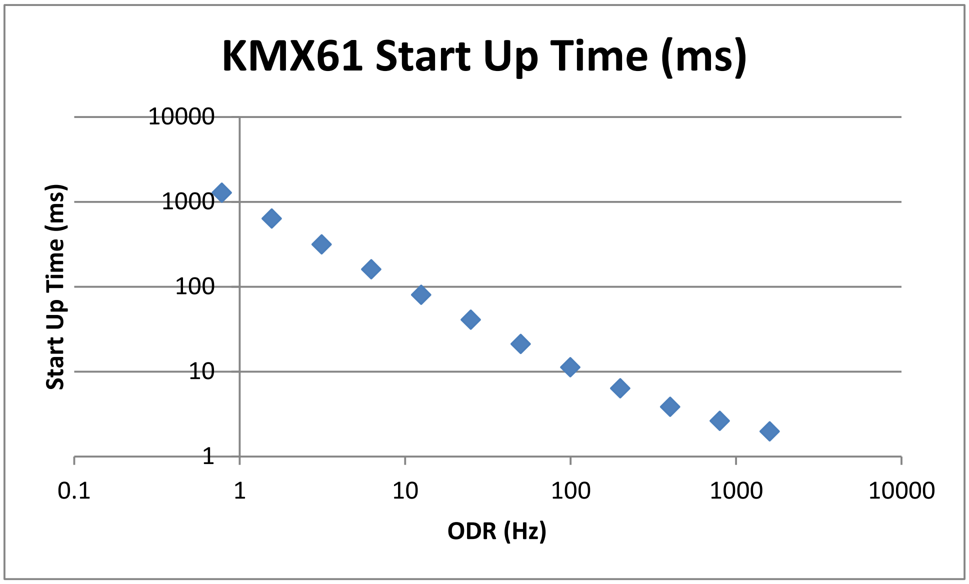

Table 5. Start Up Time

Time from sensor enable to Valid output.

KMX61 Start Up Time (ms)	
ODR (Hz)	Time (ms)
1600	2.0
800	2.6
400	3.8
200	6.3
100	11
50	21
25	40
12.5	79
6.25	158
3.125	312
1.5625	629
0.78125	1260

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KMX61 I^2C Timing Diagram

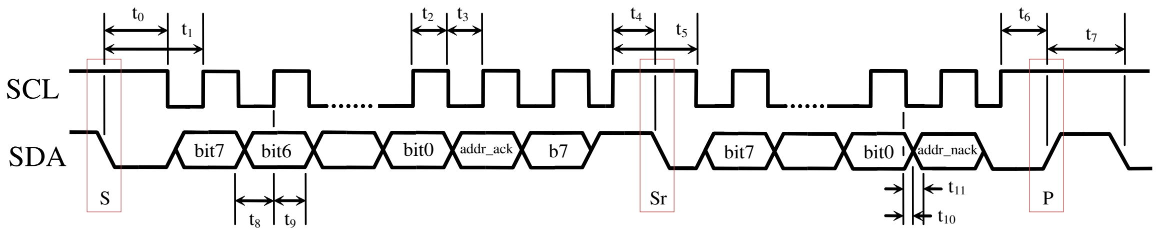

Table 6. I^2C Timing (Fast Mode)

Number	Description	MIN	MAX	Units
t_0	SDA low to SCL low transition (Start event)	50	-	ns
t_1	SDA low to first SCL rising edge	100	-	ns
t_2	SCL pulse width: high	100	-	ns
t_3	SCL pulse width: low	100	-	ns
t_4	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: high during a S/Sr/P event	100	-	ns
t_6	SCL high before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: high	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I^2C CLK	2.5	-	us

Table 7. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (Vdd)	Absolute Limits	V	-0.3	-	3.6
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Application Schematic

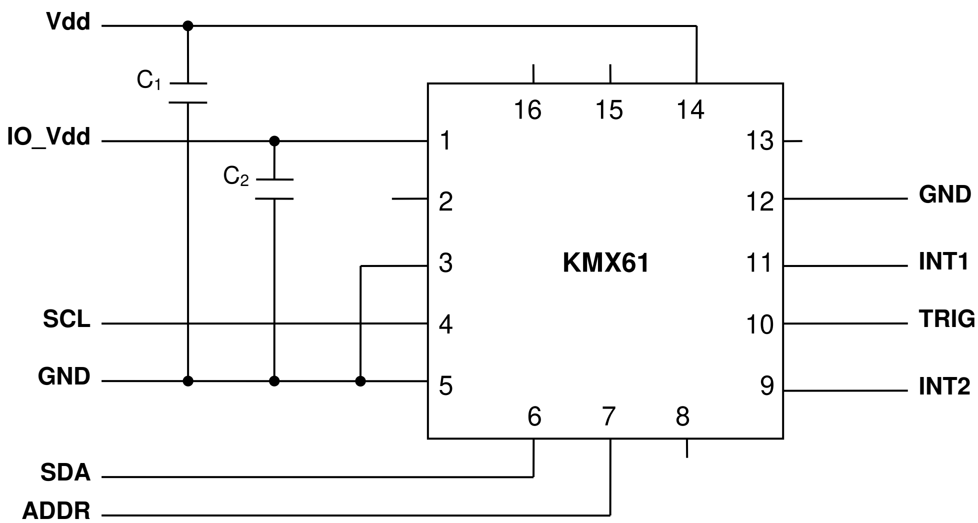

Table 8. KMX61 Pin Descriptions

Pin	Name	Description
1	IO Vdd	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	Reserved	Leave this pin unconnected or alternatively couple this pin to ground with a 1 uF ceramic capacitor.
3	GND	Ground
4	SCL	I^2C Serial Clock
5	GND	Ground
6	SDA	I^2C Serial Data
7	ADDR	I^2C Address pin .This pin can be connected to IO_VDD or GND to determine the I2C Device Address.
8	NC	Not Internally Connected
9	INT2	Physical Interrupt 2
10	TRIG	Trigger input for buffer. Connect to GND if not used.
11	INT1	Physical Interrupt 1
12	GND	Ground
13	NC	Not Internally Connected
14	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected
16	NC	Not Internally Connected

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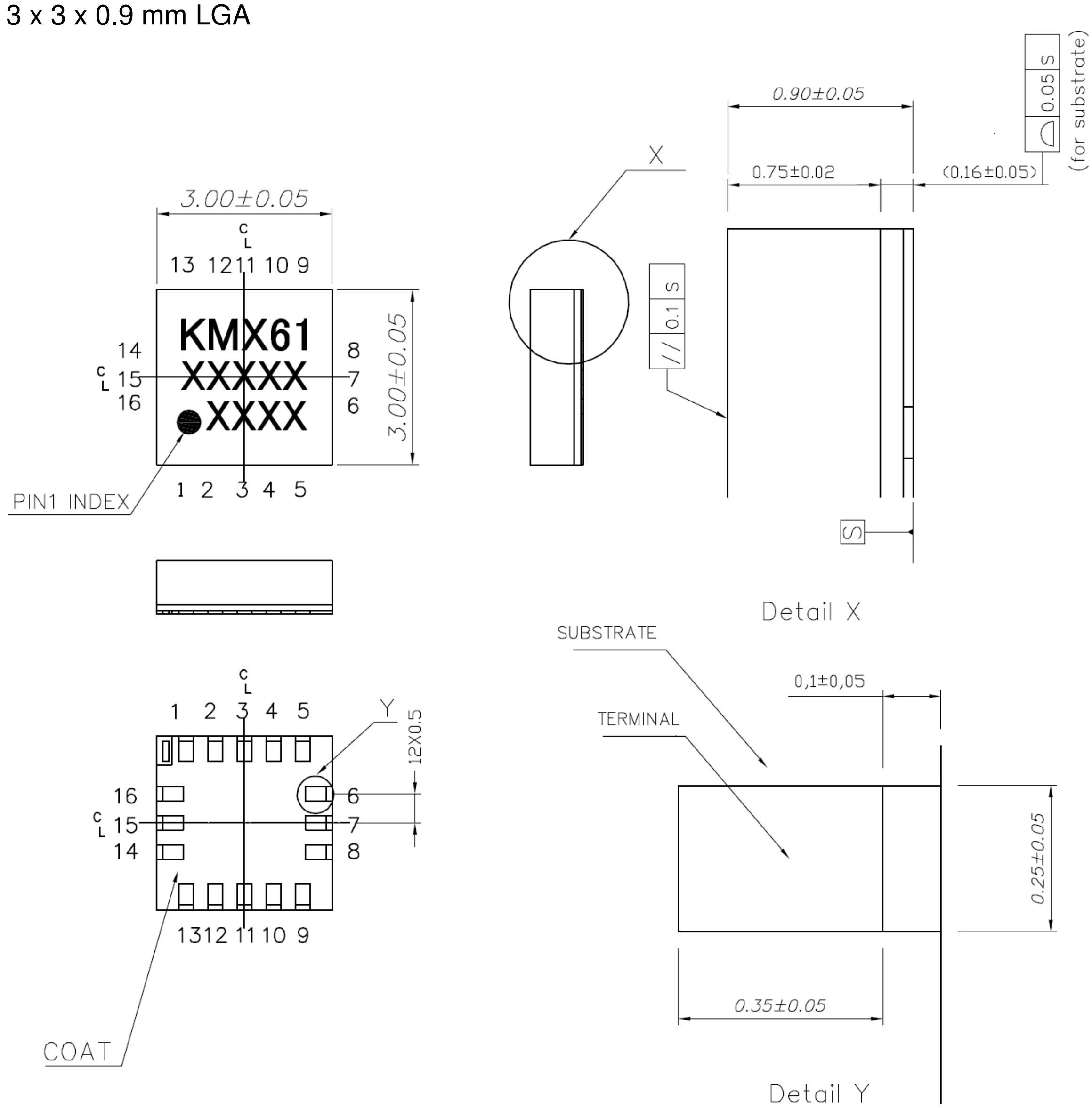
Package Dimensions and Orientation:

Dimensions

3 x 3 x 0.9 mm LGA



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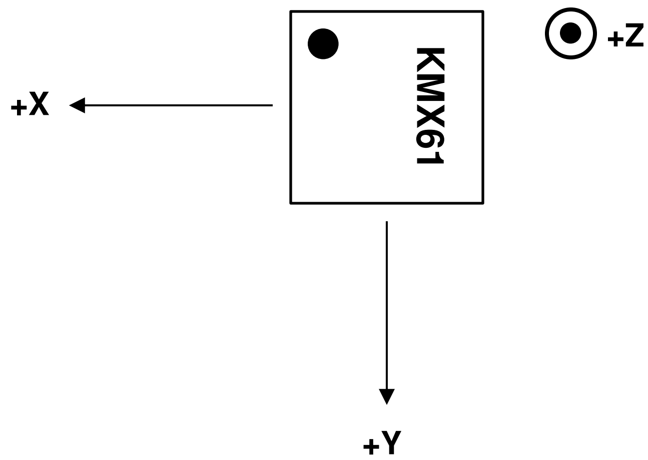
Orientation

When device is moved in +X, +Y, or +Z direction, the corresponding accelerometer output will increase. When the +X, +Y, or +Z arrow is directed toward North, the magnetometer output of that axis is positive.



Board Layout

Please avoid mounting this product on the part in which magnetic field disturbance exists, such as near any parts containing ferrous materials.

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KMX61 Digital Interface

The Kionix KMX61 digital sensor has the ability to communicate on the I^2C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system processors. The I2C interface is compliant with high-speed mode, fast mode and standard mode I2C protocols.

The serial interface terms and descriptions as indicated in Table 8 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 8. Serial Interface Terminologies

I^2C Serial Interface

As previously mentioned, the KMX61 has the ability to communicate on an I^2C bus. I^2C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The system Master provides the serial clock signal and addresses Slave devices on the bus. The KMX61 always operates as a Slave device during standard Master-Slave I^2C operation.

I^2C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I^2C bus is considered free when both lines are high.

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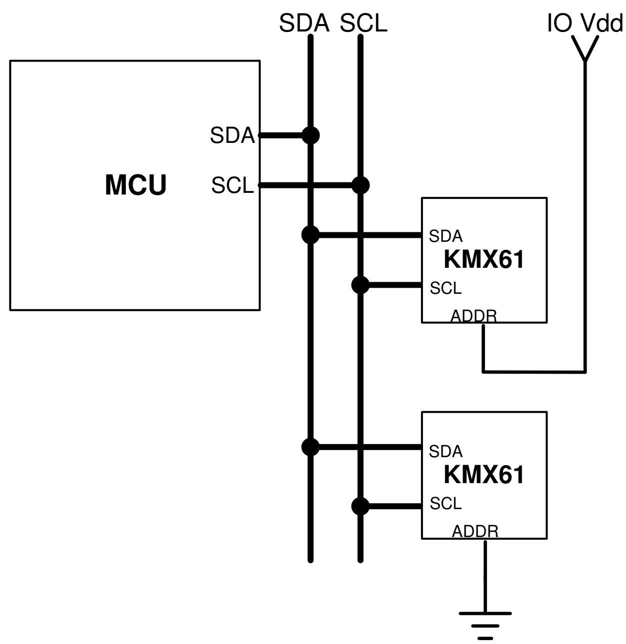

Figure 1. Multiple KMX61 I²C Connection

Description	Address Pad	7 bit Address	Address	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
I2C Wr	IO_VDD	0Fh	1Eh	0	0	0	1	1	1	1	0
I2C Rd	IO_VDD	0Fh	1Fh	0	0	0	1	1	1	1	1
I2C Wr	GND	0Eh	1Ch	0	0	0	1	1	1	0	0
I2C Rd	GND	0Eh	1Dh	0	0	0	1	1	1	0	1

Table 9. I2C Address

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally-stored address. If they match, the device considers itself addressed by the Master. The KMX61's Slave Address is comprised of two programmable parts, which allows for connection of multiple KMX61's to the same I²C bus. The LSB is determined by the

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assignment of ADDR to GND or IO_Vdd. Figure 1 and Table above shows how two KMX61's would be implemented on an I2C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free. Note that if the KMX61 is accessed through I^2C protocol before the startup is finished a NACK signal is sent.

Writing to a KMX61 8-bit Register

Upon power up, the Master must write to the KMX61's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KMX61 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KMX61 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KMX61 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KMX61 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KMX61 is now stored in the appropriate register. The KMX61 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page. When the auto-increment feature reaches register address 0x7F (Buffer Read), it stops and does not advance to register address 0x80. A new read command must be issued for registers above 0x7F. The part then continues to auto-increment until it reaches address 0xFF.

Reading from a KMX61 8-bit Register

When reading data from a KMX61 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KMX61 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KMX61 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KMX61 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KMX61 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^2C bus and how the Master and Slave interact during these transfers. Table 10 defines the I^2C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 10. I^2C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing one byte to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	S	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

Power Modes

The KMX61 has four power modes: Off, Stand-by, Sleep, Enabled. The part exists in one of these four modes at any given time. Off and Stand-by modes have very low current consumptions.

Power Mode	Bus State	V_{IO}	V_{dd}	Function	Outputs
Off	-	OFF	OFF	No sensor activity	Not available
		ON	OFF		
		OFF	ON		
Stand-by	Active	ON	ON	Waiting activation command	Not available
Sleep	Active	ON	ON	Accelerometer active looking for motion wake up	Accel registers only – no buffer, no DRDY int
Enabled	Active	ON	ON	All functionalities available	All sensors available

Off mode

One or both of the power supplies (V_{dd} or V_{IO}) are not powered. The sensor is completely inactive and neither reporting nor communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on V_{IO} before V_{dd}, but if V_{dd} is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

1. V_{IO} supply is valid
2. V_{dd} power supply is going to valid level

OR

1. V_{IO} power supply is going to valid level
2. V_{dd} supply is valid

When POR occurs, the registers are loaded from OTP and the part is put into Stand-by mode.

Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command from the external application processor via the I^2C bus.

Sleep mode

While in sleep mode, the accelerometer is periodically taking a measurement to detect if there is any motion. Data in the accelerometer registers is being updated, however, there is no data ready interrupt being reported. Also, no data is being sent to the buffer.

Enable mode

Stand-by-mode can be changed to Enabled mode by writing to register STBY_REG.

This engages the full functionality of accelerometer and/or magnetometer measurements in a higher power, higher resolution mode. The host has the ability to change settings in the control register back to Stand-by mode for either or both the accelerometer and magnetometer. If enabled, the back to sleep function will put the part into the Sleep mode.

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KMX61 Embedded Registers

The KMX61 has 49 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 11 below provides a listing of the accessible 8-bit registers and their addresses.

Table 11. I^2C Register Map

I2C Address (Hex)	Register Name	Type R/W
00h	WHO_AM_I	R
01h	INS1	R
02h	INS2	R
03h	STATUS_REG	R
0Ah	ACCEL_XOUT_L	R
0Bh	ACCEL_XOUT_H	R
0Ch	ACCEL_YOUT_L	R
0Dh	ACCEL_YOUT_H	R
0Eh	ACCEL_ZOUT_L	R
0Fh	ACCEL_ZOUT_H	R
10h	TEMP_OUT_L	R
11h	TEMP_OUT_H	R
12h	MAG_XOUT_L	R
13h	MAG_XOUT_H	R
14h	MAG_YOUT_L	R
15h	MAG_YOUT_H	R
16h	MAG_ZOUT_L	R
17h	MAG_ZOUT_H	R
18h	XOUT_HPF_L	R
19h	XOUT_HPF_H	R
1Ah	YOUT_HPF_L	R
1Bh	YOUT_HPF_H	R
1Ch	ZOUT_HPF_L	R
1Dh	ZOUT_HPF_H	R
24h	SN_1	R

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25h	SN_2	R
26h	SN_3	R
27h	SN_4	R
28h	INL	W
29h	STBY_REG	R/W
2Ah	CNTL1	R/W
2Bh	CNTL2	R/W
2Ch	ODCNTL	R/W
2Dh	INC1	R/W
2Eh	INC2	R/W
2Fh	INC3	R/W
3Ch	COTR	R
3Dh	WUFTH	R/W
3Eh	WUFC	R/W
3Fh	BTH	R/W
40h	BTSC	R/W
4Ch	TEMP_EN_CNTL	R/W
60h	SELF_TEST	W
76h	BUF_THRESH_H	R/W
77h	BUF_THRESH_L	R/W
78h	BUF_CTRL1	R/W
79h	BUF_CTRL2	R/W
7Ah	BUF_CLEAR	W
7Bh	BUF_STATUS_REG	R
7Ch	BUF_STATUS_H	R
7Dh	BUF_STATUS_L	R
7Eh	BUF_READ	R