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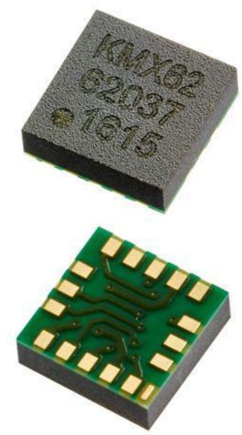
Kionix®	**± 1200uT Tri-axis Digital Magnetometer/ ± 2g/4g/8g/16g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KMX62-1031** **Rev. 4.0** **20-Dec-2017**

Product Description



KMX62 is a 6 Degrees-of-Freedom inertial sensor system that features 16-bit digital outputs accessed through I²C communication. The KMX62 sensor consists of a tri-axial magnetometer plus a tri-axial accelerometer coupled with an ASIC. It is packaged in a 3 x 3 x 0.9 mm Land Grid Array (LGA) package. The ASIC is realized in standard 0.18µm CMOS technology and features flexible user programmable ±2g / ±4g / ±8g / ±16g full scale range for the accelerometer and ±1200µT full scale range for the magnetometer. Accelerometer and Magnetometer data can be accumulated in an internal 384-byte FIFO buffer and transmitted to the application processor.

Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias, and sensitivity adjustments, as well as temperature compensation.

Magnetic sensing is based on the principle of magnetic impedance. The magnetic sensor detects very small magnetic fields by passing an electric pulse through a special electron spin aligned amorphous wire. Due to the high Curie temperature of the wire, the sensor's thermal performance shows excellent stability.

Noise performance is excellent with bias stability over temperature. Bias errors resulting from assembly can be trimmed digitally by the user. These sensors can accept supply voltages between 1.7V and 3.6V, and digital communication voltages between 1.2V and 3.6V.

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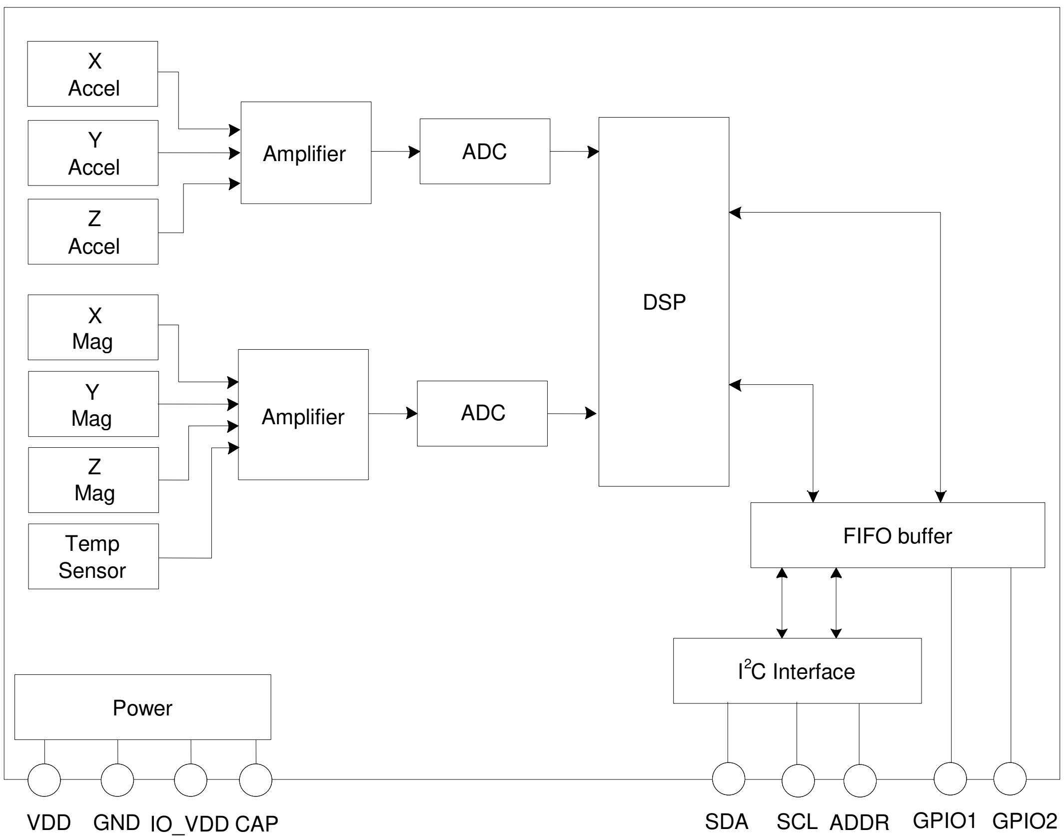
Functional Diagram



Product Specifications

Note: Specifications are for operation at VDD = 2.5V, T = 25ºC, High Resolution Mode (<RES> = 10, 11) unless stated otherwise.

Mechanical

Magnetometer

Parameters	Units	Min	Typical	Max
Operating Temperature Range	ºC	-40	-	+85
Full Scale Range	µT		±1200	
Digital Bit Depth	bits		16	
Offset at Zero Magnetic Field	µT		0	
Offset Temperature Coefficient	µT/ºC		±0.3	
Magnetic Sensitivity	counts/µT		27.3	
Sensitivity Accuracy	%		±20	
Sensitivity Temperature Coefficient.	%/ºC		±0.05	
Positive Self Test Output change on Activation	µT		800	
Integral Non-Linearity	% of FS		0.5	
Noise[1,2]	µT (RMS)		0.3	
Cross Axis Sensitivity	% of FS		2 (XY) 0.5 (XZ) 0.3 (YX) 0.2 (YZ) 0.9 (ZX) 0.2 (ZY)	
Maximum Exposed Field[3]	µT			500000

Table 1: Magnetometer Specifications

Notes:

1. Noise varies with Output Data Rate (ODR) as set by OSM<3:0> bits in ODCNTL and RES<1:0> bits in CNTL2 registers.
2. Measured at ODR = 50Hz, RES = 10, 11.
3. No permanent effect on Zero Magnetic Field Offset

Accelerometer

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	+85
Full Scale Range	GSEL1=0, GSEL0=0	g		±2	
	GSEL1=0, GSEL0=1			±4	
	GSEL1=1, GSEL0=0			±8	
	GSEL1=1, GSEL0=1			±16	
Digital Bit Depth				16	
Zero-g Offset		mg		±25	±90
Zero-g Offset Temperature Coefficient		mg/ºC		±0.25	
Sensitivity	GSEL1=0, GSEL0=0 (±2g)	counts/g		16384	
	GSEL1=0, GSEL0=1 (±4g)			8192	
	GSEL1=1, GSEL0=0 (±8g)			4096	
	GSEL1=1, GSEL0=1 (±16g)			2048	
Sensitivity Accuracy		%		±5	
Sensitivity Temperature Coefficient		%/ºC		±0.01	
Positive Self Test Output change on Activation		g	0.25 (xy) 0.2 (z)	0.5	0.75
Signal Bandwidth (-3dB)		Hz		3500 (xy) 1800 (z)	
Integral Non-Linearity		% of FS		1	
Cross Axis Sensitivity[1]		%		-2 (XY) 0.1 (XZ) 2.7 (YX) -0.7 (YZ) -0.8 (ZX) 1.4 (ZY)	
Noise[2,3]	RMS	mg		0.75	
	Density	µg/√Hz		130	

Table 2: Accelerometer Specifications

Notes:

1. As measured in a test socket at the factory. The cross-axis sensitivity that is measured is the by-product of positional inaccuracies at all stages of test and assembly.
2. Noise varies with Output Data Rate (ODR) as set by OSA<3:0> bits in ODCNTL, and RES<1:0> bits in CNTL2 registers.
3. Measured at ODR = 50Hz, RES = 10, 11.

Temperature Sensor

(specifications are for operation at VDD = 2.5V and T = 25ºC unless stated otherwise)

Parameters	Units	Min	Typical	Max
Operating Temperature Range	ºC	-40	-	+85
Output Accuracy	± ºC		5	
Sensitivity (16-bit digital)	counts/ºC		256	
Sensitivity (8-bit digital, TEMP<15:8>)	counts/ºC		1	

Table 3: Temperature Sensor Mechanical Specifications

Electrical

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.7	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.2		3.6
Current Consumption[1] (High Resolution Mode) (<RES> = 10 or 11)	Operating (mag + accel)	µA		395	
	Magnetometer only	µA		295	
	Accelerometer only	µA		150	
	Standby	µA		1	5
Output Low Voltage[2] (IO_VDD < 2V)		V	-	-	0.2 * IO_VDD
Output Low Voltage[2] (IO_VDD ≥ 2V)		V	-	-	0.4
Output High Voltage		V	0.9 * IO_VDD	-	-
Input Low Voltage		V	-	-	0.3 * IO_VDD
Input High Voltage		V	0.7 * IO_VDD	-	-
I²C Communication Rate[3,4]		kHz	100	400	3400
I²C Slave Address (7-bit)				0x0E / 0x0F	
Output Data Rate (ODR)		Hz	0.781	100	1600
Bandwidth (-3dB)[5]	RES 00,01	Hz		400	
	RES 10,11	Hz		ODR/2	
Internal Oscillator Tolerance		%	-10		10
Start Up Time[6]		ms	1		1300

Table 4: Electrical Specifications

Notes:

1. See Figure 2 for other modes (RES = 00 or 01)
2. Assuming I²C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA
3. Assuming max bus capacitance load of 20pF
4. The I²C bus supports Standard-Mode, Fast-Mode, and High-Speed Mode.
5. User selectable via ODR control register setting
6. Start up time is from ACCEL_EN / MAG_EN set to valid outputs. Time varies with Output Data Rate (ODR) and mode setting (RES) (see Figure 1).

Start Up Time Profile

Typical Start Up Time over selected ODR (0.781,1.563,3.125,6.25,12.5,25,50,100,200,400,800,1600Hz)

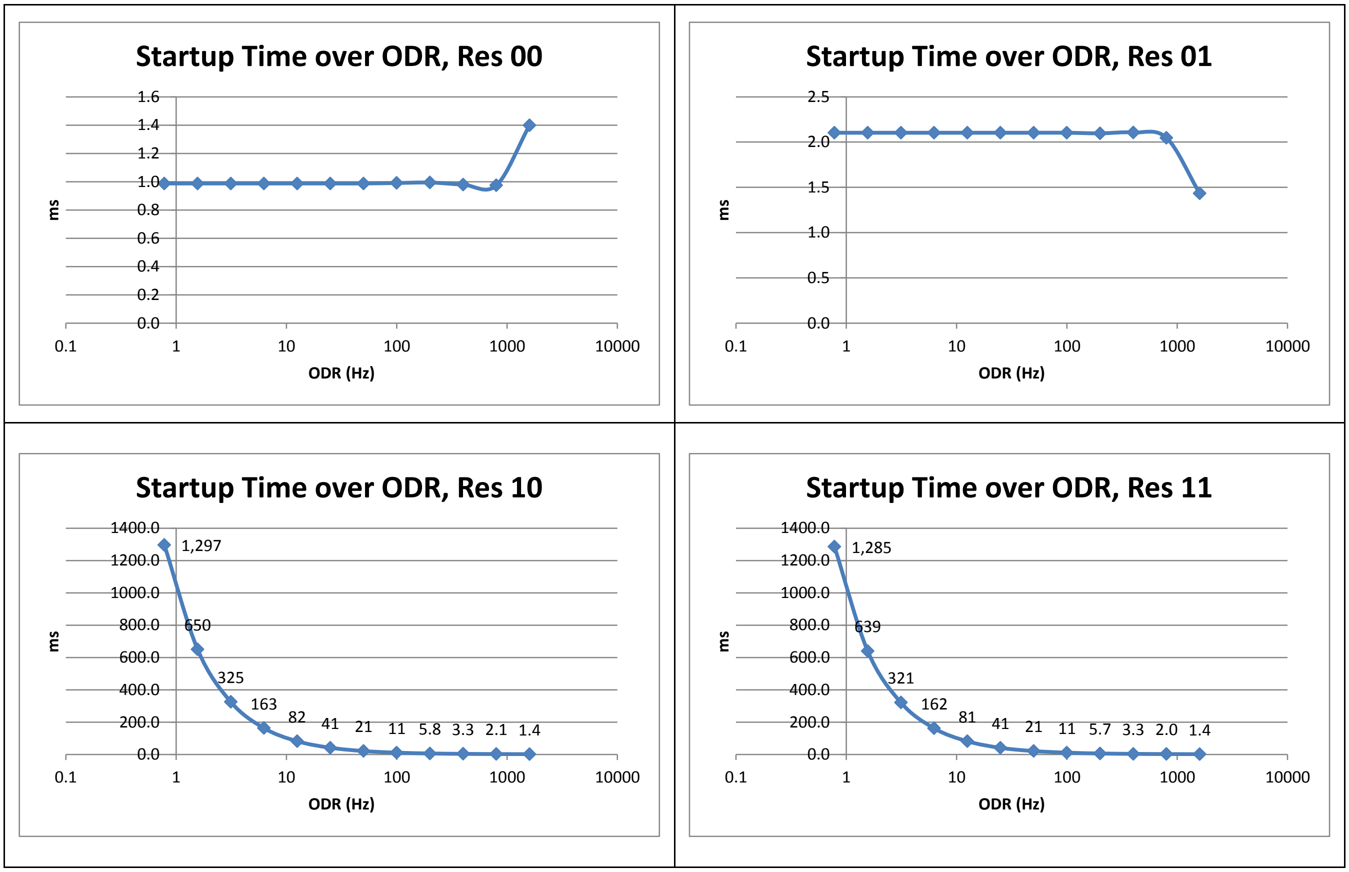


Figure 1: Start Up Time Diagram

Current Profile

Typical current over selected ODR (0.781,1.563,3.125,6.25,12.5,25,50,100,200,400,800,1600Hz) @ VDD = 2.5V and T = 25ºC

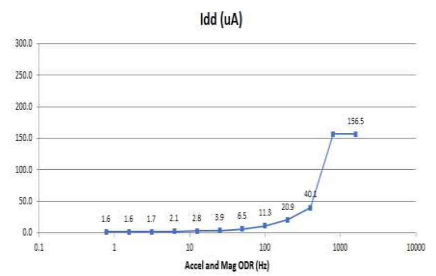
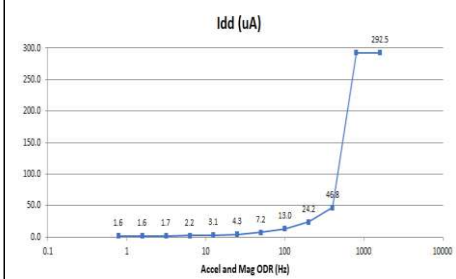
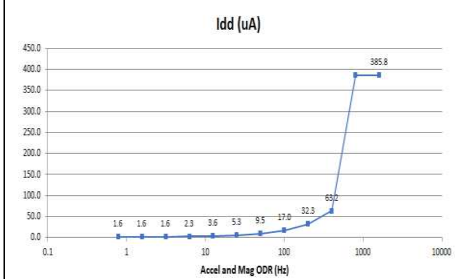
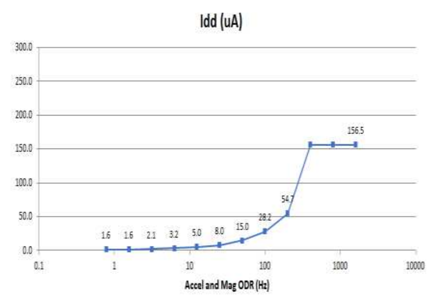
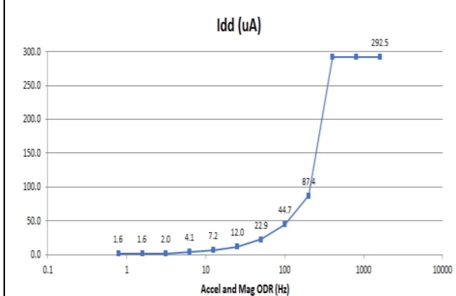
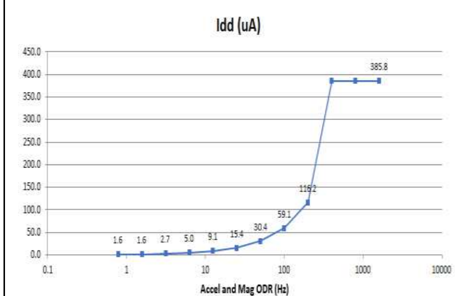
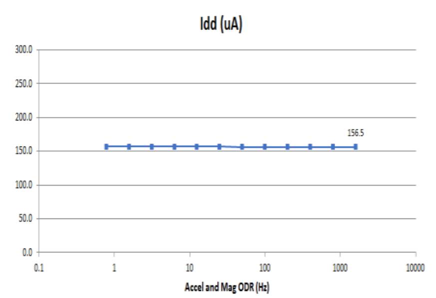
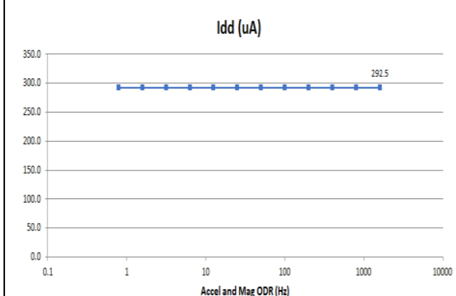
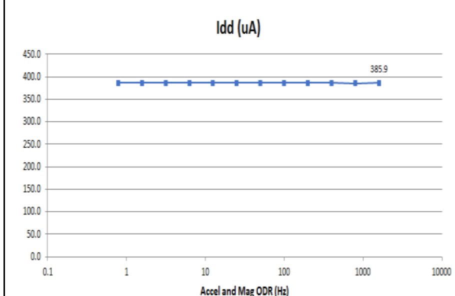
Res	Accel Only	Mag Only	Accel and Mag
00			
01			
10, 11			

Figure 2: Current Consumption Diagram

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Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{LOW}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{LOW}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the VDD ramp up time **T_{VDD}** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

! *To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{LOW}, T_{VDD}, T_{VDD_OFF} and temperature as POR performance can vary depending on these parameters.*

Please refer to Technical Note ***TN005 Power-On Procedure*** for more information.

Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.3	-	3.6
Operating Temperature Range		°C	-40	-	85
Storage Temperature Range		°C	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Table 5: Environmental Specifications

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

RoHS 2011/65/EU

These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout". The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: *7C-I - Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectric devices) or in a glass or ceramic matrix compound.*

REACH COMPLIANCE

These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-174) as identified by the European Chemicals Agency as of 12 July 2017.

HF

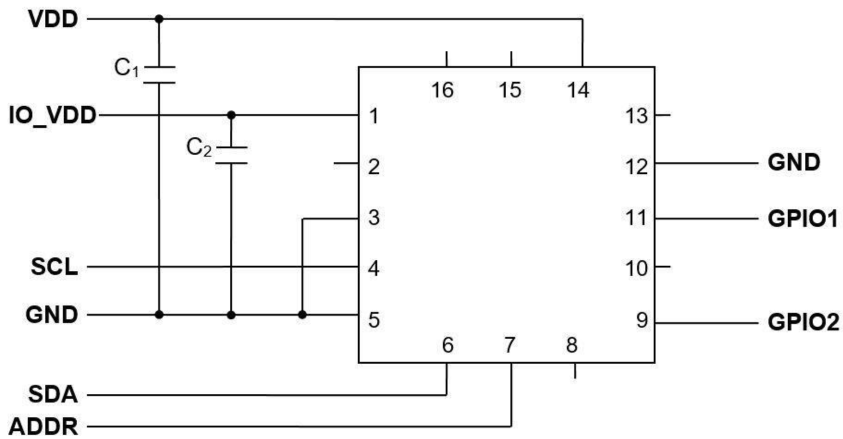
This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Application Schematic and Pin Description

Application Schematic



Pin Description

Pin	Name	Description
1	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	CAP	Do not connect. Must be left floating.
3	GND	Ground
4	SCL	I2C Serial Clock
5	GND	Ground
6	SDA	I2C Serial Data
7	ADDR	I2C Address pin. This pin must be connected to IO_VDD or GND to determine the I2C Device Address.
8	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.
9	GPIO2	GPIO 2. Cannot float when configured as an input.
10	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.
11	GPIO1	GPIO 1. Cannot float when configured as an input.
12	GND	Ground
13	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.
14	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.
16	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.

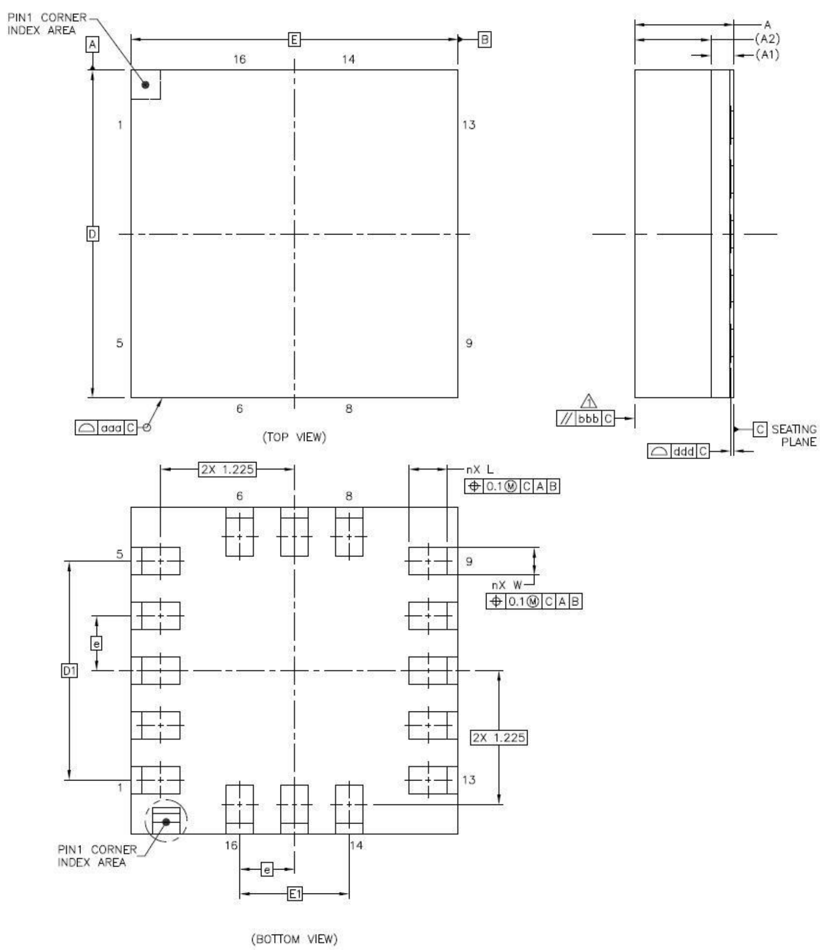
Table 6: Pin Description

Note: Pins 3, 5, and 12 (GND) are internally tied together.

Package Dimensions and Orientation

Dimensions

3 x 3 x 0.9 mm LGA



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.21	REF
MOLD THICKNESS	A2		0.7	REF
BODY SIZE	D		3	BSC
	E		3	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.3	0.35	0.4
LEAD PITCH	e		0.5	BSC
LEAD COUNT	n		16	
EDGE BALL CENTER TO CENTER	D1		2	BSC
	E1		1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

NOTES:

⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

All dimensions and tolerances conform to ASME Y14.5M-1994

Orientation

When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase. When the +X, +Y, or +Z arrow is directed toward North, the output of that axis is positive.

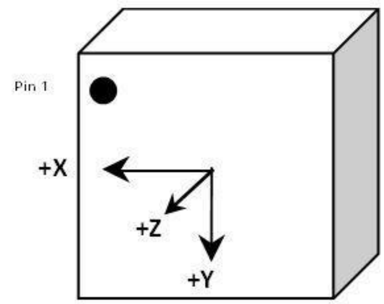


Figure 3: Accelerometer and Magnetometer Orientation

Please avoid mounting this product on the part in which magnetic field disturbance exists, such as near any parts containing ferrous materials.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):
GSEL1=0, GSEL0=0 (±2g)

Position	**1**	**2**	**3**	**4**	**5**	**6**
Diagram					Top Bottom	Bottom Top
Resolution (bits)	16	16	16	16	16	16
X (counts)	0	-16384	0	+16384	0	0
Y (counts)	-16384	0	+16384	0	0	0
Z (counts)	0	0	0	0	+16384	-16384
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**

(1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):
GSEL1=0, GSEL0=1 (±4g)

Position	1	2	3	4	5	6
Diagram					Top / Bottom	Bottom / Top
Resolution (bits)	16	16	16	16	16	16
X (counts)	0	-8192	0	+8192	0	0
Y (counts)	-8192	0	+8192	0	0	0
Z (counts)	0	0	0	0	+8192	-8192
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**

(1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):
GSEL1=1, GSEL0=0 (±8g)

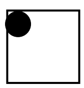
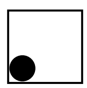
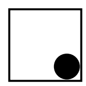
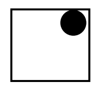
Position	1	2	3	4	5	6
Diagram					Top / Bottom	Bottom / Top
Resolution (bits)	16	16	16	16	16	16
X (counts)	0	-4096	0	+4096	0	0
Y (counts)	-4096	0	+4096	0	0	0
Z (counts)	0	0	0	0	+4096	-4096
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**

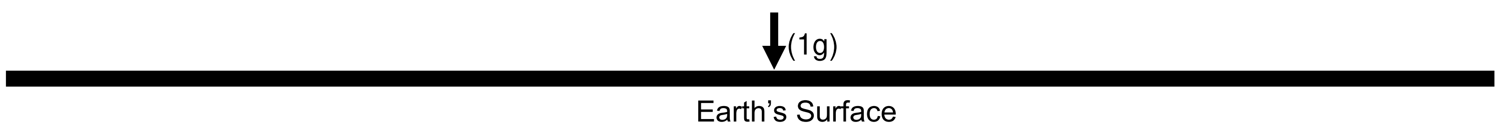
(1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1 (±16g)

Position	**1**	**2**	**3**	**4**	**5**	**6**
Diagram					Top / Bottom	Bottom / Top
Resolution (bits)	16	16	16	16	16	16
X (counts)	0	-2048	0	+2048	0	0
Y (counts)	-2048	0	+2048	0	0	0
Z (counts)	0	0	0	0	+2048	-2048
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**



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Digital Interface

The Kionix KMX62 digital sensor can communicate on the I^2C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system processors. The I^2C interface is compliant with high-speed mode, fast mode, and standard mode I^2C protocols.

The serial interface terms and descriptions as indicated in Table 7 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 7: Serial Interface Terminologies

I^2C Serial Interface

As previously mentioned, the KMX62 can communicate on an I^2C bus. I^2C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The system Master provides the serial clock signal and addresses Slave devices on the bus. The KMX62 always operates as a Slave device during standard Master-Slave I^2C operation.

I^2C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held LOW by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I^2C bus is considered free when both lines are HIGH.

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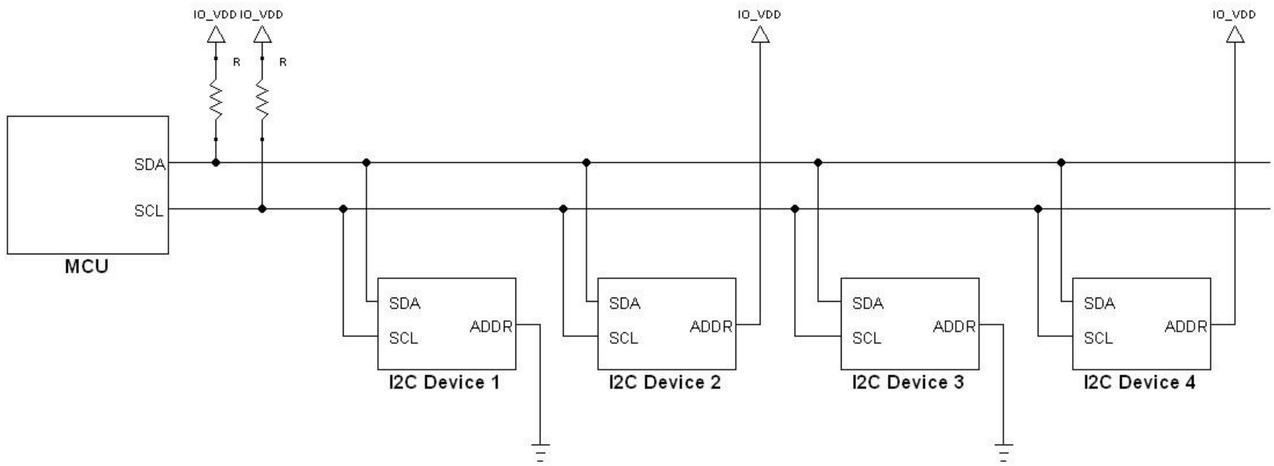
I^2C Operation

Transactions on the I^2C bus begin after the Master transmits a start condition (S), which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally-stored address. If they match, the device considers itself addressed by the Master. The KMX62 Slave Address is comprised of a user programmable part, a factory programmable part, and a fixed part, which allows for connection of multiple sensors to the same I^2C bus. The Slave Address associated with the KMX62 is 00011YX, where the user programmable bit X, is determined by the assignment of ADDR (pin 7) to GND or IO_VDD. Also, the factory programmable bit Y is set at the factory. **For KMX62-1031, the factory programmable bit Y is fixed to 1** (contact your Kionix sales representative for list of available devices). Table 8 lists possible I^2C addresses for KMX62-1031. It is possible to have up to four sensors on a shared I^2C bus as shown in Figure 4 (i.e. two KMX62-1031 accelerometer/magnetometer and two additional accelerometer/magnetometer with the factory programmable bit Y set to **0**).

									Y	X	
Description	**Address Pad**	**7-bit Address**	**Address**	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
I2C Wr	GND	0x0E	0x1C	0	0	0	1	1	1	0	0
I2C Rd	GND	0x0E	0x1D	0	0	0	1	1	1	0	1
I2C Wr	IO_VDD	0x0F	0x1E	0	0	0	1	1	1	1	0
I2C Rd	IO_VDD	0x0F	0x1F	0	0	0	1	1	1	1	1

Table 8: I^2C Address

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line LOW so that it remains stable LOW during the HIGH period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from LOW to HIGH while SCL is HIGH. The I^2C bus is now free. Note that if the KMX62 is accessed through I^2C protocol before the startup is finished a NACK signal is sent.



I2C Device	Part Number	ADDR Pin	Slave Address	Bit Y (Bit 1 in 7-bit address)
1	KMX62-1031	GND	0x0E	Factory Set to 1
2	KMX62-1031	IO_VDD	0x0F	Factory Set to 1
3	*KXMMM	GND	0x0C	Factory Set to 0
4	*KXMMM	IO_VDD	0x0D	Factory Set to 0

* KXMMM – contact Kionix sales representative for list of compatible devices

Figure 4: Multiple KMX62 I^{2}C Connection

Writing to an 8-bit Register

Upon power up, the Master must write to the KMX62's control registers to set its operational mode. Therefore, when writing to a control register on the I^{2}C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KMX62 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KMX62 to which 8-bit register the Master will be writing the data. Since this is I^{2}C mode, the MSB of the RA command should always be zero (0). The KMX62 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KMX62 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KMX62 is now stored in the appropriate register. The KMX62 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Reading from an 8-bit Register

When reading data from a KMX62 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KMX62 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KMX62 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KMX62 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. The KMX62 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. Table 9 defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 9: I²C Terms

Sequence 1: The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2: The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3: The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4: The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

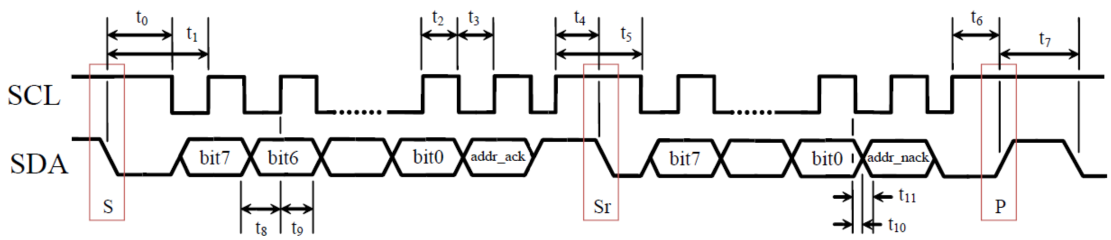
HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: A Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5: HS-mode data transfer of the Master writing one byte to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	S	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

I²C Timing Diagram



Number	Description	MIN	MAX	Units
t_0	SDA LOW to SCL LOW transition (Start event)	50	-	ns
t_1	SDA LOW to first SCL rising edge	100	-	ns
t_2	SCL pulse width: HIGH	100	-	ns
t_3	SCL pulse width: LOW	100	-	ns
t_4	SCL HIGH before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: HIGH during a S/Sr/P event	100	-	ns
t_6	SCL HIGH before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: HIGH	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I²C CLK	2.5	-	µs

Table 10: I²C Timing (Fast Mode)

Power Modes

The KMX62 has five power modes: Off, Stand-by, Sleep, Low Power (RES = 00, 01) and High Resolution (RES = 10, 11). The part exists in one of these five modes at any given time. Off and Stand-by modes have very low current consumptions.

Power Mode	Bus State	IO_VDD	VDD	Function	Outputs
Off	-	OFF	OFF	No sensor activity	Not available
		ON	OFF		
		OFF	ON		
Stand-by	Active	ON	ON	Waiting activation command	Not available
Sleep	Active	ON	ON	Accelerometer active looking for motion wake up	Accel registers only – no buffer, no DRDY interrupt
<RES> = 00 or 01	Active	ON	ON	All functionalities available	All sensors available
<RES> = 10 or 11	Active	ON	ON	All functionalities available	All sensors available

Off mode

One or both power supplies (VDD or IO_VDD) are not powered. The sensor is completely inactive and not reporting or communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on IO_VDD before VDD, but if VDD is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

1. IO_VDD supply is valid
2. VDD power supply is going to valid level

OR

1. IO_VDD power supply is going to valid level
2. VDD supply is valid

When POR occurs, the registers are loaded from OTP and the part is put into Stand-by mode.

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