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KMZ80

Programmable angle sensor IC

Rev. 2.1 — 4 July 2018 Product data sheet

SAFE ASSURE by NXP

1 General description

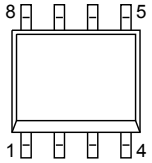
The KMZ80 is a single channel magnetic angle sensor. Magnetoresistive (MR) sensor bridges and mixed signal IC are integrated into a single package. The KMZ80 in SO8 package is intended for printed-circuit boards (PCBs) where external filter components are required. The IC allows user-specific adjustments of angular range, zero angle, and clamping voltages. The settings are stored permanently in a non-volatile memory (NVM). The programmable angle sensor is pre-programmed, pre-calibrated and therefore, ready to use.

2 Features and benefits

- High precision sensor for magnetic angular measurement
- Single package sensor module
- Automotive qualified in accordance with AEC-Q100 Rev-H
- Programmable user adjustments, e.g. zero angle and angular range
- Fail-safe non-volatile memory with write protection using lock bit
- Independent from magnetic field strength above 25 kA/m
- Factory calibrated
- Separate temperature sensor and auxiliary analog-to-digital converter (ADC) for magnetic field conversion check
- High temperature range up to 150 °C
- Ratiometric analog output voltage or push pull output stage compliant with SAE J2716 SENT using pulse shaping
- Overvoltage protection up to 18 V
- Power-loss detection
- Programming via one-wire interface (OWI)
- 8 × 12-bit original equipment manufacturer (OEM) code registers for identification (ID)
- ISO 26262 ASIL-C capable, safety element out of context (SEooC)
- Multipoint calibration (MPC) with 17 equidistant or seven free selectable calibration points
- Low latency

3 Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline
1	n.c.	not connected	
2	V_{DD}	supply voltage	
3	V_{DD}	supply voltage	
4	GND	ground	
5	OUT/DATA	analog/single edge nibble transmission (SENT) output or data interface	
6	n.c.	not connected	
7	n.c.	not connected	
8	n.c.	not connected	

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
KMZ80	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 Functional diagram

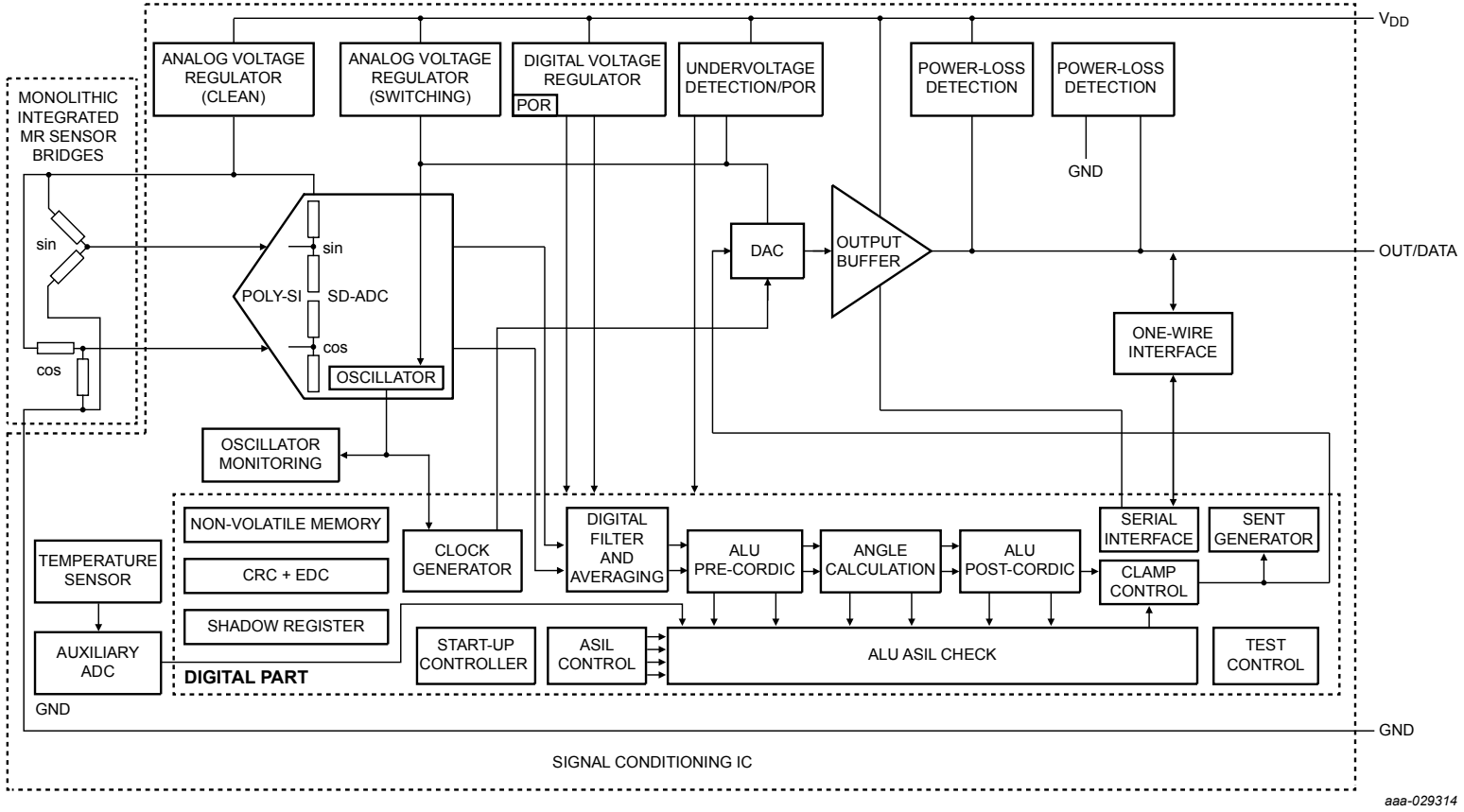


Figure 1. Functional diagram

6 Functional description

The KMZ80 converts two orthogonal signals from MR sensor bridges into the digital domain. The angle is calculated using the coordinate rotation digital computer (CORDIC) algorithm. After a digital-to-analog conversion, the analog signal is provided to the output as a linear representation of the angular value or transmitted in a SENT frame compliant to SAE J2716. Zero angle, clamping voltages and angular range are programmable. In addition, eight 12-bit registers are available for customer purposes, such as sample ID.

KMZ80 comprises a cyclic redundancy check (CRC) and an error detection code (EDC) to ensure a fail-safe operation. If either the supply voltage or the ground line of the mixed signal IC is interrupted, a power-loss detection circuit pulls the output to the remaining connection.

After conversion into the digital domain by an ADC, further processing is done within an on-chip state machine. This state machine controls offset cancelation, calculation of the mechanical angle using the CORDIC algorithm, as well as zero angle and angular range adjustment. The internal digital-to-analog converter (DAC) and the analog output stage are used for conversion of the angle information into an analog output voltage, which is ratiometric to the supply voltage. Alternatively, the output signal can be transmitted digitally in a SENT frame compliant to SAE J2716.

The configuration parameters are stored in a user-programmable non-volatile memory. The OWI (accessible using pin OUT/DATA) is used for accessing the memory. In order to protect the memory content a lock bit can be set. After locking the non-volatile memory, its content cannot be changed anymore.

6.1 Angular measurement directions

The signals of the MR sensor bridges depend only on the direction of the external magnetic field vector H_{ext}, which is applied parallel to the plane of the sensor. In order to obtain a correct output signal, exceed the minimum saturation field strength.

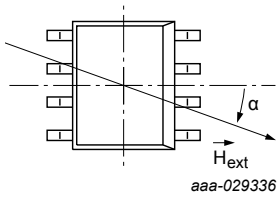


Figure 2. Angular measurement directions

Since the anisotropic MR (AMR) effect is periodic over 180°, the sensor output is also 180°-periodic. The angle is calculated relative to a freely programmable zero angle. The dashed line indicates the mechanical zero degree position.

7 Analog output

KMZ80 provides an analog output signal on pin OUT/DATA (if bit 12 in register SYS_SETTING is set to logic 0; see Table 49). The measured angle α is converted linearly into a value, which is ratiometric to the supply voltage V_{DD}. Either a positive or a negative slope is provided for this purpose.

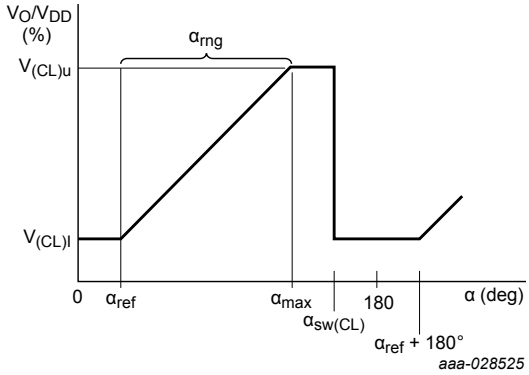
Table 3 describes the analog output behavior for a positive slope. A magnetic field angle, above the programmed maximum angle α_{max}, but below the clamp switch angle $\alpha_{sw(CL)}$

sets the analog output to the upper clamping voltage. If the magnetic field angle is larger than the clamp switch angle, the analog output switches from upper to lower clamping voltage. If there is a negative slope, the clamping voltages are changed.

Table 3. Analog output behavior for a positive slope

Magnetic field angle	Analog output
$\alpha_{max} < \alpha < \alpha_{sw(CL)}$	$V_{(CL)u}$
$\alpha_{sw(CL)} < \alpha < \alpha_{ref} + 180°$	$V_{(CL)l}$

The analog output voltage range encodes both angular and diagnostic information. A valid angle value is between the upper and lower clamping voltage. If the analog output is in the diagnostic range that is below 4 $\%V_{DD}$ or above 96 $\%V_{DD}$, an error condition has been detected. The analog output repeats every 180°.



$\alpha_{max} = \alpha_{ref} + \alpha_{rng}$

Figure 3. Characteristic of the analog output

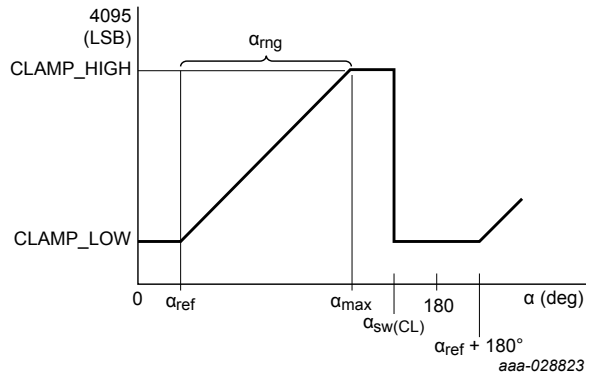
8 Digital output

KMZ80 provides a digital output signal on pin OUT/DATA (if bit 12 in register SYS_SETTING is set to logic 1; see Table 49) compliant with the SAE J2716 SENT standard. The measured angle α is converted linearly into a value, which is digital encoded in SENT frames. Either a positive or a negative angular slope characteristic is provided for this purpose.

Table 4 describes the digital output behavior for a positive slope. A magnetic field angle above the programmed maximum angle α_{max} but below the clamp switch angle $\alpha_{sw(CL)}$ sets the output to the upper clamping value. If the magnetic field angle is larger than the clamp switch angle, the output value switches from upper to lower clamping value. If there is a negative slope, the clamping levels are changed.

Table 4. Digital output behavior for a positive slope

Magnetic field angle	Data value
$\alpha_{max} < \alpha < \alpha_{sw(CL)}$	CLAMP_HIGH
$\alpha_{sw(CL)} < \alpha < \alpha_{ref} + 180°$	CLAMP_LOW



$\alpha_{max} = \alpha_{ref} + \alpha_{rng}$

Figure 4. Characteristic of the digital output

8.1 Transmission of sensor messages

KMZ80 encodes a 12-bit angular value into a sequence of pulses based on the encoding scheme of the SAE J2716 SENT standard. Data is split into 4-bit nibbles that are encoded in the time-domain as the duration between two falling edges. The message frame is a sequence of 4-bit nibbles (SENT frame). The timebase of the SENT frame is defined in clock ticks with a configurable duration of T_{clk} = 2.7 µs, 3 µs, 4.5 µs, and 6 µs each clock tick. A calibration pulse (SYNC nibble) followed by a STATUS nibble, a constant number of fast channel DATA nibbles, a CRC nibble, and an optional PAUSE pulse define one message frame of a SENT transmission as shown in Figure 5. The KMZ80 is compatible with revisions of the SENT specification listed below and supports data formats in accordance with appendix A.1, H.1, A.3, H.4, and H.3.

General SENT specification can be found in:

- SAE J2716 FEB2008 SENT rev 2
- SAE J2716 JAN2010 SENT rev 3
- SAE J2716 APR2016 SENT rev 4

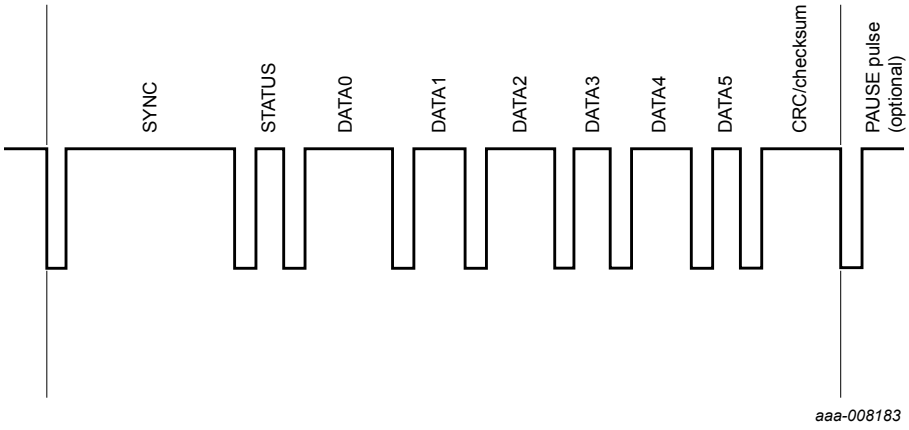


Figure 5. SENT frame

8.2 SYNC nibble

The synchronization and calibration nibble is always 56 clock ticks long. The receiver uses the SYNC nibble to derive the clock tick time from the SENT frame.

8.3 STATUS nibble

The STATUS nibble contains status and slow channel information of the KMZ80. Bit 0 reflects the operating mode, i.e. normal or diagnostic mode. Bit 1 is a pre-warning indication and is set while the device is still in normal mode. For a detailed description of the pre-warning bit, see Section 8.11.1.2.

Bit 2 and bit 3 are used for optional slow channel serial data messages using the enhanced serial protocol (ESP), described in Section 8.10.

Table 5. STATUS nibble

Bit	Description
3 [most significant bit (MSB)]	serial data message bit if ESP is enabled, otherwise logic 0
2	serial data message bit if ESP is enabled, otherwise logic 0
1	pre-warning[1] 0b – normal operation 1b – pre-warning condition
0 [least significant bit (LSB)]	operating mode[2] 0b – normal operation 1b – diagnostic condition[3]

[1] Bit 1 can be permanently set to logic 0 via register bit; see Table 49.
[2] Bit 0 can be permanently set to logic 0 via register bit; see Table 49.
[3] Enable the serial data communication for detailed diagnostic information; see Table 14 and Table 15.

8.4 CRC nibble

The CRC nibble contains the 4-bit checksum of the DATA nibbles only. The CRC calculation does not cover the STATUS nibble.

The CRC is calculated using polynomial $x^4 + x^3 + x^2 + 1$ with seed value of 0101b. The KMZ80 supports both the legacy CRC defined in SENT SAE J2716 FEB2008 and earlier revisions and the recommended CRC defined in SENT SAE J2716 JAN2010 and later.

The CRC version can be selected via CRC type bit in the SENT_SETTING1 register; see Table 49. CRC in accordance with SAE J2710 JAN2010 is the default configuration.

8.5 PAUSE pulse

A PAUSE pulse can be optionally attached to the SENT frame to generate messages with a constant frame length via register; see Table 49. The frame length depends on the protocol format:

- A.1 and H.1: 239 clock ticks
- A.3 and H.4: 269 clock ticks
- H.3: 196 clock ticks

Additionally, the frame length with PAUSE pulse can be set to 297 clock ticks for all protocol formats via register.

8.6 DATA nibbles

In general, the DATA nibbles contain the fast channel angular value of the device. The DATA nibble content depends on the selected protocol format. KMZ80 supports the following different protocol formats as defined in the SAE J2716 SENT specification:

- Single secure sensor format A.3 (rev 3), H.4 (rev 4)
- Dual throttle position sensor format A.1 (rev 3), H.1 (rev 4)
- High-speed 12-bit message format H.3 (rev 4)

A detailed frame format description can be found in the corresponding subsection.

8.7 Single secure sensor formats A.3 and H.4

KMZ80 generates the sequence shown in Table 6 repeatedly in accordance with the single secure sensor format defined in SAE J2716 JAN2010 SENT appendix A.3, respectively J2716 APR2016 SENT appendix H.4. DATA nibbles D0 to D2 contain the 12-bit angular value. D3 and D4 reflect the value of an 8-bit loop counter. D5 is an inverted copy of the most significant nibble (MSN) DATA0. The difference between A.3 and H.4 is that A.3 uses the whole 12-bit data range for angular values while H.4 excludes the values 0 and 4089 to 4095 from the angular data range for diagnostic purposes; see Table 7.

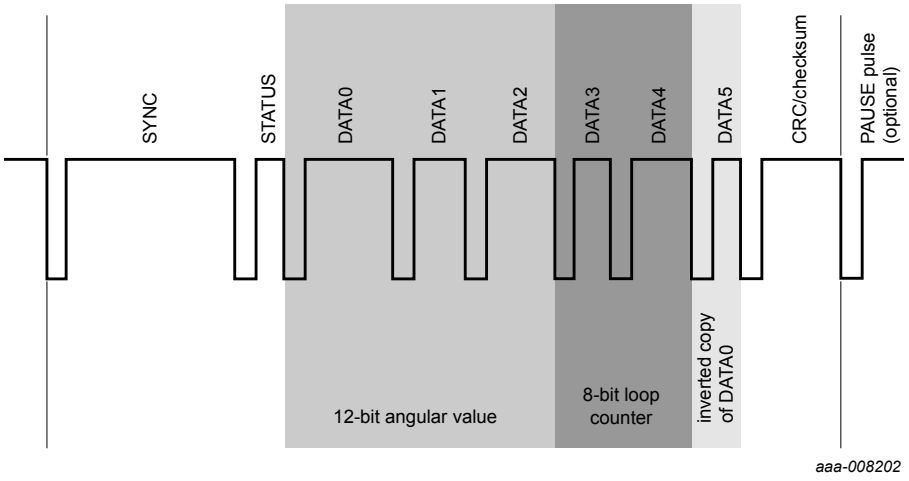


Figure 6. Single secure sensor formats A.3 and H.4

Table 6. Single secure sensor formats A.3 and H.4: frame

SYNC	STATUS	DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	CRC
-	diagnostic and pre-warning	D0[1]	D1	D2[2]	D3[1]	D4[2]	D5	-
-		12-bit angular value			8-bit loop counter		inverted D0	-

[1] MSN.
[2] Least significant nibble (LSN).

DATA nibbles D0 to D2 contain the angular value information in the single secure sensor format. A.3 uses the complete 12-bit data range for angular values while H.4 has reserved values for initialization and diagnostic information.

Table 7. DATA nibbles D0 to D2: angular value

D0[1]	D1	D2[2]	A.3		H.4	
			12-bit value	Angle	12-bit value	Angle/mode
0000	0000	0000	0	0°	0	initialization message
0000	0000	0001			1	0°
:	:	:			:	:
1111	1111	1000			4088	α_{max}
1111	1111	:	:	:	:	reserved
1111	1111	1010			4090	diagnostic mode[3]
1111	1111	:			:	reserved
1111	1111	1111	4095	α_{max}	4095	reserved

[1] MSN.
[2] LSN.
[3] For detailed diagnostic information, the serial data communication can be enabled.

Data nibbles D3 and D4 contain an 8-bit loop counter value with wrap-around common for both protocol formats A.3 and H.4.

Table 8. DATA nibbles D3 and D4: 8-bit loop counter

D3[1]	D4[2]	8-bit loop counter
0000	0000	0
:	:	:
1111	1111	255

[1] MSN.
[2] LSN.

For the single secure sensor format H.4 the clamping levels must be set to the correct values to comply with the SAE J2716 SENT specification: CLAMP_HIGH = 4088, CLAMP_LOW = 1. Otherwise angular values overwrite the reserved data range for diagnostic information.

8.8 Dual throttle position sensor formats A.1 and H.1

The KMZ80 generates the sequence shown in Table 9 repeatedly in accordance with the dual throttle position sensor format defined in SAE J2716 JAN2010 SENT appendix A.1 or H.1 defined in SAE J2716 APR2016.

DATA nibbles D0 to D2 contain the 12-bit angular value. DATA nibbles D3 to D5 contain the opposite slope of the same 12-bit angular value while also the order of these DATA nibbles is reversed.

A.1 uses the data range 1 to 4094 for angular values and the values 0 and 4095 for diagnostic information. While H.1 uses data range 1 to 4088 for angular values and 4090 for diagnostic information.

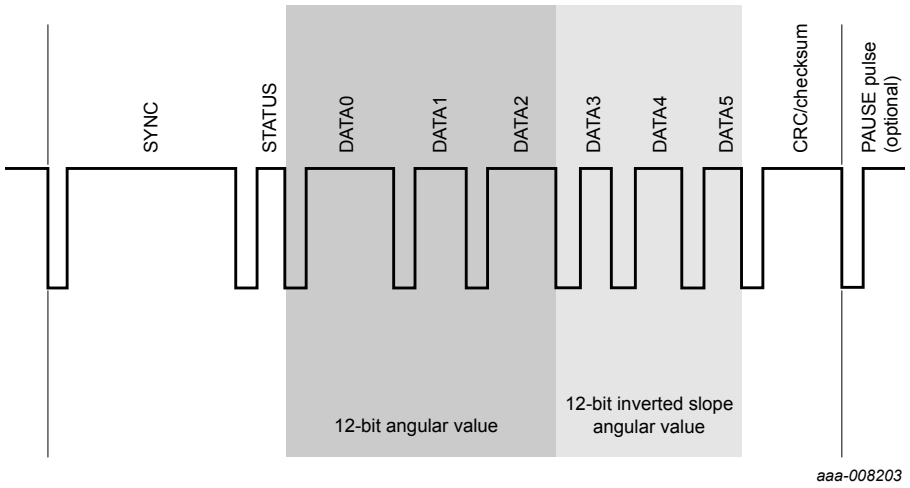


Figure 7. Dual throttle position sensor formats A.1 and H.1

Table 9. Dual throttle position sensor formats A.1 and H.1: frame

SYNC	STATUS	DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	CRC
-	diagnostic and pre-warning	D0[1]	D1	D2[2]	D5[2]	D4	D3[1]	-
-		12-bit angular value			12-bit inverted slope angular value			-

[1] MSN.
[2] LSN.

DATA nibbles D0 to D2 contain the angular value information in the dual throttle position sensor formats A.1 and H.1.

Table 10. DATA nibbles D0 to D2: angular value

D0[1]	D1	D2[2]	A.1		H.1	
			12-bit value	Angle	12-bit value	Angle/mode
0000	0000	0000	0	reserved	0	initialization message
0000	0000	0001	1	0°	1	0°
:	:	:			:	:
1111	1111	1000			4088	α_{max}
1111	1111	:	:	:	:	reserved
1111	1111	1010			4090	diagnostic mode[3]
1111	1111	:			:	reserved
1111	1111	1110	4094	α_{max}	4094	reserved
1111	1111	1111	4095	diagnostic mode[3]	4095	reserved

[1] MSN.
[2] LSN.
[3] For detailed diagnostic information, the serial data communication can be enabled.

For the inverted slope angular value in the DATA nibbles D3 to D5 the order of nibbles is also reversed: LSN and MSN.

When a diagnostic condition occurs in A.1 mode, the DATA nibbles D0 to D2 are all set to Fh and DATA nibbles D3 to D5 are all set to 0h. In H.1 mode, the data value of nibbles D0 to D2 is set to 4090 and DATA nibbles D3 to D5 are inverted to diagnostic value 5.

For the dual throttle position sensor formats A.1 and H.1, the clamping levels must be set to the correct values to comply with the SAE J2716 SENT specification. A.1: CLAMP_HIGH = 4094, CLAMP_LOW = 1. H.1: CLAMP_HIGH = 4088, CLAMP_LOW = 1. Otherwise angular values overwrite the reserved data range for diagnostic information.

Table 11. DATA nibbles D3 to D5: inverted slope angular value

D5[1]	D4	D3[2]	A.1		H.1	
			12-bit value	Angle	12-bit value	Angle/mode
0000	0000	0000	0	diagnostic mode[3]	0	reserved
0000	0000	0001	1	α_{max}	1	reserved
:	:	:	:	:	:	reserved
0000	0000	0101	:	:	5	diagnostic mode[3]
:	:	:	:	:	:	reserved
0000	0000	0111	:	:	7	α_{max}
:	:	:	:	:	:	:
1111	1111	1110	4094	0°	4094	0°
1111	1111	1111	4095	reserved	4095	initialization message

[1] MSN.
[2] LSN.
[3] For detailed diagnostic information, the serial data communication can be enabled.

8.9 High-speed 12-bit message format H.3

The KMZ80 generates the sequence shown in Table 12 repeatedly in accordance with the high-speed 12-bit message format H.3 defined in SAE J2716 APR2016. This mode realizes almost a doubling of the update rate compared to other modes. The increase of the update rate is achieved by transmitting 12-bit angular data with only four DATA nibbles using only 3 bit of the available 4 bit per nibble. The MSB of each nibble is always zero. Additionally, the clock tick length shall be set to 2.7 µs typically with a maximum variation of ±10 %. The SYNC, STATUS, and CRC nibble and the serial communication are the same as for the other protocol formats.

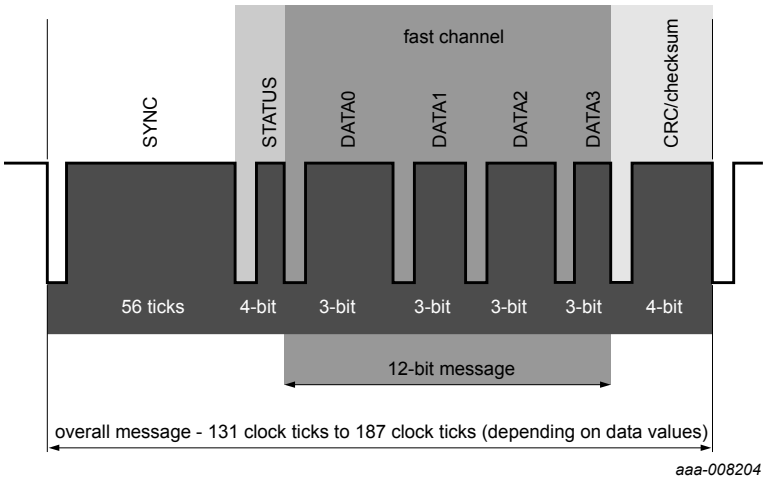


Figure 8. High-speed 12-bit message format frame H.3

Table 12. High-speed 12-bit message format: frame

SYNC	STATUS	DATA0	DATA1	DATA2	DATA3	CRC
-	diagnostic and pre-warning	D0[1]	D1	D2	D3[2]	-
-		12-bit angular value				-

[1] MSN.
[2] LSN.

Table 13. DATA nibbles D0 to D3: angular value

D0[1]	D1	D2	D3[2]	H.3	
				12-bit value	Angle/mode
0000	0000	0000	0000	0	initialization
0000	0000	0000	0001	1	0°
:	:	:	:	:	:
0111	0111	0111	0000	4088	α_{max}
0111	0111	0111	0001	4089	reserved
0111	0111	0111	0010	4090	diagnostic mode[3]
0111	0111	0111	:	:	reserved
0111	0111	0111	0111	4095	reserved

[1] MSN.
[2] LSN.
[3] For detailed diagnostic information, the serial data communication can be enabled.

For the 12-bit high-speed mode H.3, the clamping levels must be set to the correct values to comply with the SAE J2716 SENT specification. CLAMP_HIGH = 4088, CLAMP_LOW = 1. Otherwise angular values overwrite the reserved data range for diagnostic information.

8.10 Enhanced serial data communication

Beside the normal message transmission, also a slow serial data communication is realized using bit 2 and bit 3 of the STATUS nibble. The slow channel message stretches over 18 consecutive SENT frames and contains sensor temperature, supply voltage, diagnostic/status information, and user-programmable messages. These messages comply with the enhanced serial data message format with 8-bit message ID and 12-bit message data described in the SAE J2716 SENT specification. Table 14 shows the serial message cycle that is constantly repeated when enhanced serial data communication is enabled.

Table 14. Serial message schedule

Message number in serial message cycle	8-bit message ID	Definition	Comment
1	01h	diagnostic status code	see Table 15
2	23h	sensor temperature	see Table 21
3	1Ch	supply voltage	see Table 20
4	03h	sensor type	see Table 17
5	29h	sensor ID	see Table 22
6	05h	manufacturer code	see Table 18
7	06h	SENT revision	see Table 19
8	01h	diagnostic status code	see Table 15
9	23h	sensor temperature	see Table 21
10	1Ch	supply voltage	see Table 20
11	90h	OEM code 1	see Table 23
12	91h	OEM code 2	see Table 24
13	92h	OEM code 3	see Table 25
14	93h	OEM code 4	see Table 26
15	94h	OEM code 5	see Table 27
16	95h	OEM code 6	see Table 28
17	96h	OEM code 7	see Table 29
18	97h	OEM code 8	see Table 30

8.10.1 Enhanced serial messages

Table 15. Diagnostic status code message

8-bit ID	12-bit code	Definition	Comment
01h	000h	no error	normal operation
	001h	OOR HIGH[1]	output value above OOR_HIGH register
	002h	OOR LOW[1]	output value below OOR_LOW register
	003h to 019h	reserved	
	020h	undervoltage[1]	V_{DD} below SENT_SETTING2[13:12]
	021h	overvoltage[1]	V_{DD} above SENT_SETTING2[15:14]
	022h	temperature[1]	application-specific integrated circuit (ASIC) temperature above SENT_SETTING2[11:7]
	023h	single-bit error[1]	CTRL1[10]
	024h to 800h	reserved	
	801h to FFFh	automotive safety integrity level (ASIL) error code	see Table 16

[1] If enabled, pre-warning is indicated and bit 1 of STATUS nibble is set.

Table 16. ASIL error code

Bit	Description	Safety mechanism
11 (MSB)	device in diagnostic mode CTRL1[14] (ASIL_STATUS_CODE[11])	-
10	angular range check	SM-12
9	CORDIC range check	SM-11
8	data adder check	SM-10
7	SD-ADC range check	SM-09
6	built-in self-test (BIST) encoding check	SM-08
5	control signal check and BIST completion check	SM-06 and SM-07
4	adjusted angle calculation check	SM-05
3	data conversion check	SM-04
2	data division check	SM-03
1	inverted angle calculation check	SM-02
0 (LSB)	magnetic field conversion check	SM-01

Table 17. SENSOR_TYPE[3:0] – channel 1/2 sensor type message

8-bit ID	12-bit code	Definition	Comment
03h	051h[1]	acceleration pedal position 1 or acceleration pedal position 2	0000b
	052h[1]	acceleration pedal position 1 or secure sensor	0001b
	053h[1]	acceleration pedal position 2 (redundant signal) or secure sensor	0010b
	054h[1]	throttle position 1 or throttle position 2	0011b
	055h[1]	throttle position 1 or secure sensor	0100b
	056h[1]	throttle position 2 (redundant signal) or secure sensor	0101b
	059h[1]	angle position	0110b
	05Ah[1]	angle position or secure sensor	0111b
	062h[2]	angle position (high speed) H.3 protocol format	1000b
	063h[2]	angle position 1 or angle position 2 H.1 protocol format	1001b
	064h[2]	angle position or secure sensor H.4 protocol format	1010b
	066h[2]	reserved for angle position sensors	1011b
	000h	reserved	1101b to 1111b

[1] Compliant with SAE JAN2010 rev 3 only.
[2] Compliant with SAE APR2016 rev 4 only.

Table 18. Manufacturer code message

8-bit ID	12-bit code	Definition	Comment
05h	04Eh	NXP Semiconductors	fix value

Table 19. SENT_REVISION[1:0] – SENT standard revision message

8-bit ID	12-bit code	Definition	Comment
06h	000h	not specified	00b
	002h	FEB2008 rev 2	01b
	003h	JAN2010 rev 3	10b
	004h	APR2016 rev 4	11b

Table 20. Supplementary data channel #3,1: sensor supply voltage

8-bit ID	12-bit code	Definition	Comment
1Ch	000h to 1FFh	9-bit sensor supply voltage	V_{DD} [V] = (digital value [LSB] + 33) / 58
	200h to FFFh	reserved	

Table 21. Supplementary data channel #4,1: sensor temperature value

8-bit ID	12-bit code	Definition	Comment
23h	000h to 0FFh	8-bit sensor temperature	000h: −45 °C to 0FFh: +210 °C
	100h to FFFh	reserved	

Table 22. SENSOR_ID – sensor ID #1 message

8-bit ID	12-bit code	Definition	Comment
29h	000h	sensor ID1	0b
	FFFh	sensor ID2	1b

Table 23. OEM_CODE_1[11:0] – OEM code 1 message

8-bit ID	12-bit code	Definition	Comment
90h	000h to FFFh	OEM code 1	user-programmable data content

Table 24. OEM_CODE_2[11:0] – OEM code 2 message

8-bit ID	12-bit code	Definition	Comment
91h	000h to FFFh	OEM code 2	user-programmable data content

Table 25. OEM_CODE_3[11:0] – OEM code 3 message

8-bit ID	12-bit code	Definition	Comment
92h	000h to FFFh	OEM code 3	user-programmable data content

Table 26. OEM_CODE_4[11:0] – OEM code 4 message

8-bit ID	12-bit code	Definition	Comment
93h	000h to FFFh	OEM code 4	user-programmable data content

Table 27. OEM_CODE_5[11:0] – OEM code 5 message

8-bit ID	12-bit code	Definition	Comment
94h	000h to FFFh	OEM code 5	user-programmable data content

Table 28. OEM_CODE_6[11:0] – OEM code 6 message

8-bit ID	12-bit code	Definition	Comment
95h	000h to FFFh	OEM code 6	user-programmable data content

Table 29. OEM_CODE_7[11:0] – OEM code 7 message

8-bit ID	12-bit code	Definition	Comment
96h	000h to FFFh	OEM code 7	user-programmable data content

Table 30. OEM_CODE_8[11:0] – OEM code 8 message

8-bit ID	12-bit code	Definition	Comment
97h	000h to FFFh	OEM code 8	user-programmable data content

8.11 SENT diagnostic

The SENT standard specifies different methods to transmit diagnostic information. These methods are used in multiple combinations, depending on the SENT revision, protocol format, and device configuration.

8.11.1 STATUS nibble diagnostic

Bit 0 and bit 1 of the STATUS nibble can be used to signal the diagnostic state while the DATA nibbles still contain an angular value at the same time. The CRC nibble does not include the STATUS nibble, thus the receiver do not detect an erroneous STATUS nibble.

8.11.1.1 Diagnostic bit

The device defines bit 0 of the STATUS nibble as diagnostic bit. In case the device is in diagnostic mode the diagnostic bit is set to logic 1.

The diagnostic bit can be disabled and permanently set to logic 0 via the mask STATUS nibble bits in the SENT_SETTING2 register in the non-volatile memory; see Table 49.

8.11.1.2 Pre-warning bit

Bit 1 is a pre-warning indication which is set while the device is still in normal mode, but one of the following conditions occurred:

- The angular value is above the programmed upper out of range (OOR) threshold; see Table 51.
- The angular value is below the programmed lower OOR threshold; see Table 51.
- Corrected single-bit error of the non-volatile memory (EDC); see Section 10.1.
- The temperature is above the programmed temperature threshold; see Table 49.
- Overvoltage: The supply voltage is above the programmed upper voltage threshold; see Table 49.
- Undervoltage: The supply voltage is below the programmed lower voltage threshold; see Table 49.

The pre-warning bit can be disabled and permanently set to logic 0 via the mask STATUS nibble bits in the SENT_SETTING2 register in the non-volatile memory; see Table 49.

8.11.2 Fast channel diagnostic value

Some protocol formats define a reserved data range in the fast channel communication for signaling diagnostic status instead of an angular value in the SENT transmission.

The KMZ80 generates a specific diagnostic value instead of an angular value in case the device is in diagnostic mode. The diagnostic value depends on the selected protocol format according to Table 31.

Table 31. Fast channel diagnostic value

Protocol format	Normal mode	Diagnostic mode
A.1	angular value	4095
A.3	angular value	angular value
H.1	angular value	4090
H.3	angular value	4090
H.4	angular value	4090

8.11.3 Enhanced serial protocol diagnostic status code message

Detailed diagnostic and pre-warning information is transmitted in the diagnostic status code message ID 01h of the slow channel message transmission. Therefore, the enhanced serial protocol must be enabled via the ESP bit in the SENT_SETTING1 register in the non-volatile memory; see Table 49. A description of the diagnostic status code message is given in Table 15.

9 Output characteristic

The MPC defines the output transfer characteristic. For this purpose, up to 17 calibration points define the range between programmed reference angle and set maximum angle.

Three different MPC types are available, see Table 49, whereas in each mode either a positive or a negative slope can be programmed. MPC17 and MPC7 enable an improved linearization of the output characteristic.

Furthermore, curve shapes can be customized in accordance with application requirements.

9.1 No MPC mode

No MPC mode refers to the conventional linear output characteristic defined by zero angle (ZERO_ANGLE), angular range (RANGE_DETECTION), clamp switch angle (CLAMP_SWITCH), and clamping levels (CLAMP_LOW and CLAMP_HIGH).

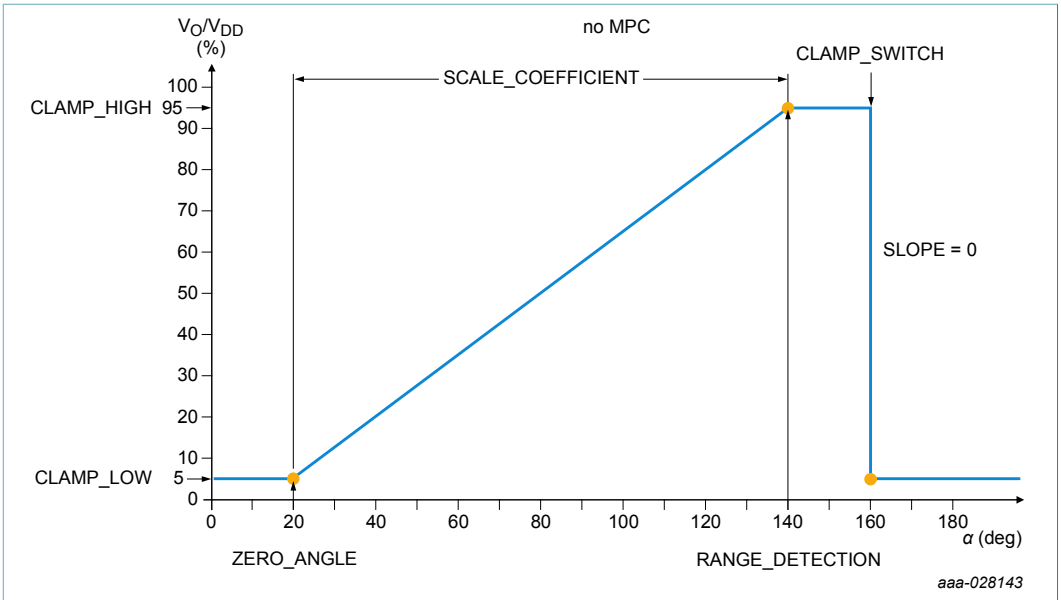


Figure 9. No MPC mode

9.2 MPC17 mode

MPC17 mode enables curve shaping by 17 equidistant calibration points. For this purpose 16 coefficients (MPC_COEFFICIENTn) can be programmed, see Table 50, to set a specific output level for each calibration point.

In this mode, all points are scaling with the angular range to define calibration coefficients at equidistant positions as shown in Figure 10.

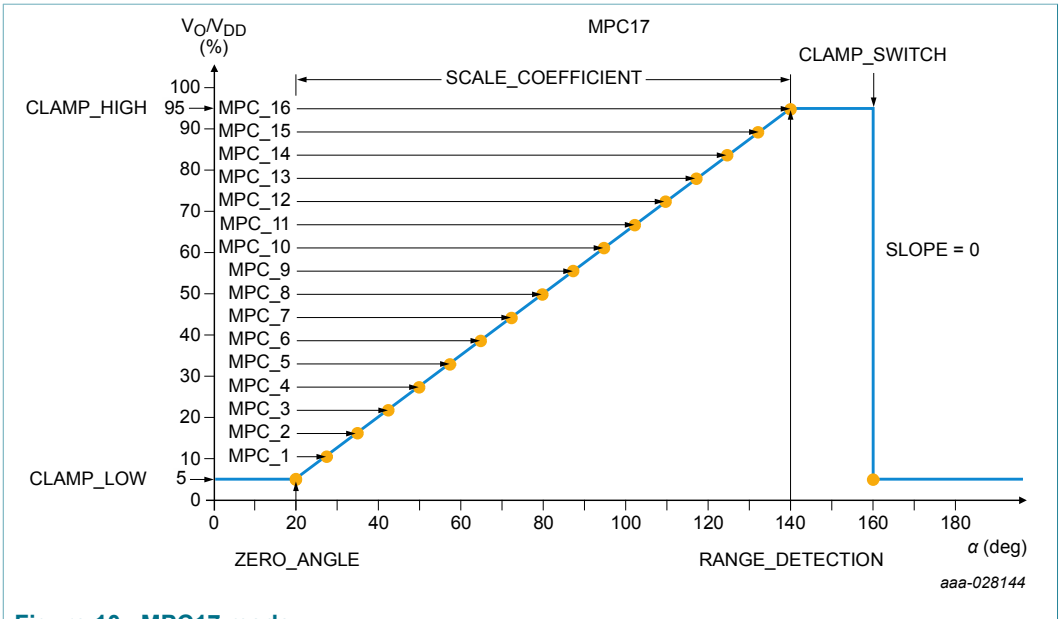


Figure 10. MPC17 mode

9.3 MPC7 mode

MPC7 in contrast provides a set of six freely selectable calibration points defined by angular position (linear Xn), output level (linear Yn), and slope (linear Sn) as shown in Figure 11.

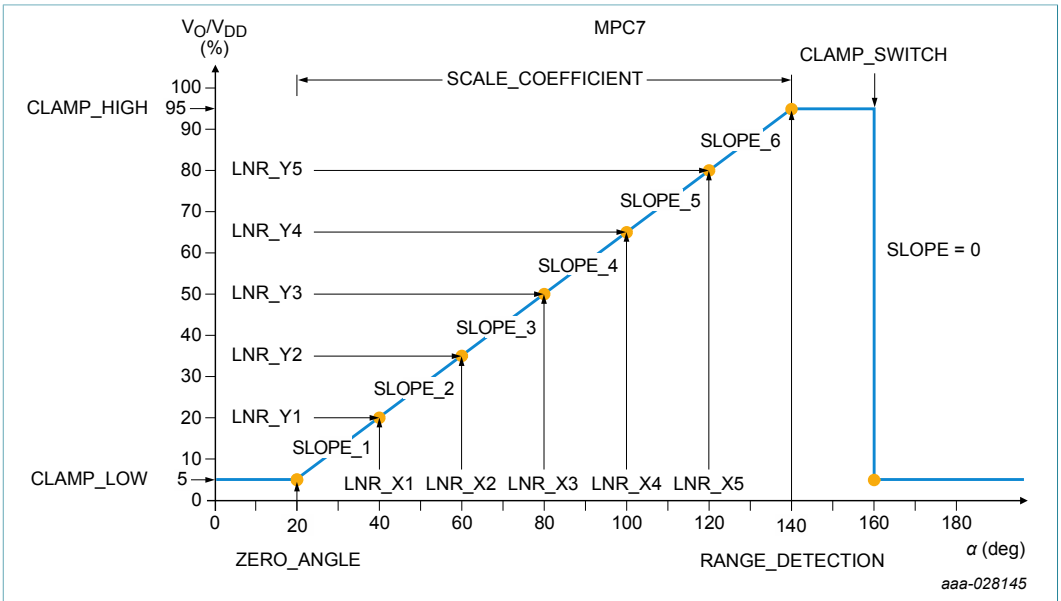


Figure 11. MPC7 mode

10 Diagnostic features

KMZ80 provides following diagnostic features. The safety mechanisms supporting functional safety operation are marked with individual numbers SM-xx. Functional risks are only minimized if all safety mechanisms are enabled as in the default configuration. Thus it is not recommended to switch them off individually.

10.1 NVM CRC (SM-20), NVM EDC check (SM-21), and NVM ECC check (SM-22)

The device includes a supervision of the programmed data. At power-on, a CRC of the non-volatile memory is performed (SM-20). The NVM is split into three customer areas with individual CRCs (CRC1, CRC2, and CRC3) and a manufacturer area which is user access restricted and also CRC protected. Furthermore, the memory is protected against bit errors. Every 16-bit data word is saved internally as a 22-bit word for this purpose. The protection logic corrects any single-bit error in a data word (SM-22), while the sensor continues in normal operation mode. Furthermore, the logic detects double-bit error per word and switches the output into diagnostic mode (SM-21).

10.2 Power-loss detection (SM-18) and GND-loss detection (SM-19)

The power-loss detection circuit enables the detection of an interrupted supply or ground line of the mixed signal IC. If there is a power-loss condition, two internal switches in the sensor are closed, connecting the pin of the analog output to the supply voltage and the ground pin.

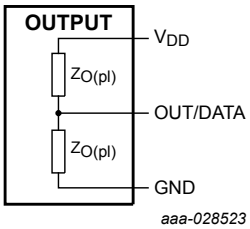


Figure 12. Equivalent output circuit in a power-loss condition

Table 32 describes the power-loss behavior and gives the resulting output voltage depending on the interrupted supply or ground line and the load resistance.

Table 32. Power-loss behavior

Load resistance	Interrupted supply line	Interrupted ground line
$R_{L(ext)}$ > 5 kΩ	$V_O \leq 4\ \%V_{DD}$	$V_O \geq 96\ \%V_{DD}$

10.3 Supply overvoltage detection (SM-16) and undervoltage detection (SM-17)

If the supply voltage is below the switch-off threshold voltage, a status bit is set and the output goes into diagnostic mode. If the supply voltage is above the overvoltage switch-on threshold voltage, the output switches to diagnostic mode. Table 33 describes the system behavior depending on the voltage range of the supply voltage.

Table 33. System behavior for each output mode

Supply voltage	State	Analog mode	SENT mode
0 V to ≅ 1.8 V	startup power	The output buffer drives an active LOW or is powered down, but the switches of the power-loss detection circuit are not fully opened and set the output to a level between ground and half the supply voltage.	high-ohmic output stage; external pull-up resistor defines output voltage
≅ 1.8 V to V_{POR}	power-on reset	The power-loss charge pump is fully operational and turns the switches of the detection circuit off. The output buffer drives an active LOW and sets the output to the lower diagnostic level. During the reset phase, all circuits are in reset and/or power-down mode.	The output buffer drives an active LOW. During the reset phase, all circuits are in reset and/or power-down mode.
V_{POR} to $V_{th(on)}$ or $V_{th(off)}$	initialization	The digital core and the oscillator are active. After reset, the content of the non-volatile memory is copied into the shadow registers. The output buffer drives an active LOW.	The digital core and the oscillator are active. After reset, the content of the non-volatile memory is copied into the shadow registers. The output buffer drives an active LOW.

Supply voltage	State	Analog mode	SENT mode
$V_{th(on)}$ or $V_{th(off)}$ to minimum V_{DD}	functional operation	All analog circuits are active and the measured angle is available at the analog output. Not all parameters are within the specified limits.	All analog circuits are active and the output is set to HIGH for at least 100 µs before SENT transmission starts. Not all parameters are within the specified limits.
Minimum V_{DD} to maximum V_{DD}	normal operation	All analog circuits are active and the measured angle is available at the analog output. All parameters are within the specified limits.	All analog circuits are active and the measured angle is available at the digital output. All parameters are within the specified limits.
Maximum V_{DD} to $V_{th(ov)}$	functional operation	All analog circuits are active and the measured angle is available at the analog output. Not all parameters are within the specified limits.	All analog circuits are active and the measured angle is available at the digital output. Not all parameters are within the specified limits.
$V_{th(ov)}$ to 18 V	overvoltage	The digital core and the oscillator are active but all other circuits are in power-down mode. The output is set to the lower diagnostic level.	The digital core and the oscillator are active but all other circuits are in power-down mode. The output buffer drives an active LOW.

Table 34 describes the diagnostic behavior and the resulting output voltage depending on the error case. Furthermore the duration and termination condition to enter and leave the diagnostic mode are given, respectively.

Table 34. Diagnostic behavior

Diagnostic condition	Duration	Output	Termination condition
Low voltage	20 µs < t < 120 µs	≤ 4 %V_{DD}	functional or normal operation
Overvoltage	20 µs < t < 120 µs	≤ 4 %V_{DD}	functional or normal operation
Checksum error	n.a.	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]	power-on reset[2]
Double-bit error	n.a.	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]	power-on reset[2]
Power-loss	≤ 2 ms	≤ 4 %V_{DD} or ≥ 96 %V_{DD}; see Table 32	power-on reset

[1] Depending on the diagnostic level setting.
[2] Status bit stays set in command register until power-on reset.

10.4 Oscillator monitoring (SM-13, SM-14 and SM-15)

If the oscillator frequency differs from the target frequency by more than ±30 % or the oscillator stops, status bit 7 of CTRL1 register is set and the output goes into diagnostic mode; see Table 48. If the oscillator frequency differs by more than ±10 %, the SENT timing can violate the SAE J2716 SENT specification.

10.5 Safe assure - ASIL control unit

The ASIL control includes a state machine, which is a 4-bit up-counter that defines time slots. The different time slots are used to trigger dedicated BISTs. To enable or disable the complete ASIL control unit globally, use the BIST bit in ASIL_SETTING register; see Table 49. The NVM register setting enables or disables individually each integrated test.

In case a self-test was performed a ready flag is generated to reset the start test trigger signals. In case no reset signal is found, the output is set to diagnostic mode.

10.5.1 Timing description

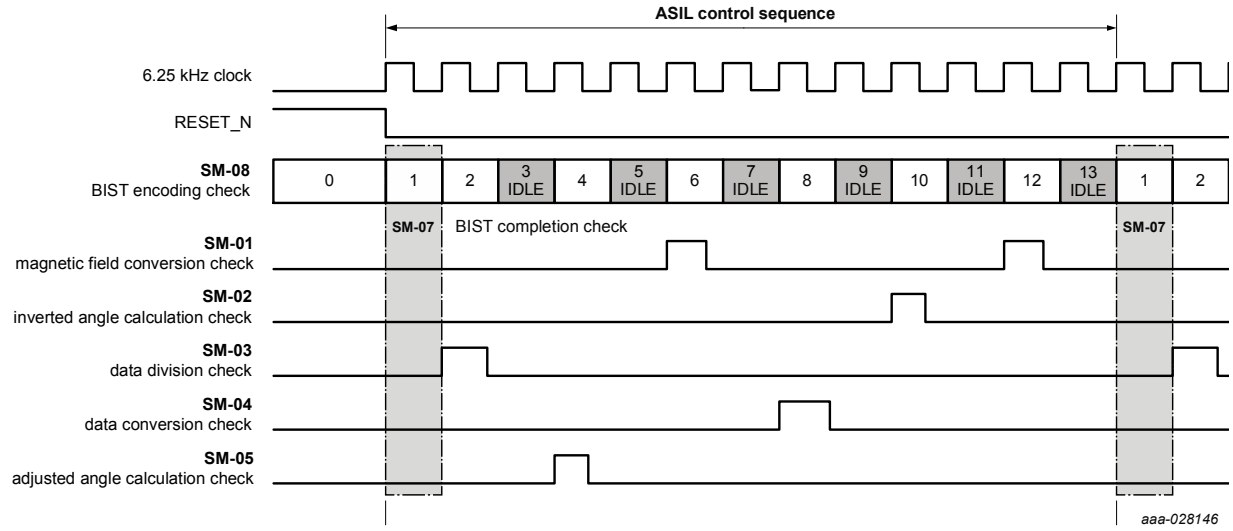


Figure 13. Sequence state register and start flags for integrated self-checks

10.5.2 User selectable BIST

To enable the BISTs SM-01 to SM-06 set the BIST bit in ASIL_SETTING register; see Table 49. User selectable self-tests can be enabled or masked separately as described in the following subsections.

10.5.2.1 Magnetic field conversion check (SM-01)

The output amplitude of an AMR sensor has a strong temperature dependency. This physical effect is used to check the plausibility of the AMR signals. The magnetic field conversion check compares a temperature value, which is based on an on-chip temperature sensor with the temperature information based on the AMR amplitude. In case the magnet is removed, the AMR amplitude goes down, and the magnetic field conversion check indicates this failure mode. Furthermore, this check can be switched off separately with the magnetic field conversion check bit of the ASIL_SETTING register; see Table 49.

In case the on-chip temperature sensor fails, the product goes to diagnostic condition, even if the angle data path is not directly affected from this failure mode.

10.5.2.2 Inverted angle calculation check (SM-02)

The inverted angle calculation check calculates a second internal output angle value. Based on the customer settings the second angle value is an exact inverted copy of the main data path angle. The check compares the sum of both calculated angle values with the sum of both adjusted customer clamping levels. In case the post-CORDIC integrated adder and multiplier are in normal operating mode the result is equal. Furthermore, this check can be switched off separately with the inverted angle calculation check bit of the ASIL_SETTING register; see Table 49.

In case internal post-memory addressing, post-multiplier or post-adder fails, the product goes into diagnostic mode.

10.5.2.3 Data division check (SM-03)

The main data path division module is only used in MPC17 mode. Nevertheless, the integrated data division check uses the same hardware, which is used by the post-CORDIC. This test performs a test division with a known result. To execute the data division check, also the post-adder and the post-memory addressing are used. Furthermore, this check can be switched off separately with the data division check bit of the ASIL_SETTING register; see Table 49.

In case internal post-memory addressing, post-adder or division fails, the product goes into diagnostic mode.

10.5.2.4 Data conversion check (SM-04)

The data conversion check checks the CORDIC module, which is used for all modes. For testing, internal cos and –sin signals are used to calculate an inverted CORDIC angle. The sum of the main data path CORDIC angle and the inverted CORDIC angle must be zero. Furthermore, this check can be switched off separately with the data conversion check bit of the ASIL_SETTING register; see Table 49.

In case internal subblocks of the CORDIC module (shift register, adder, state-controller) fail, the product goes into diagnostic mode.

10.5.2.5 Adjusted angle calculation check (SM-05)

The zero angle corrected CORDIC signal is one of the most important signals within the system. This signal is used for the main data path angle value and for the segment detection for MPC7 and MPC17 mode. The integrated adjusted angle calculation check compares the post-CORDIC zeroed result with a redundant calculated CORDIC zeroed signal. The arithmetic logic unit (ALU) ASIL module performs this redundant calculation. Furthermore, this check can be switched off separately with the adjusted angle calculation check bit of the ASIL_SETTING register; see Table 49.

In case the redundant calculation of the ALU ASIL check fails, the product goes into diagnostic mode, even if the angle data path is not directly affected from this failure mode.

10.5.3 Fixed internal diagnostics

The following internal diagnostics are permanently enabled and automatically executed. The corresponding flags can be masked individually.

10.5.3.1 Control signal check (SM-06)

Checks, if the main data path processing was performed correctly. This status flag can be masked with the mask control signal check bit of the ASIL_SETTING register; see Table 49.

10.5.3.2 BIST completion check (SM-07)

Checks, if all selected self-tests were executed without any errors. In case a failure mode occurs at one selected test, the BIST completion check flag indicates this failure latest after 2.08 ms.

In case the ASIL control block fails, the product goes into diagnostic mode, even if the angle data path is not directly affected from this failure mode. This status flag can be masked with the mask BIST completion check bit of the ASIL_SETTING register; see Table 49.

10.5.3.3 BIST encoding check (SM-08)

The ASIL control module provides the test sequence number for all implemented self-tests. To prove that this module is running normal, the state register of the ASIL control module is coded with a parity bit to prevent single bit failures.

In case the ASIL control block fails, the product goes into diagnostic mode, even if the angle data path is not directly affected from this failure mode. This status flag can be masked with the mask BIST encoding check bit of the ASIL_SETTING register; see Table 49.

10.5.3.4 SD-ADC range check (SM-09)

The SD-ADC is not using full scale range. Some part is reserved to detect overflows. In case the filter result is larger than 95 % (including the gain factor) the overflow flag is set. This status flag can be masked with the mask SD-ADC range check bit of the ASIL_SETTING register; see Table 49.

10.5.3.5 Data adder check (SM-10)

The pre-CORDIC adder is used for AMR offset cancelation, new AMR offset value calculation, and temperature calculation from the auxiliary ADC. In case overflow occurs, the bit is set. This status flag can be masked with the mask data adder check bit of the ASIL_SETTING register; see Table 49.

10.5.3.6 CORDIC range check (SM-11)

The CORDIC block, which is used for angle calculation, is using internally more than 16 bit. To prevent a wrap-around for unexpected sin/cos input signals, the block has a built-in overflow monitor. In case overflow occurs, a status flag is set. This status flag can be masked with the mask CORDIC range check bit of the ASIL_SETTING register; see Table 49.

10.5.3.7 Angular range check (SM-12)

The clamp control checks the plausibility of the internal status flags coming from the clamp and range detection. In case the clamp switch angle position was detected before the range position, the flag is set. This status flag can be masked with the mask angular range check bit of the ASIL_SETTING register; see Table 49.