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KSZ8041TL/FTL/MLL

10Base-T/100Base-TX/100Base-FX Physical Layer Transceiver

Data Sheet Rev. 1.2

General Description

The KSZ8041TL is a single supply 10Base-T/100Base-TX Physical Layer Transceiver, which provides MII/RMII/SMII interfaces to transmit and receive data. It utilizes a unique mixed-signal design to extend signaling distance while reducing power consumption.

HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables.

Micrel LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling.

The KSZ8041TL represents a new level of features and performance and is an ideal choice of physical layer transceiver for 10Base-T/100Base-TX applications.

The KSZ8041FTL has all the identical rich features of the KSZ8041TL plus 100Base-FX support for fiber and media converter applications.

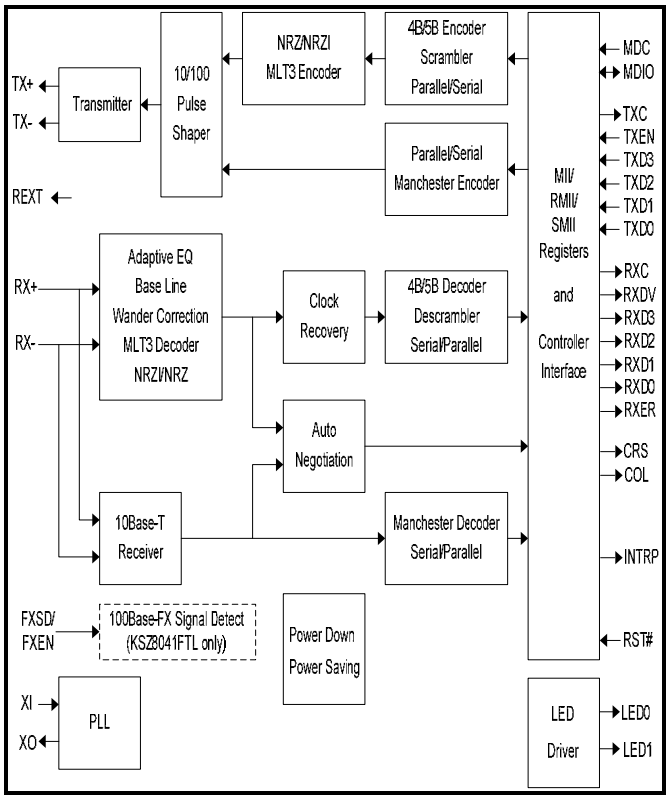
The KSZ8041MLL is the basic 10Base-T/100Base-TX Physical Layer Transceiver version with MII support.

The KSZ8041TL and KSZ8041FTL are available in 48-pin, lead-free TQFP packages. The KSZ8041MLL is provided in the 48-pin, lead-free LQFP package (See Ordering Information).

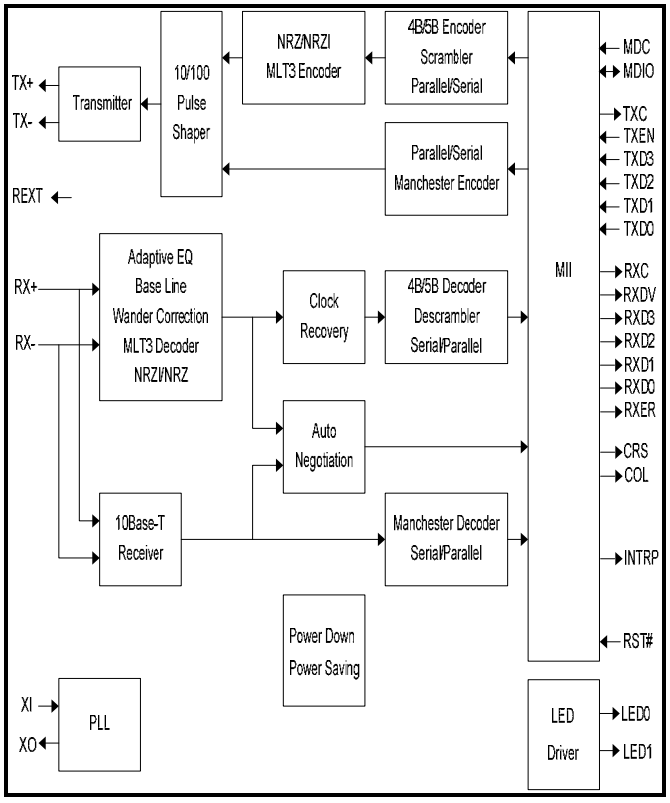
Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram

KSZ8041TL/FTL



KSZ8041MLL



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Features

- Single-chip 10Base-T/100Base-TX physical layer solution
- Fully compliant to IEEE 802.3u Standard
- Low power CMOS design, power consumption of <180mW
- HP auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Robust operation over standard cables
- LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling
- Fiber support: 100Base-FX (KSZ8041FTL only),
- Back-to-Back mode support for 100Mbps repeater or media converter
- MII interface support
- RMII interface support with external 50MHz system clock (KSZ8041TL/FTL only)
- SMII interface support with external 125MHz system clock and 12.5MHz sync clock from MAC (KSZ8041TL/FTL only)
- MIIM (MDC/MDIO) management bus to 12.5MHz for rapid PHY register configuration
- Interrupt pin option
- Programmable LED outputs for link, activity and speed
- Power down and power saving modes
- Single power supply (3.3V)
- Built-in 1.8V regulator for core
- Available packages:
  - 48-pin LQFP (KSZ8041MLL)
  - 48-pin TQFP (KSZ8041TL/FTL)

Applications

- Printer
- LOM
- Game Console
- IPTV
- IP Phone
- IP Set-top Box
- Media Converter

Ordering Information

Part Number (marking)	Ordering Number	Temp. Range	Package	Lead Finish	Description
KSZ8041MLL	KSZ8041MLL	0°C to 70°C	48-Pin LQFP	Pb-Free	MII, 10/100 Copper, C-Temp, 48-LQFP
KSZ8041TL	KSZ8041TL	0°C to 70°C	48-Pin TQFP	Pb-Free	MII / RMII, 10/100 Copper, C-Temp, 48-TQFP
KSZ8041TLI (1)	KSZ8041TLI	-40°C to 85°C	48-Pin TQFP	Pb-Free	MII / RMII, 10/100 Copper, I-Temp, 48-TQFP
KSZ8041FTL	KSZ8041FTL	0°C to 70°C	48-Pin TQFP	Pb-Free	MII / RMII, 100Base-FX Fiber, C-Temp, 48-TQFP
KSZ8041FTLI (1)	KSZ8041FTLI	-40°C to 85°C	48-Pin TQFP	Pb-Free	MII / RMII, 100Base-FX Fiber, I-Temp, 48-TQFP
KSZ8041TL (1)	KSZ8041TL-S	0°C to 70°C	48-Pin TQFP	Pb-Free	SMII, 10/100 Copper, C-Temp, 48-TQFP
KSZ8041TLI (1)	KSZ8041TLI-S	-40°C to 85°C	48-Pin TQFP	Pb-Free	SMII, 10/100 Copper, I-Temp, 48-TQFP
KSZ8041FTL (1)	KSZ8041FTL-S	0°C to 70°C	48-Pin TQFP	Pb-Free	SMII, 100Base-FX Fiber, C-Temp, 48-TQFP
KSZ8041FTLI (1)	KSZ8041FTLI-S	-40°C to 85°C	48-Pin TQFP	Pb-Free	SMII, 100Base-FX Fiber, I-Temp, 48-TQFP

Note:

1. Contact factory for lead time.

Revision History

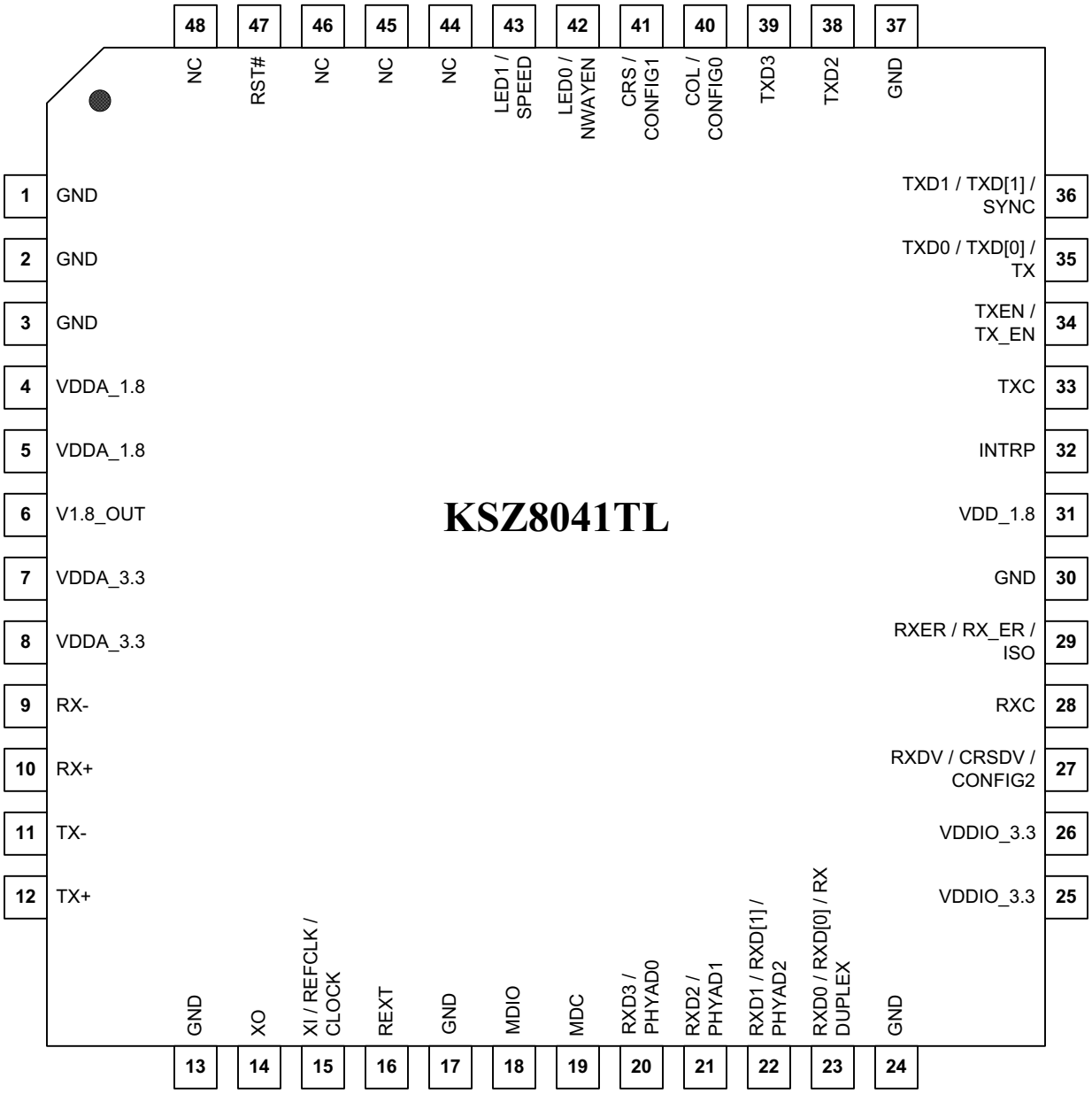
Revision	Date	Summary of Changes
1.0	12/21/06	Data sheet created.
1.1	4/27/07	Added maximum MDC clock speed. Added 40K +/-30% to note 1 of Pin Description and Strapping Options tables for internal pull-ups/pull-downs. Changed Model Number in Register 3h – PHY Identifier 2. Changed polarity (swapped definition) of DUPLEX strapping pin. Removed DUPLEX strapping pin update to Register 4h – Auto-Negotiation Advertisement bits [8, 6]. Added Back-to-Back mode for KSZ8041TL. Added Symbol Error to MII/RMII Receive Error description and Register 15h – RXER Counter. Added a 100pF capacitor on REXT (pin 16) in Pin Description table.
1.2	12/9/09	Updated Ordering Information. Changed MDIO hold time (min) from 10ns to 4ns. Added thermal resistance (θ_{JC}). Added chip maximum current consumption. Added LED drive current. Renamed Register 3h bits [3:0] to “manufacturer’s revision number” and changed default value to “Indicates silicon revision.” Updated RMII output delay for CRSDV and RXD[1:0] output pins. Added support for Asymmetric PAUSE in register 4h bit [11]. Added control bits for 100Base-TX preamble restore (register 14h bit [7]) and 10Base-T preamble restore (register 14h bit [6]). Changed strapping pin definition for CONFIG[2:0] = 100 from “PCS Loopback” to “MII 100Mbps Preamble Restore.” Corrected MII timing for t_{RLAT}, t_{CRS1}, t_{CRS2}. Added SMII timing. Added KSZ8041MLL device and updated entire data sheet accordingly. Added 48-Pin LQFP package information.

Contents

List of Figures

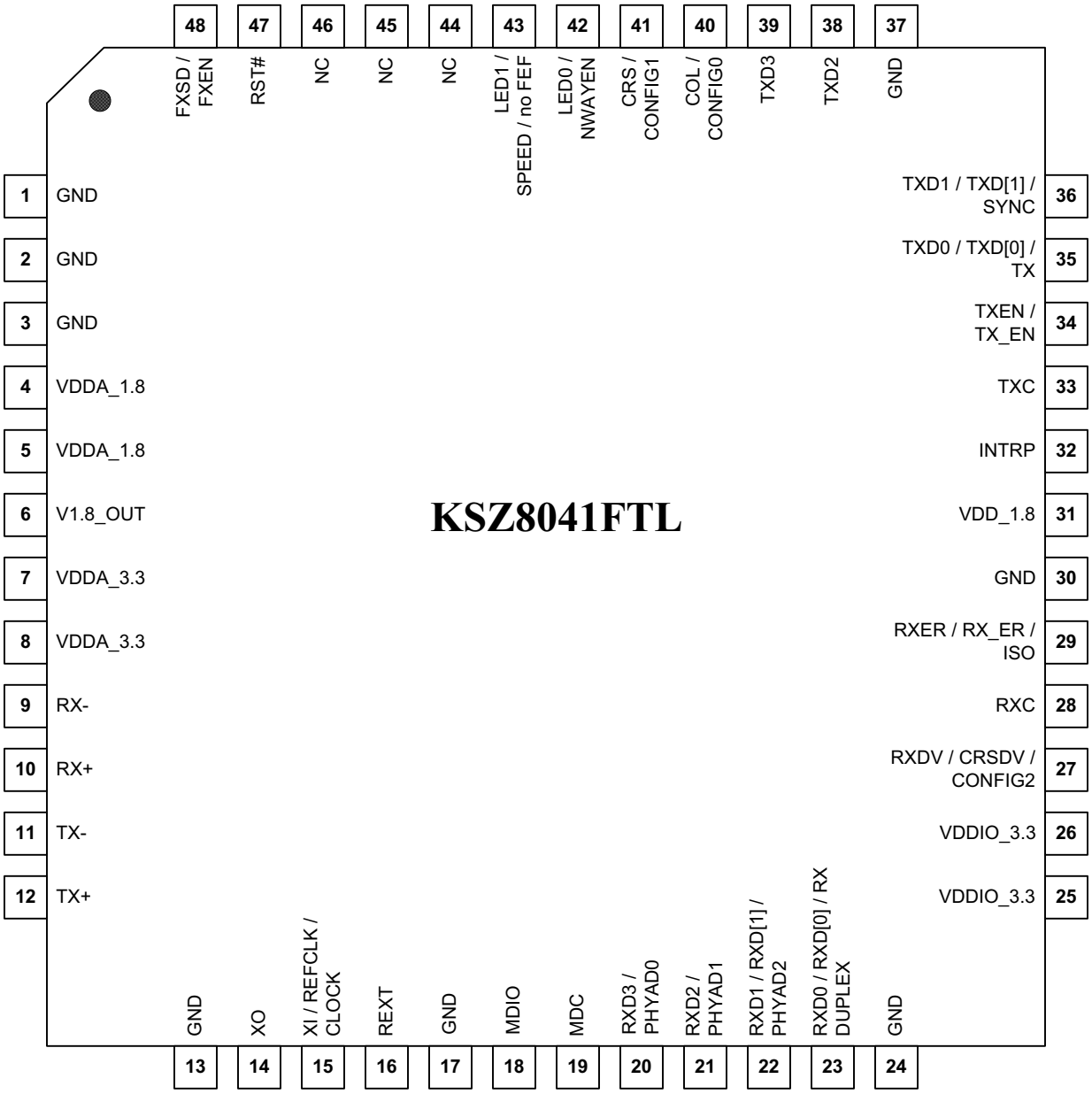
List of Tables

Pin Configuration – KSZ8041TL



48-Pin TQFP

Pin Configuration – KSZ8041FTL



48-Pin TQFP

Pin Description- KSZ8041TL/FTL

Pin Number	Pin Name	Type[1]	Pin Function
1	GND	Gnd	Ground
2	GND	Gnd	Ground
3	GND	Gnd	Ground
4	VDDA_1.8	P	1.8V analog V_{DD}
5	VDDA_1.8	P	1.8V analog V_{DD}
6	V1.8_OUT	P	1.8V output voltage from chip
7	VDDA_3.3	P	3.3V analog V_{DD}
8	VDDA_3.3	P	3.3V analog V_{DD}
9	RX-	I/O	Physical receive or transmit signal (- differential)
10	RX+	I/O	Physical receive or transmit signal (+ differential)
11	TX-	I/O	Physical transmit or receive signal (- differential)
12	TX+	I/O	Physical transmit or receive signal (+ differential)
13	GND	Gnd	Ground
14	XO	O	Crystal feedback This pin is used only in MII mode when a 25MHz crystal is used. This pin is a no connect if oscillator or external clock source is used, or if RMII mode or SMII mode is selected.
15	XI / REFCLK / CLOCK	I	Crystal / Oscillator / External Clock Input MII Mode: 25MHz +/-50ppm (crystal, oscillator, or external clock) RMII Mode: 50MHz +/-50ppm (oscillator, or external clock only) SMII Mode: 125MHz +/-100ppm (oscillator, or external clock only)
16	REXT	I/O	Set physical transmit output current Connect a 6.49KΩ resistor in parallel with a 100pF capacitor to ground on this pin. See KSZ8041TL-FTL reference schematics.
17	GND	Gnd	Ground
18	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7KΩ pull-up resistor.
19	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
20	RXD3 / PHYAD0	Ipu/O	MII Mode: Receive Data Output[3][2] / Config. Mode: The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See “Strapping Options” section for details.
21	RXD2 / PHYAD1	Ipd/O	MII Mode: Receive Data Output[2][2] / Config. Mode: The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See “Strapping Options” section for details.
22	RXD1 / RXD[1] / PHYAD2	Ipd/O	MII Mode: Receive Data Output[1][2] / RMII Mode: Receive Data Output[1][3] / Config. Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See “Strapping Options” section for details.

Pin Number	Pin Name	Type[1]	Pin Function
23	RXD0 / RXD[0] / RX DUPLEX	Ipu/O	MII Mode: Receive Data Output[0][2] / RMII Mode: Receive Data Output[0][3] / SMII Mode: Receive Data and Control[4] / Config. Mode: Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See “Strapping Options” section for details.
24	GND	Gnd	Ground
25	VDDIO_3.3	P	3.3V digital V_{DD}
26	VDDIO_3.3	P	3.3V digital V_{DD}
27	RXDV / CRSDV / CONFIG2	Ipd/O	MII Mode: Receive Data Valid Output / RMII Mode: Carrier Sense/Receive Data Valid Output / Config. Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See “Strapping Options” section for details.
28	RXC	O	MII Mode: Receive Clock Output.
29	RXER / RX_ER / ISO	Ipd/O	MII Mode: Receive Error Output / RMII Mode: Receive Error Output / Config. Mode: The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See “Strapping Options” section for details.
30	GND	Gnd	Ground
31	VDD_1.8	P	1.8V digital V_{DD}
32	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
33	TXC	I/O	MII Mode: Transmit Clock Output MII Back-to Back Mode: Transmit Clock Input
34	TXEN / TX_EN	I	MII Mode: Transmit Enable Input / RMII Mode: Transmit Enable Input
35	TXD0 / TXD[0] / TX	I	MII Mode: Transmit Data Input[0][5] / RMII Mode: Transmit Data Input[0][6] / SMII Mode: Transmit Data and Control[7]
36	TXD1 / TXD[1] / SYNC	I	MII Mode: Transmit Data Input[1][5] / RMII Mode: Transmit Data Input[1][6] / SMII Mode: SYNC Clock Input
37	GND	Gnd	Ground
38	TXD2	I	MII Mode: Transmit Data Input[2][5] /
39	TXD3	I	MII Mode: Transmit Data Input[3][5] /
40	COL / CONFIG0	Ipd/O	MII Mode: Collision Detect Output / Config. Mode: The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See “Strapping Options” section for details.
41	CRS / CONFIG1	Ipd/O	MII Mode: Carrier Sense Output / Config. Mode: The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See “Strapping Options” section for details.

Pin Number	Pin Name	Type(1)	Pin Function
42 **(KSZ8041TL)**	LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config. Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See "Strapping Options" section for details. The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Link/Activity** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON Activity / Toggle / Blinking **LED mode = [01]** **Link** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON **LED mode = [10]** Reserved **LED mode = [11]** Reserved
42 **(KSZ8041FTL)**	LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config. Mode: If copper mode (FXEN=0), latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. If fiber mode (FXEN=1), this pin configuration is always strapped to disable Auto-Negotiation. See "Strapping Options" section for details. The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Link/Activity** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON Activity / Toggle / Blinking **LED mode = [01]** **Link** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON **LED mode = [10]** Reserved **LED mode = [11]** Reserved

Pin Number	Pin Name	Type(1)	Pin Function
43 **(KSZ8041TL)**	LED1 / SPEED	Ipu/O	LED Output: Programmable LED1 Output / Config. Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See "Strapping Options" section for details. The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Speed** / **Pin State** / **LED Definition** 10BT / H / OFF 100BT / L / ON **LED mode = [01]** **Activity** / **Pin State** / **LED Definition** No Activity / H / OFF Activity / Toggle / Blinking **LED mode = [10]** Reserved **LED mode = [11]** Reserved
43 **(KSZ8041FTL)**	LED1 / SPEED / no FEF	Ipu/O	LED Output: Programmable LED1 Output / Config. Mode: If copper mode (FXEN=0), latched as SPEED (register 0h, bit 13) during power-up / reset. If fiber mode (FXEN=1), latched as no FEF (no Far-End Fault) during power-up / reset. See "Strapping Options" section for details. The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Speed** / **Pin State** / **LED Definition** 10BT / H / OFF 100BT / L / ON **LED mode = [01]** **Activity** / **Pin State** / **LED Definition** No Activity / H / OFF Activity / Toggle / Blinking **LED mode = [10]** Reserved **LED mode = [11]** Reserved
44	NC	-	No connect
45	NC	-	No connect
46	NC	-	No connect

Pin Number	Pin Name	Type(1)	Pin Function
47	RST#	I	Chip Reset (active low)
48 **(KSZ8041TL)**	NC	-	No connect
48 **(KSZ8041FTL)**	FXSD / FXEN	Ipd	FXSD: Signal Detect for 100Base-FX fiber mode FXEN: Fiber Enable for 100Base-FX fiber mode If FXEN=0, fiber mode is disabled. PHY is in copper mode. The default is "0". See "100Base-FX Operation" section for details.

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipd = Input with internal pull-down (40K +/-30%).
   Ipu = Input with internal pull-up (40K +/-30%).
   Opu = Output with internal pull-up (40K +/-30%).
   Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.
2. MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.
3. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.
4. SMII Rx Mode: Receive data and control information are sent in 10 bit segments. In 100MBit mode, each segment represents a new byte of data. In 10MBit mode, each segment is repeated ten times; therefore, every ten segments represent a new byte of data. The MAC can sample any one of every 10 segments in 10MBit mode.
5. MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.
6. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.
7. SMII Tx Mode: Transmit data and control information are received in 10 bit segments. In 100MBit mode, each segment represents a new byte of data. In 10MBit mode, each segment is repeated ten times; therefore, every ten segments represent a new byte of data. The PHY can sample any one of every 10 segments in 10MBit mode.

Strapping Options- KSZ8041TL/FTL

Pin Number	Pin Name	Type(1)	Pin Function
22 21 20	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are always set to '00'.
27 41 40	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows: **CONFIG[2:0] Mode** 000 MII (default) 001 RMII 010 SMII 011 Reserved – not used 100 MII 100Mbps Preamble Restore 101 RMII back-to-back 110 MII back-to-back 111 Reserved – not used
29	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable During power-up / reset, this pin value is latched into register 0h bit 10.
43 **(KSZ8041TL)**	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
43 **(KSZ8041FTL)**	SPEED /	Ipu/O	If copper mode (FXEN=0), pin strap-in is SPEED mode. Pull-up (default) = 100Mbps Pull-down = 10Mbps During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
	no FEF		If fiber mode (FXEN=1), pin strap-in is no FEF. Pull-up (default) = Enable Far-End Fault Pull-down = Disable Far-End Fault This pin value is latched during power-up / reset.

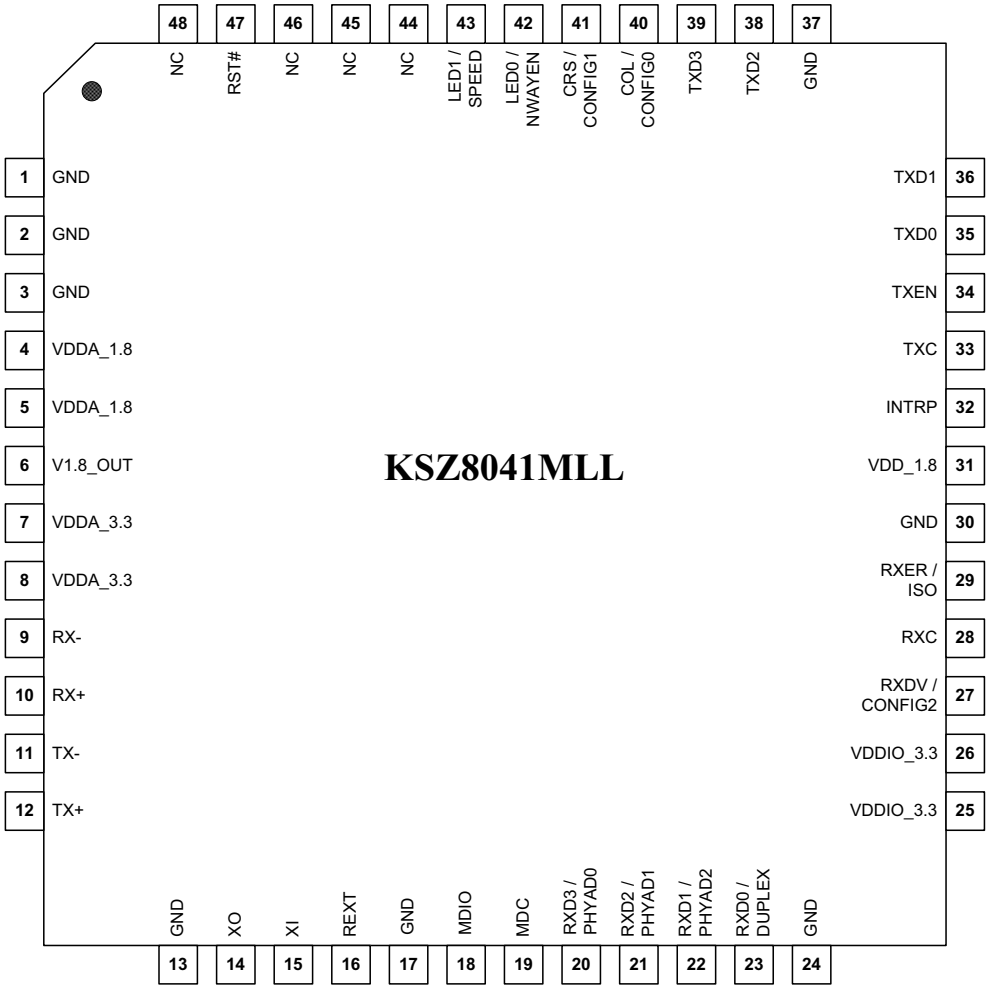
Pin Number	Pin Name	Type[1]	Pin Function
23	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
42 **(KSZ8041TL)**	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.
42 **(KSZ8041FTL)**	NWAYEN	Ipu/O	If copper mode (FXEN=0), pin strap-in is Nway Auto-Negotiation Enable. Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.
			If fiber mode (FXEN=1), this pin configuration is always strapped to disable Auto-Negotiation.

Note:

1. Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII/SMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

Pin Configuration –KSZ8041MLL



48-Pin LQFP

Pin Description– KSZ8041MLL

Pin Number	Pin Name	Type[1]	Pin Function
1	GND	Gnd	Ground
2	GND	Gnd	Ground
3	GND	Gnd	Ground
4	VDDA_1.8	P	1.8V analog V_{DD}
5	VDDA_1.8	P	1.8V analog V_{DD}
6	V1.8_OUT	P	1.8V output voltage from chip
7	VDDA_3.3	P	3.3V analog V_{DD}
8	VDDA_3.3	P	3.3V analog V_{DD}
9	RX-	I/O	Physical receive or transmit signal (- differential)
10	RX+	I/O	Physical receive or transmit signal (+ differential)
11	TX-	I/O	Physical transmit or receive signal (- differential)
12	TX+	I/O	Physical transmit or receive signal (+ differential)
13	GND	Gnd	Ground
14	XO	O	Crystal feedback This pin is used only when a 25 MHz crystal is used. This pin is a no connect if oscillator or external clock source is used.
15	XI	I	Crystal / Oscillator / External Clock Input 25MHz +/-50ppm
16	REXT	I/O	Set physical transmit output current Connect a 6.49KΩ resistor in parallel with a 100pF capacitor to ground on this pin. See KSZ8041MLL reference schematic.
17	GND	Gnd	Ground
18	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7KΩpull-up resistor.
19	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
20	RXD3 / PHYAD0	Ipu/O	MII Mode: Receive Data Output[3][2] / Config. Mode: The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See “Strapping Options” section for details.
21	RXD2 / PHYAD1	Ipd/O	MII Mode: Receive Data Output[2][2] / Config. Mode: The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See “Strapping Options” section for details.
22	RXD1 / PHYAD2	Ipd/O	MII Mode: Receive Data Output[1][2] / Config. Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See “Strapping Options” section for details.
23	RXD0 / DUPLEX	Ipu/O	MII Mode: Receive Data Output[0][2] / Config Mode: Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See “Strapping Options” section for details.
24	GND	Gnd	Ground
25	VDDIO_3.3	P	3.3V digital V_{DD}
26	VDDIO_3.3	P	3.3V digital V_{DD}

Pin Number	Pin Name	Type(1)	Pin Function
27	RXDV / CONFIG2	Ipd/O	MII Mode: Receive Data Valid Output / Config. Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See “Strapping Options” section for details.
28	RXC	O	MII Receive Clock Output
29	RXER / ISO	Ipd/O	MII Mode: Receive Error Output / Config. Mode: The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See “Strapping Options” section for details.
30	GND	Gnd	Ground
31	VDD_1.8	P	1.8V digital V_{DD}
32	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
33	TXC	I/O	MII Transmit Clock Output
34	TXEN	I	MII Transmit Enable Input
35	TXD0	I	MII Transmit Data Input[0](3)
36	TXD1	I	MII Transmit Data Input[1](3)
37	GND	Gnd	Ground
38	TXD2	I	MII Transmit Data Input[2](3) /
39	TXD3	I	MII Transmit Data Input[3](3) /
40	COL / CONFIG0	Ipd/O	MII Mode: Collision Detect Output / Config. Mode: The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See “Strapping Options” section for details.
41	CRS / CONFIG1	Ipd/O	MII Mode: Carrier Sense Output / Config. Mode: The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See “Strapping Options” section for details.
42	LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config. Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See “Strapping Options” section for details. The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Link/Activity** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON Activity / Toggle / Blinking **LED mode = [01]** **Link** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON **LED mode = [10]** Reserved **LED mode = [11]** Reserved

Pin Number	Pin Name	Type(1)	Pin Function
43	LED1 / SPEED	Ipu/O	LED Output: Programmable LED1 Output / Config. Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See "Strapping Options" section for details. The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Speed** / **Pin State** / **LED Definition** 10BT / H / OFF 100BT / L / ON **LED mode = [01]** **Activity** / **Pin State** / **LED Definition** No Activity / H / OFF Activity / Toggle / Blinking **LED mode = [10]** Reserved **LED mode = [11]** Reserved
44	NC	-	No connect
45	NC	-	No connect
46	NC	-	No connect
47	RST#	I	Chip Reset (active low)
48	NC	-	No connect

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipd = Input with internal pull-down (40K +/-30%).
   Ipu = Input with internal pull-up (40K +/-30%).
   Opu = Output with internal pull-up (40K +/-30%).
   Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.
2. MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.
3. MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.

Strapping Options – KSZ8041MLL

Pin Number	Pin Name	Type[1]	Pin Function
22 21 20	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are always set to '00'.
27 41 40	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows: **CONFIG[2:0] Mode** 000 MII (default) 001 Reserved – not used 010 Reserved – not used 011 Reserved – not used 100 MII 100Mbps Preamble Restore 101 Reserved – not used 110 MII back-to-back 111 Reserved – not used
29	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable During power-up / reset, this pin value is latched into register 0h bit 10.
43	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
23	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
42	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.

Note:

1. Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

Functional Description

The KSZ8041TL is a single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3u specification.

On the media side, the KSZ8041TL supports 10Base-T and 100Base-TX with HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

The KSZ8041TL offers a choice of MII, RMII, or SMII data interface connection to a MAC processor. The MII management bus option gives the MAC processor complete access to the KSZ8041TL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

The KSZ8041FTL has all the identical rich features of the KSZ8041TL plus 100Base-FX fiber support.

The KSZ8041MLL is the basic 10Base-T/100Base-TX copper version with MII support.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.

The output current is set by an external 6.49 KΩ 1% resistor for the 1:1 transformer ratio. It has typical rise/fall times of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10Base-T output drivers are also incorporated into the 100Base-TX drivers.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based upon comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8041TL/FTL/MLL generates 125MHz, 25MHz and 20MHz clocks for system timing. In MII mode, internal clocks are generated from an external 25MHz crystal or oscillator. For the KSZ8041TL/FTL, in RMII and SMII modes, these internal clocks are generated from external 50MHz and 125MHz oscillators or system clocks, respectively.

Scrambler/De-scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers also perform internal wave-shaping and pre-emphasize, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RX+ and RX- inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8041TL/FTL/MLL decodes a data frame. The receive clock is kept active during idle periods in between data reception.

SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

Auto-Negotiation

The KSZ8041TL/FTL/MLL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation is enabled by either hardware pin strapping (pin 42) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8041TL/FTL/MLL link partner is forced to bypass auto-negotiation, the KSZ8041TL/FTL/MLL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8041TL/FTL/MLL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the following flow chart.

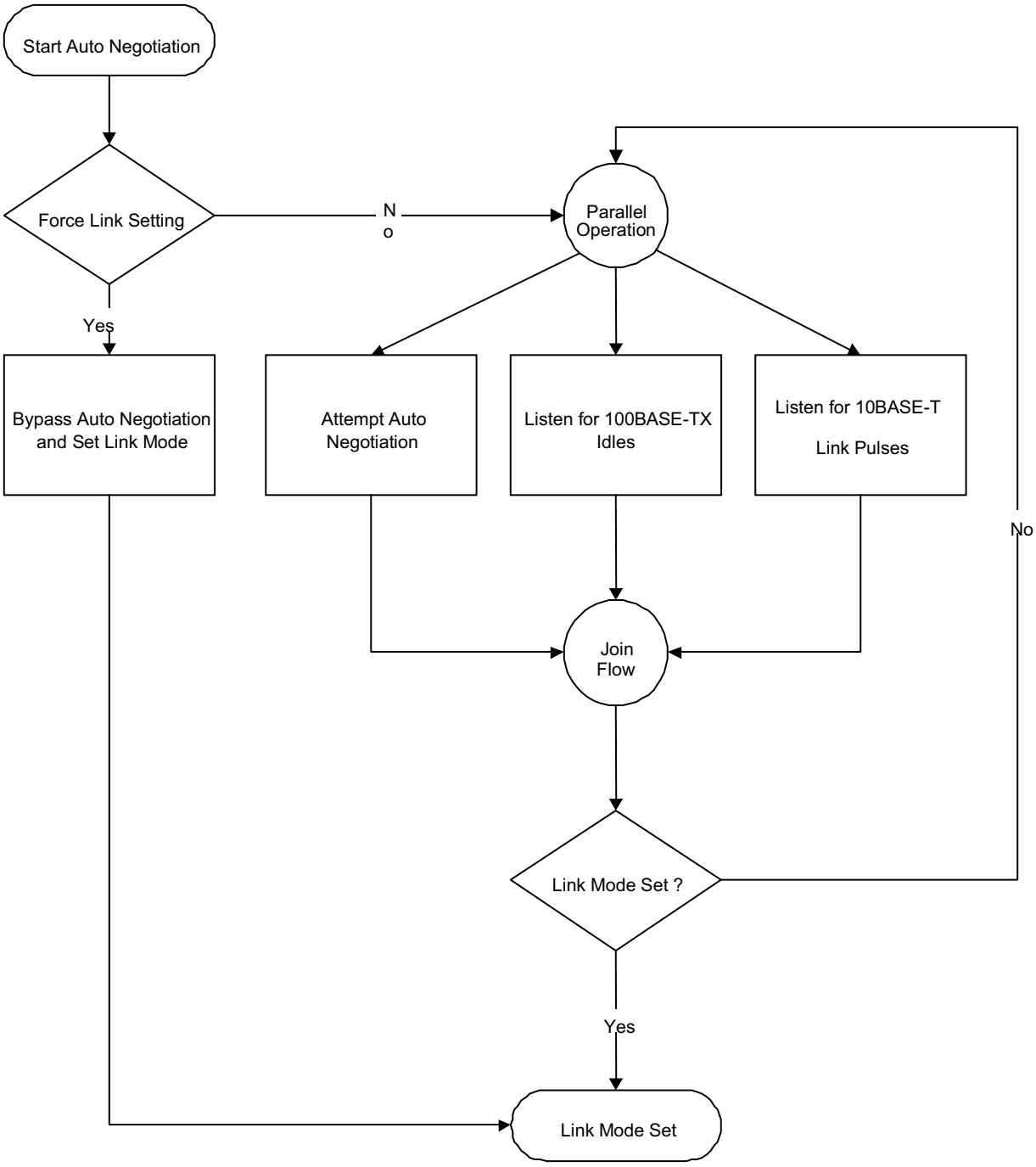


Figure 1. Auto-Negotiation Flow Chart

MII Management (MIIM) Interface

The KSZ8041TL/FTL/MLL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ8041TL/FTL/MLL. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows a external controller to communicate with one or more PHY devices. Each KSZ8041TL/FTL/MLL device is assigned a unique PHY address between 1 and 7 by its PHYAD[2:0] strapping pins. Also, every KSZ8041TL/FTL/MLL device supports the broadcast PHY address 0, as defined per the IEEE 802.3 Specification, which can be used to read/write to a single KSZ8041TL/FTL/MLL device, or write to multiple KSZ8041TL/FTL/MLL devices simultaneously.
- A set of 16-bit MDIO registers. Register [0:6] are required, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality.

The following table shows the MII Management frame format for the KSZ8041TL/FTL/MLL.

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 1. MII Management Frame Format

Interrupt (INTRP)

INTRP (pin 32) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8041TL/FTL/MLL PHY register. Bits[15:8] of register 1Bh are the interrupt control bits, and are used to enable and disable the conditions for asserting the INTRP signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit 9 of register 1Fh sets the interrupt level to active high or active low.

MII Data Interface

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 Specification. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 25MHz reference clock, sourced by the PHY.
- Provides independent 4-bit wide (nibble) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

By default, the KSZ8041TL/FTL/MLL is configured to MII mode after it is power-up or reset with the following:

- A 25MHz crystal connected to XI, XO (pins 15, 14), or an external 25MHz clock source (oscillator) connected to XI.
- CONFIGURATION[2:0] (pins 27, 41, 40) set to '000' (default setting).