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KSZ8041NL/RNL

10Base-T/100Base-TX Physical Layer Transceiver

Revision 1.5

General Description

The KSZ8041NL is a single supply 10Base-T/100Base-TX physical layer transceiver, which provides MII/RMII interfaces to transmit and receive data. A unique mixed signal design extends signaling distance while reducing power consumption.

HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables.

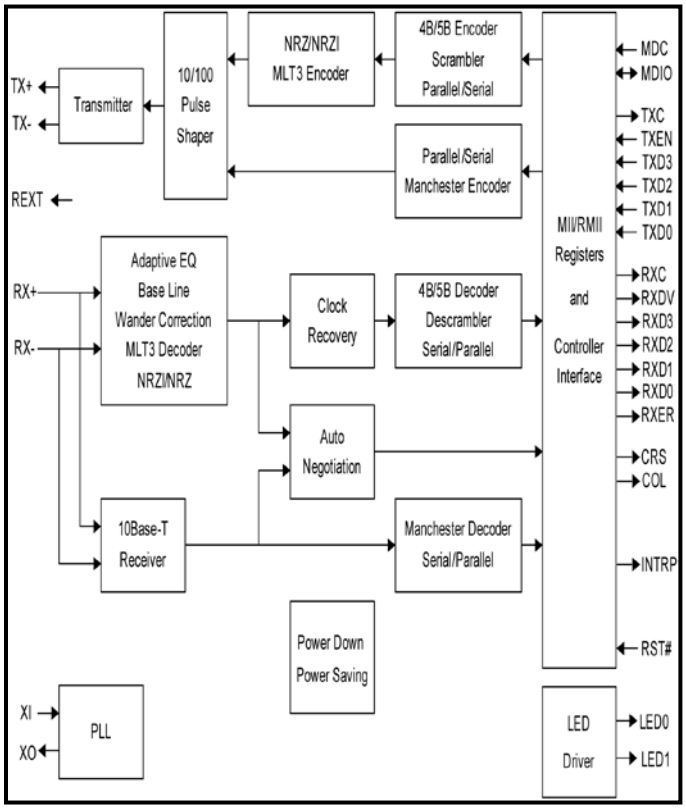
The KSZ8041NL represents a new level of features and performance and is an ideal choice of physical layer transceiver for 10Base-T/100Base-TX applications.

The KSZ8041RNL is an enhanced RMII version of the KSZ8041NL that does not require a 50MHz system clock. It uses a 25MHz crystal for its input reference clock and outputs a 50MHz RMII reference clock to the MAC.

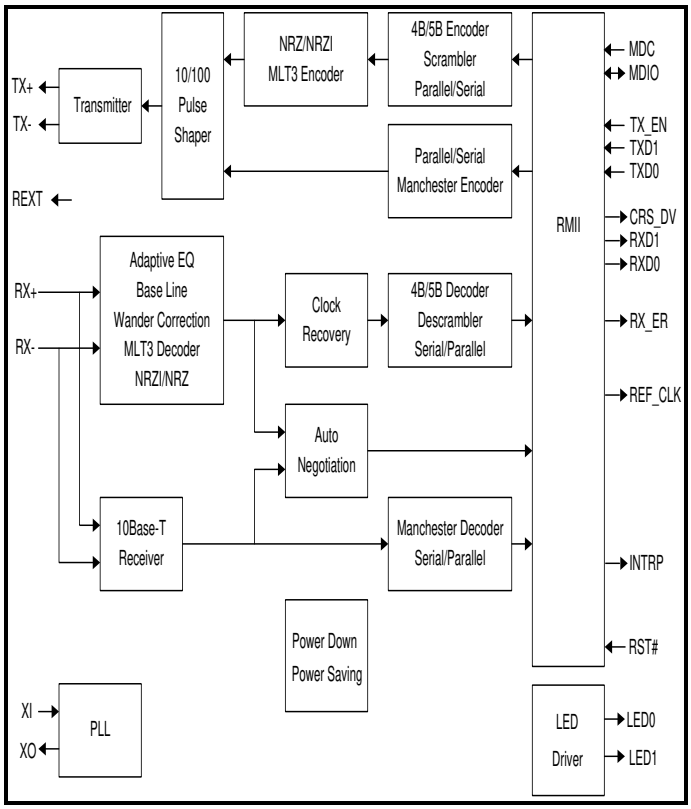
The KSZ8041NL and KSZ8041RNL are available in 32-pin, lead-free QFN packages (see *Ordering Information*).

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Functional Diagram



KSZ8041NL



KSZ8041RNL

Features

- Single-chip 10Base-T/100Base-TX physical layer solution
- Fully compliant to IEEE 802.3u standard
- Low power CMOS design, power consumption of <180mW
- HP auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Robust operation over standard cables
- Power down and power saving modes
- MII interface support (KSZ8041NL only)
- RMII interface support with external 50MHz system clock (KSZ8041NL only)
- RMII interface support with 25MHz crystal/clock input and 50MHz reference clock output to MAC (KSZ8041RNL only)
- MIIM (MDC/MDIO) management bus to 6.25MHz for rapid PHY register configuration
- Interrupt pin option
- Programmable LED outputs for link, activity and speed
- ESD rating (6kV)
- Single power supply (3.3V)
- Built-in 1.8V regulator for core
- Available in 32-pin 5mm × 5mm QFN package

Applications

- Printer
- LOM
- Game console
- IPTV
- IP phone
- IP set-top box

Ordering Information

For the device marking (second column in the Ordering Information table), the fifth character of line 3 indicates whether the device has gold wire bonding or silver wire bonding, as follows:

- Gold wire bonding: The letter “S” is not present as the fifth character of line 3.
- Silver wire bonding: The letter “S” is present as the fifth character of line 3.

For line three, the presence or non-presence of the letter “S” is preceded by YYWW, indicating the last two digits of the year and the two digits work week for the chip date code, and is followed by xxx, indicating the chip revision and assembly site.

Part Number	Device Marking	Package	Temperature Range	Wire Bonding	Description
KSZ8041NL	KSZ8041NL YYWWxxx	32-Pin QFN	0°C to 70°C	Gold	MII, Commercial Temperature, Gold Wire Bonding, 32-Pin QFN, Pb-Free
SPNZ801162(1)	KSZ8041NL YYWW**S**xxx	32-Pin QFN	0°C to 70°C	Silver	MII, Commercial Temperature, Silver Wire Bonding, 32-Pin QFN, Pb-Free
KSZ8041NLI	KSZ8041NLI YYWWxxx	32-Pin QFN	–40°C to 85°C	Gold	MII, Industrial Temperature, Gold Wire Bonding, 32-Pin QFN, Pb-Free
SPNY801162(1)	KSZ8041NLI YYWW**S**xxx	32-Pin QFN	–40°C to 85°C	Silver	MII, Industrial Temperature, Silver Wire Bonding, 32-Pin QFN, Pb-Free
KSZ8041NL AM(1)	KSZ8041NL AM YYWWxxx	32-Pin QFN	–40°C to 85°C	Gold	MII, Industrial Temperature, Gold Wire Bonding, 32-Pin QFN, Pb-Free, Automotive Qualified Device.
KSZ8041RNLU(1)	KSZ8041 RNLU YYWWxxx	32-Pin QFN	–40°C to 85°C	Gold	RMII with 50MHz clock output, Industrial Temperature, Gold Wire Bonding, 32-Pin QFN, Pb-Free, Automotive Qualified Device.
KSZ8041RNL	KSZ8041RNL YYWWxxx	32-Pin QFN	0°C to 70°C	Gold	RMII with 50MHz clock output, Commercial Temperature, Gold Wire Bonding, 32-Pin QFN, Pb-Free
SPNZ801164(1)	KSZ8041RNL YYWW**S**xxx	32-Pin QFN	0°C to 70°C	Silver	RMII with 50MHz clock output, Commercial Temperature, Silver Wire Bonding, 32-Pin QFN, Pb-Free
KSZ8041RNLI	KSZ8041RNLI YYWWxxx	32-Pin QFN	–40°C to 85°C	Gold	RMII with 50MHz clock output, Industrial Temperature, Gold Wire Bonding, 32-Pin QFN, Pb-Free
SPNY801164(1)	KSZ8041RNLI YYWW**S**xxx	32-Pin QFN	–40°C to 85°C	Silver	RMII with 50MHz clock output, Industrial Temperature, Silver Wire Bonding, 32-Pin QFN, Pb-Free

Note:

1. Contact factory for availability.

Revision History

Revision	Date	Summary of Changes
1.0	10/13/06	Data sheet created.
1.1	4/27/07	Added maximum MDC clock speed. Added 40K ±30% to Note 1 of Pin Description and Strapping Options tables for internal pull-ups/pull-downs. Changed Model Number in Register 3h – PHY Identifier 2. Changed polarity (swapped definition) of DUPLEX strapping pin. Removed DUPLEX strapping pin update to Register 4h – Auto-Negotiation Advertisement bits [8, 6]. Set “Disable power saving” as the default for Register 1Fh bit [10]. Corrected LED1 (pin 31) definition for Activity in LED mode 01. Added Symbol Error to MII/RMII Receive Error description and Register 15h – RXER Counter. Added a 100pF capacitor on REXT (pin 10) in Pin Description table.
1.2	7/18/08	Added Automotive Qualified part number to Ordering Information. Added maximum case temperature. Added thermal resistance (θ_{JC}). Added chip maximum current consumption.
1.3	12/11/09	Added Automotive Qualified part number, KSZ8041NL EAM, to Ordering Information. Changed MDIO hold time (min) from 10ns to 4ns. Added LED drive current. Renamed Register 3h bits [3:0] to “manufacturer’s revision number” and changed default value to “Indicates silicon revision.” Updated RMII output delay for CRSDV and RXD[1:0] output pins. Added support for Asymmetric PAUSE in register 4h bit [11]. Added control bits for 100Base-TX preamble restore (register 14h bit [7]) and 10Base-T preamble restore (register 14h bit [6]). Changed strapping pin definition for CONFIG[2:0] = 100 from “PCS Loopback” to “MII 100Mbps Preamble Restore.” Corrected MII timing for t_{RLAT}, t_{CRS1}, t_{CRS2}. Added KSZ8041RNL device and updated entire data sheet accordingly.
1.4	1/19/10	Removed part number (KSZ8041NL EAM) from Ordering Information. Removed chip maximum current consumption.
1.5	2/2/15	Added automotive qualified part number, KSZ8041RNLU. Changed VDDPLL_1.8 (Pin 2) decoupling capacitor value from 10µF to 1.0µF. Specified minimum 250µs rise time for 3.3V input supply voltages ($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$). Add the part numbers of the silver wire bonding in *Ordering Information*.

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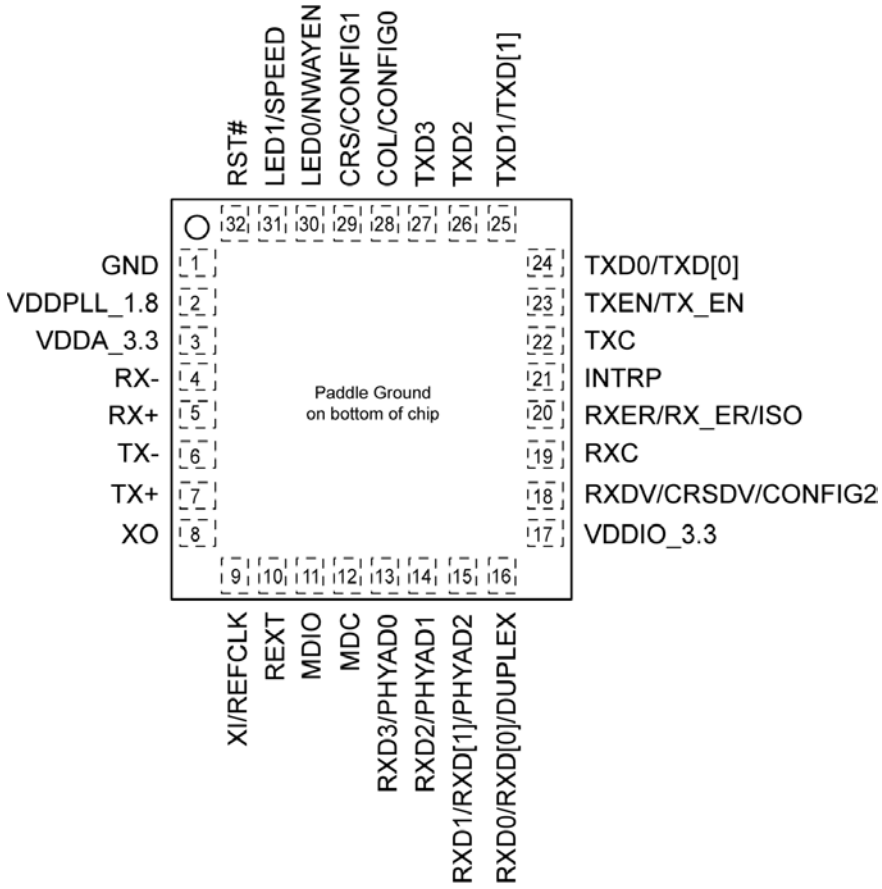
Pin Configuration – KSZ8041NL



32-Pin 5mm × 5mm QFN

Pin Description – KSZ8041NL

Pin Number	Pin Name	Type[2]	Pin Function
1	GND	Gnd	Ground.
2	VDDPLL_1.8	P	1.8V Analog V_{DD} Decouple with 1.0µF and 0.1µF capacitors to ground.
3	VDDA_3.3	P	3.3V Analog V_{DD}.
4	RX-	I/O	Physical receive or transmit signal (- differential).
5	RX+	I/O	Physical receive or transmit signal (+ differential).
6	TX-	I/O	Physical transmit or receive signal (- differential).
7	TX+	I/O	Physical transmit or receive signal (+ differential).
8	XO	O	Crystal Feedback. This pin is used only in MII mode when a 25MHz crystal is used. This pin is a no connect if oscillator or external clock source is used, or if RMII mode is selected.
9	XI / REFCLK	I	Crystal / Oscillator / External Clock Input: MII Mode: 25MHz ±50ppm (crystal, oscillator, or external clock) RMII Mode: 50MHz ±50ppm (oscillator, or external clock only)
10	REXT	I/O	Set physical transmit output current. Connect a 6.49KΩ resistor in parallel with a 100pF capacitor to ground on this pin. See KSZ8041NL reference schematics.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
13	RXD3 / PHYAD0	Ipu/O	MII Mode: Receive Data Output[3][3] /. Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See *Strapping Options – KSZ8041NL* for details.
14	RXD2 / PHYAD1	Ipd/O	MII Mode: Receive Data Output[2][3] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See *Strapping Options – KSZ8041NL* for details.

Notes:

2. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipd = Input with internal pull-down (40K +/-30%).
   Ipu = Input with internal pull-up (40K +/-30%).
   Opu = Output with internal pull-up (40K +/-30%).
   Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.
3. MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.
4. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.
5. MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.
6. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

Pin Description – KSZ8041NL (Continued)

Pin Number	Pin Name	Type[2]	Pin Function
15	RXD1 / RXD[1] / PHYAD2	Ipd/O	MII Mode: Receive Data Output[1][3]/. RMII Mode: Receive Data Output[1][4] /. Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See *Strapping Options – KSZ8041NL* for details.
16	RXD0 / RXD[0] / DUPLEX	Ipu/O	MII Mode: Receive Data Output[0][3]/. RMII Mode: Receive Data Output[0][4] /. Config Mode: Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See *Strapping Options – KSZ8041NL* for details.
17	VDDIO_3.3	P	3.3V Digital V_{DD}.
18	RXDV / CRSDV / CONFIG2	Ipd/O	MII Mode: Receive Data Valid Output /. RMII Mode: Carrier Sense/Receive Data Valid Output /. Config Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See *Strapping Options – KSZ8041NL* for details.
19	RXC	O	MII Mode: Receive Clock Output.
20	RXER / RX_ER / ISO	Ipd/O	MII Mode: Receive Error Output. RMII Mode: Receive Error Output. Config Mode: The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See *Strapping Options – KSZ8041NL* for details.
21	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
22	TXC	O	MII Mode: Transmit Clock Output.
23	TXEN / TX_EN	I	MII Mode: Transmit Enable Input /. RMII Mode: Transmit Enable Input.
24	TXD0 / TXD[0]	I	MII Mode: Transmit Data Input[0][5] /. RMII Mode: Transmit Data Input[0][6].
25	TXD1 / TXD[1]	I	MII Mode: Transmit Data Input[1][5] /. RMII Mode: Transmit Data Input[1][6].
26	TXD2	I	MII Mode: Transmit Data Input[2][5] /.
27	TXD3	I	MII Mode: Transmit Data Input[3][5] /.
28	COL / CONFIG0	Ipd/O	MII Mode: Collision Detect Output /. Config Mode: The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See *Strapping Options – KSZ8041NL* for details.
29	CRS / CONFIG1	Ipd/O	MII Mode: Carrier Sense Output /. Config Mode: The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See *Strapping Options – KSZ8041NL* for details.

Pin Description – KSZ8041NL (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(2)</th><th>Pin Function</th></tr>
<tr><td>30</td><td>LED0 / NWAYEN</td><td>Ipu/O</td><td>
LED Output: Programmable LED0 Output /.
Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See Strapping Options – KSZ8041NL for details.
The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

LED Mode = [00]
<table>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
LED Mode = [01]
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>
<u>LED Mode = [10]</u>
Reserved

<u>LED Mode = [11]</u>
Reserved
</td></tr>
</table>

Pin Description – KSZ8041NL (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(2)</th><th>Pin Function</th></tr>
<tr><td>31</td><td>LED1 / SPEED</td><td>Ipu/O</td><td>
LED Output: Programmable LED1 Output /
Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See Strapping Options – KSZ8041NL for details.
The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00]</th></tr>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10BT</td><td>H</td><td>OFF</td></tr>
<tr><td>100BT</td><td>L</td><td>ON</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01]</th></tr>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<u>LED Mode = [10]</u>
Reserved.

<u>LED Mode = [11]</u>
Reserved.
</td></tr>
<tr><td>32</td><td>RST#</td><td>I</td><td>Chip Reset (active low).</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>Gnd</td><td>Ground.</td></tr>
</table>

Strapping Options – KSZ8041NL

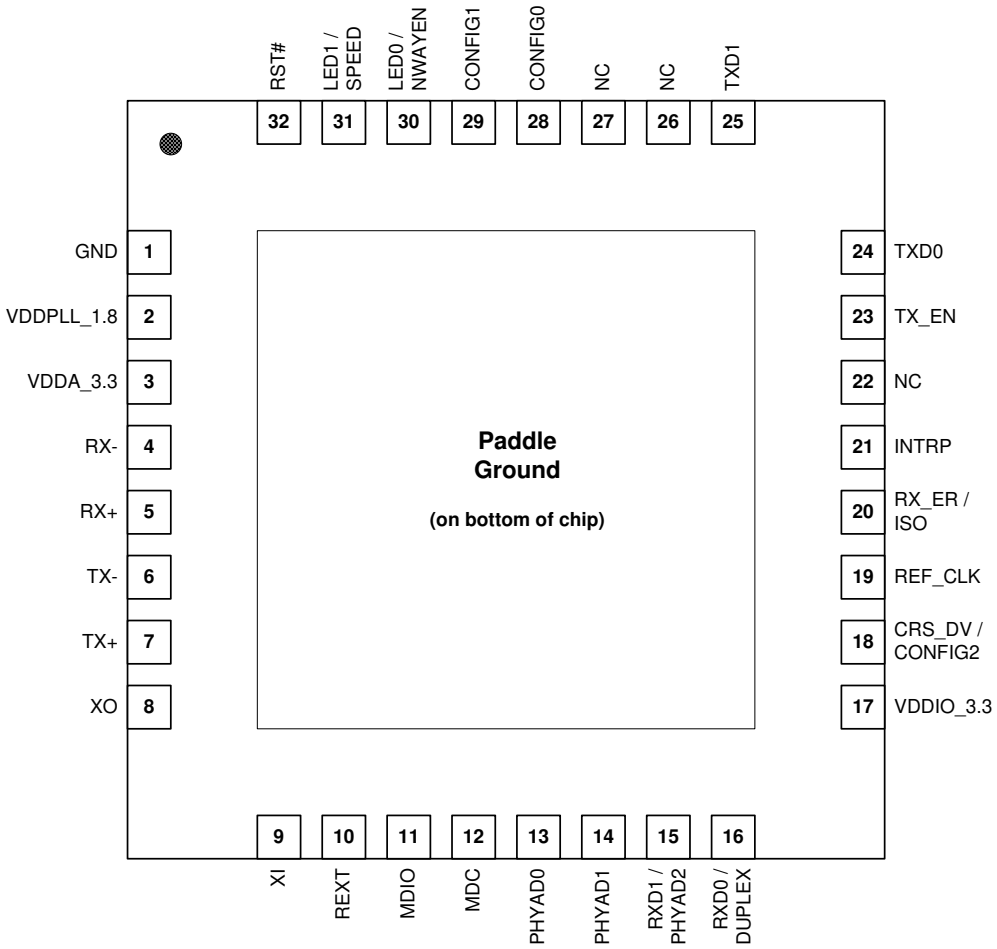
Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(7)</th><th>Pin Function</th></tr>
<tr><td>15
14
13</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>18
29
28</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>010</td><td>Reserved – not used</td></tr><tr><td>011</td><td>Reserved – not used</td></tr><tr><td>100</td><td>MII 100Mbps Preamble Restore</td></tr><tr><td>101</td><td>Reserved – not used</td></tr><tr><td>110</td><td>Reserved – not used</td></tr><tr><td>111</td><td>Reserved – not used</td></tr></table></td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>ISOLATE Mode:
Pull-up = Enable
Pull-down (default) = Disable
During power-up / reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>SPEED Mode:
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>DUPLEX Mode:
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway Auto-Negotiation Enable
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
During power-up / reset, this pin value is latched into register 0h bit 12.</td></tr>
</table>

Note:

7. Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.

Pin Configuration – KSZ8041RNL



32-Pin 5mm × 5mm QFN

Pin Description – KSZ8041RNL

Pin Number	Pin Name	Type[8]	Pin Function
1	GND	Gnd	Ground.
2	VDDPLL_1.8	P	1.8V Analog V_{DD}. Decouple with 1.0µF and 0.1µF capacitors to ground.
3	VDDA_3.3	P	3.3V Analog V_{DD}.
4	RX-	I/O	Physical receive or transmit signal (- differential).
5	RX+	I/O	Physical receive or transmit signal (+ differential).
6	TX-	I/O	Physical transmit or receive signal (- differential).
7	TX+	I/O	Physical transmit or receive signal (+ differential).
8	XO	O	Crystal Feedback – for 25MHz Crystal. This pin is a no connect if oscillator or external clock source is used.
9	XI	I	Crystal / Oscillator / External Clock Input. 25MHz ±50ppm.
10	REXT	I/O	Set physical transmit output current. Connect a 6.49KΩ resistor in parallel with a 100pF capacitor to ground on this pin. See KSZ8041RNL reference schematics.
11	MDIO	I/O	Management Interface (MII) Data I/O. This pin requires an external 4.7KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input. This pin is synchronous to the MDIO data interface.
13	PHYAD0	Ipu/O	The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.
14	PHYAD1	Ipd/O	The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.
15	RXD1 / PHYAD2	Ipd/O	RMII Mode: RMII Receive Data Output[1][9] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.
16	RXD0 / DUPLEX	Ipu/O	RMII Mode: RMII Receive Data Output[0][9] / Config Mode: Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.

Notes:

8. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Opu = Output with internal pull-up (40K ±30%).
   Ipu/O = Input with internal pull-up (40K ±30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K ±30%) during power-up/reset; output pin otherwise.
9. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.

Pin Description – KSZ8041RNL (Continued)

Pin Number	Pin Name	Type[8]	Pin Function
17	VDDIO_3.3	P	3.3V Digital V_{DD}
18	CRS_DV / CONFIG2	Ipd/O	RMII Mode: Carrier Sense/Receive Data Valid Output /. Config Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.
19	REF_CLK	O	50MHz Clock Output. This pin provides the 50MHz RMII reference clock output to the MAC.
20	RX_ER / ISO	Ipd/O	RMII Mode: RMII Receive Error Output / Config Mode: The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.
21	INTRP	Opu	Interrupt Output: Programmable Interrupt Output. Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
22	NC	O	No Connect.
23	TX_EN	I	RMII Transmit Enable Input.
24	TXD0	I	RMII Transmit Data Input[0][10].
25	TXD1	I	RMII Transmit Data Input[1][10].
26	NC	I	No Connect.
27	NC	I	No Connect.
28	CONFIG0	Ipd/O	The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.
29	CONFIG1	Ipd/O	The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See *Strapping Options – KSZ8041RNL* for details.

Note:

10. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

Pin Description – KSZ8041RNL (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[8]</th><th>Pin Function</th></tr>
<tr><td>30</td><td>LED0 /
NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output /.
Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See Strapping Options – KSZ8041RNL for details.
The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01]</th></tr>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>

<u>LED Mode = [10] , [11]</u>
Reserved.</td></tr>
<tr><td>31</td><td>LED1 /
SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output /.
Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See Strapping Options – KSZ8041RNL for details.
The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00]</th></tr>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10BT</td><td>H</td><td>OFF</td></tr>
<tr><td>100BT</td><td>L</td><td>ON</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01]</th></tr>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<u>LED Mode = [10], [11]</u>
Reserved.</td></tr>
<tr><td>32</td><td>RST#</td><td>I</td><td>Chip Reset (active low).</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>Gnd</td><td>Ground.</td></tr>
</table>

Strapping Options – KSZ8041RNL

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>15
14
13</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>18
29
28</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>Reserved – not used</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>010</td><td>Reserved – not used</td></tr><tr><td>011</td><td>Reserved – not used</td></tr><tr><td>100</td><td>Reserved – not used</td></tr><tr><td>101</td><td>Reserved – not used</td></tr><tr><td>110</td><td>Reserved – not used</td></tr><tr><td>111</td><td>Reserved – not used</td></tr></table></td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>ISOLATE Mode:
Pull-up = Enable
Pull-down (default) = Disable
During power-up / reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>SPEED Mode:
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>DUPLEX Mode:
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway Auto-Negotiation Enable:
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
During power-up / reset, this pin value is latched into register 0h bit 12.</td></tr>
</table>

Note:

11. Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.

Functional Description

The KSZ8041NL is a single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3u Specification.

On the media side, the KSZ8041NL supports 10Base-T and 100Base-TX with HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

The KSZ8041NL offers a choice of MII or RMII data interface connection with the MAC processor. The MII management bus option gives the MAC processor complete access to the KSZ8041NL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

The KSZ8041RNL is an enhanced RMII version of the KSZ8041NL that does not require a 50MHz system clock. It uses a 25MHz crystal for its input reference clock and outputs a 50MHz RMII reference clock to the MAC.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.

The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio. It has typical rise/fall times of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10Base-T output drivers are also incorporated into the 100Base-TX drivers.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8041NL/RNL generates 125MHz, 25MHz and 20MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator. For the KSZ8041NL in RMII mode, these internal clocks are generated from an external 50MHz oscillator or system clock.

Scrambler/De-Scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers also perform internal wave-shaping and pre-emphasize, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RX+ and RX- inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8041NL/RNL decodes a data frame. The receive clock is kept active during idle periods in between data reception.

SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

Auto-Negotiation

The KSZ8041NL/RNL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation is enabled by either hardware pin strapping (pin 30) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8041NL/RNL link partner is forced to bypass auto-negotiation, the KSZ8041NL/RNL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8041NL/RNL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the flow chart illustrated as Figure 1.

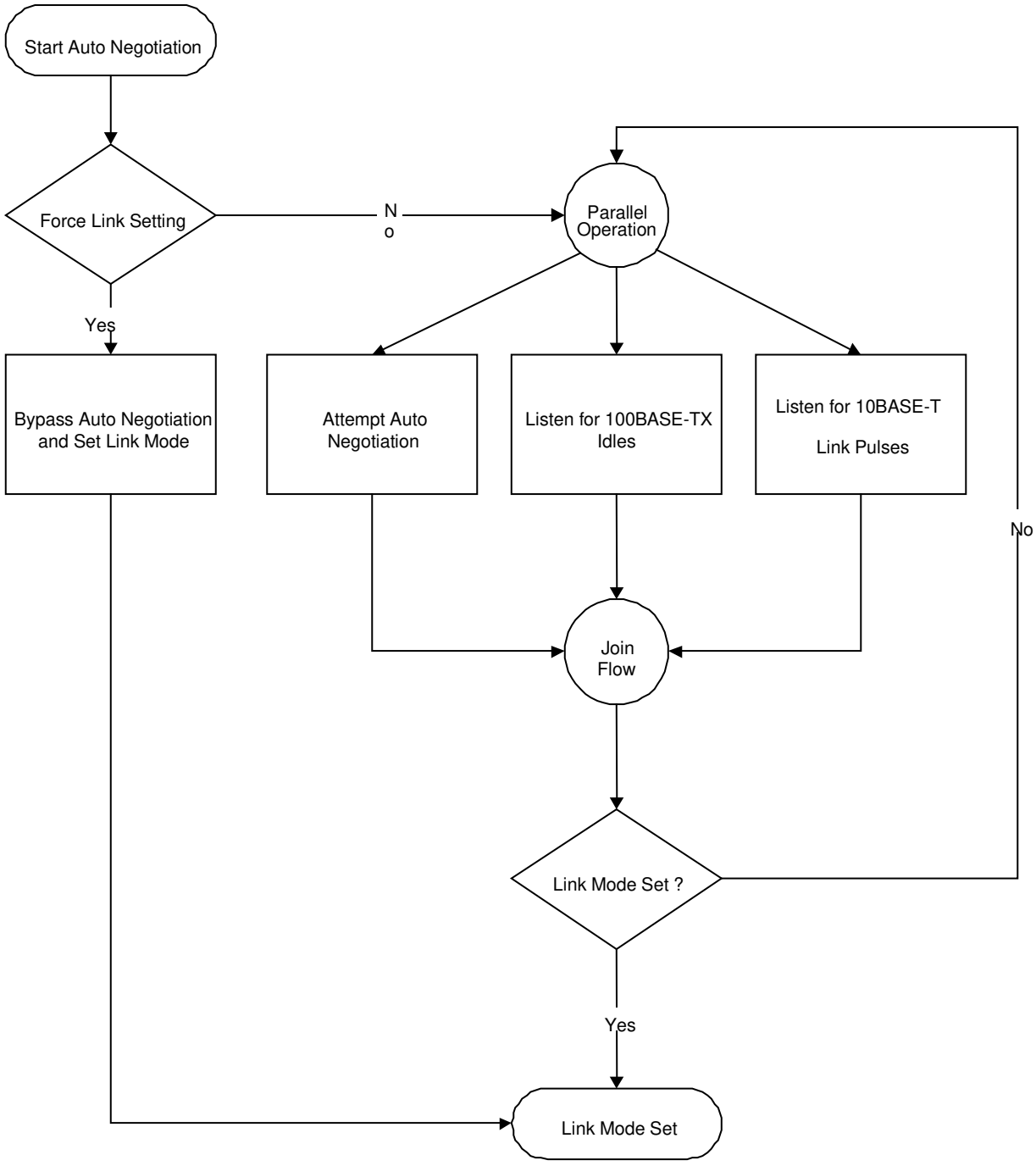


Figure 1. Auto-Negotiation Flow Chart

MII Management (MIIM) Interface

The KSZ8041NL/RNL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ8041NL/RNL. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows a external controller to communicate with one or more PHY devices. Each KSZ8041NL/RNL device is assigned a unique PHY address between 1 and 7 by its PHYAD[2:0] strapping pins. Also, every KSZ8041NL/RNL device supports the broadcast PHY address 0, as defined per the IEEE 802.3 Specification, which can be used to read/write to a single KSZ8041NL/RNL device, or write to multiple KSZ8041NL/RNL devices simultaneously.
- A set of 16-bit MDIO registers. Register [0:6] are required, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality.

Table 1 shows the MII Management frame format for the KSZ8041NL/RNL.

Table 1. MII Management Frame Format

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Interrupt (INTRP)

INTRP (pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8041NL/RNL PHY register. Bits[15:8] of register 1Bh are the interrupt control bits, and are used to enable and disable the conditions for asserting the INTRP signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit 9 of register 1Fh sets the interrupt level to active high or active low.

MII Data Interface (KSZ8041NL only)

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 Specification. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 25MHz reference clock, sourced by the PHY.
- Provides independent 4-bit wide (nibble) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

By default, the KSZ8041NL is configured to MII mode after it is power-up or reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- CONFIG[2:0] (pins 18, 29, 28) set to '000' (default setting).

MII Signal Definition (KSZ8041NL only)

Table 2 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

Table 2. MII Signal Definition

MII Signal Name	Direction (with respect to PHY, KSZ8041NL signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

Transmit Data [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is ”00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY’s reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY’s reference clock.

RXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), “5D”, and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

Receive Data [3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter, or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter, or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

Reduced MII (RMII) Data Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 50MHz reference clock.
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The KSZ8041NL is configured in RMII mode after it is power-up or reset with the following:

- A 50MHz reference clock connected to REFCLK (pin 9).
- CONFIG[2:0] (pins 18, 29, 28) set to ‘001’.

The KSZ8041RNL is configured in RMII mode and outputs the 50MHz RMII reference clock to the MAC on REF_CLK (pin 19) after it is power-up or reset with the following:

- A 25MHz crystal connected to XI (pin 9) and XO (pin 8), or a 25MHz reference clock connected to XI (pin 9).
- CONFIG[2:0] (pins 18, 29, 28) set to ‘001’.

In RMII mode, unused MII signals, TXD[3:2] (pins 27, 26), are tied to ground.