Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

KSZ8051MNL/RNL

10Base-T/100Base-TX Physical Layer Transceiver

General Description

The KSZ8051 is a single supply 10Base-T/100Base-TX Ethernet physical layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8051 is a highly integrated, compact solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low noise regulator to supply the 1.2V core.

The KSZ8051MNL offers the Media Independent Interface (MII) and the KSZ8051RNL offers the Reduced Media Independent Interface (RMII) for direct connection with MII/ RMII compliant Ethernet MAC processors and switches.

A 25MHz crystal is used to generate all required clocks, including the 50MHz RMII reference clock output for the KSZ8051RNL.

The KSZ8051 provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ8051 I/Os and board. Micrel LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling.

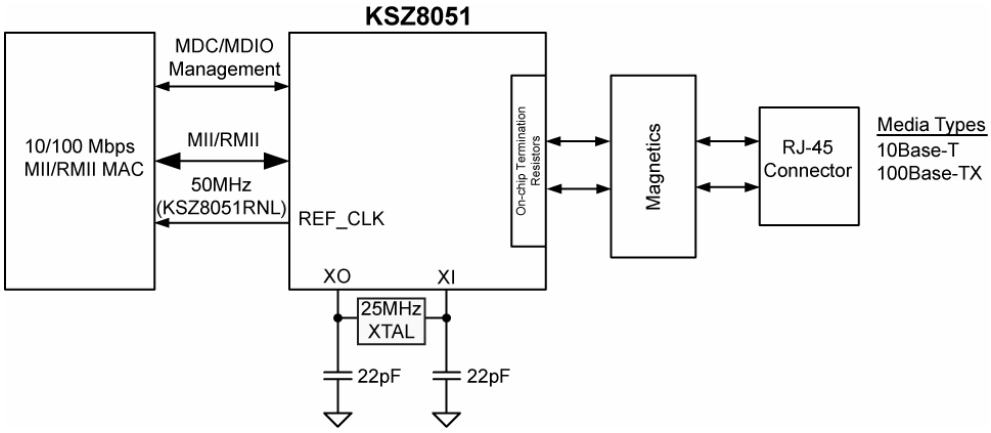
The KSZ8051MNL and KSZ8051RNL are available in 32-pin, lead-free QFN packages (See Ordering Information).

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Single-chip 10Base-T/100Base-TX IEEE 802.3 compliant Ethernet Transceiver
- MII Interface support (KSZ8051MNL)
- RMII v1.2 Interface support with 50MHz reference clock output to MAC, and option to input 50MHz reference clock (KSZ8051RNL)
- Back-to-Back mode support for 100Mbps copper repeater or media converter
- MDC/MDIO Management Interface for PHY register configuration
- Programmable interrupt output
- LED outputs for link, activity and speed status indication
- On-chip termination resistors for the differential pairs
- Baseline Wander Correction
- HP Auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Auto-negotiation to automatically select the highest link up speed (10/100 Mbps) and duplex (half/full)
- Power down and power saving modes
- LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and board.

Functional Diagram



LinkMD is a registered trademark of Micrel, Inc.

More Features

- Loopback modes for diagnostics
- Single 3.3V power supply with VDD I/O options for 1.8V, 2.5V, or 3.3V
- Built-in 1.2V regulator for core
- Available in 32-pin (5mm x 5mm) QFN package

Applications

- Game Console
- IP Phone
- IP Set-top Box
- IP TV
- LOM
- Printer

Ordering Information

Part Number	Temp. Range	Package	Lead Finish	Description
KSZ8051MNL	0°C to 70°C	32-Pin QFN	Pb-Free	MII, Commercial Temperature
KSZ8051MNLI (1)	-40°C to 85°C	32-Pin QFN	Pb-Free	MII, Industrial Temperature
KSZ8051RNL	0°C to 70°C	32-Pin QFN	Pb-Free	RMII, Commercial Temperature
KSZ8051RNLI (1)	-40°C to 85°C	32-Pin QFN	Pb-Free	RMII, Industrial Temperature

Note:

1. Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
1.0	6/22/10	Data sheet created.

Contents

General Description 1
Features 1
Functional Diagram 1
Applications 2
Ordering Information 2
Revision History 3
Contents 4
List of Figures 7
List of Tables 8
Pin Configuration – KSZ8051MNL 9
Pin Description – KSZ8051MNL 10
Strapping Options – KSZ8051MNL 13
Pin Configuration – KSZ8051RNL 14
Pin Description – KSZ8051RNL 15
Strapping Options – KSZ8051RNL 18
Functional Description: 10Base-T/100Base-TX Transceiver 19
100Base-TX Transmit 19
100Base-TX Receive 19
10Base-T Transmit 19
10Base-T Receive 19
Scrambler/De-scrambler (100Base-TX only) 20
SQE and Jabber Function (10Base-T only) 20
PLL Clock Synthesizer 20
Auto-Negotiation 20
MII Data Interface (KSZ8051MNL only) 21
MII Signal Definition 22
Transmit Clock (TXC) *22*
Transmit Enable (TXEN) *22*
Transmit Data [3:0] (TXD[3:0]) *22*
Receive Clock (RXC) *22*
Receive Data Valid (RXDV) *22*
Receive Data[3:0] (RXD[3:0]) *23*
Receive Error (RXER) *23*
Carrier Sense (CRS) *23*
Collision (COL) *23*
MII Signal Diagram 23
RMII Data Interface (KSZ8051RNL only) 24
RMII – 25MHz Clock Mode 24
RMII – 50MHz Clock Mode 24
RMII Signal Definition 24
Reference Clock (REF_CLK) *24*

Transmit Enable (TXEN) *25*
Transmit Data [1:0] (TXD[1:0]) *25*
Carrier Sense/Receive Data Valid (CRS_DV) *25*
Receive Data [1:0] (RXD[1:0]) *25*
Receive Error (RXER) *25*
Collision Detection *25*
RMII Signal Diagram 25
RMII – 25MHz Clock Mode *26*
RMII – 50MHz Clock Mode *26*
Back-to-Back Mode – 100Mbps Copper Repeater / Media Converter **27**
MII Back-to-Back Mode (KSZ8051MNL only) 27
RMII Back-to-Back Mode (KSZ8051RNL only) 28
MII Management (MIIM) Interface **28**
Interrupt (INTRP) **29**
HP Auto MDI/MDI-X **29**
Straight Cable 29
Crossover Cable 30
LinkMD® Cable Diagnostics **30**
NAND Tree Support **30**
NAND Tree I/O Testing 32
Power Management **32**
Power Saving Mode 32
Energy Detect Power Down Mode 32
Power Down Mode 32
Slow Oscillator Mode 32
Reference Circuit for Power and Ground Connections **33**
Register Map **34**
Register Description **34**
Register Description (Continued) **35**
Register Description (Continued) **36**
Register Description (Continued) **37**
Register Description (Continued) **38**
Register Description (Continued) **39**
Register Description (Continued) **40**
Register Description (Continued) **41**
Register Description (Continued) **42**
Register Description (Continued) **43**
Absolute Maximum Ratings(1) **44**
Operating Ratings(2) **44**
Electrical Characteristics(3) **44**
Electrical Characteristics(3) (Continued) **45**
Timing Diagrams **46**
MII SQE Timing (10Base-T) 46

MII Transmit Timing (10Base-T) 47
MII Receive Timing (10Base-T) 48
MII Transmit Timing (100Base-TX) 49
MII Receive Timing (100Base-TX) 50
RMII Timing 51
Auto-Negotiation Timing 52
MDC/MDIO Timing 53
Reset Timing 54
Reset Circuit 55
Reference Circuits for LED Strapping Pins 56
Magnetics Specification 57
Reference Clock – Connection and Selection 57
Package Information 59

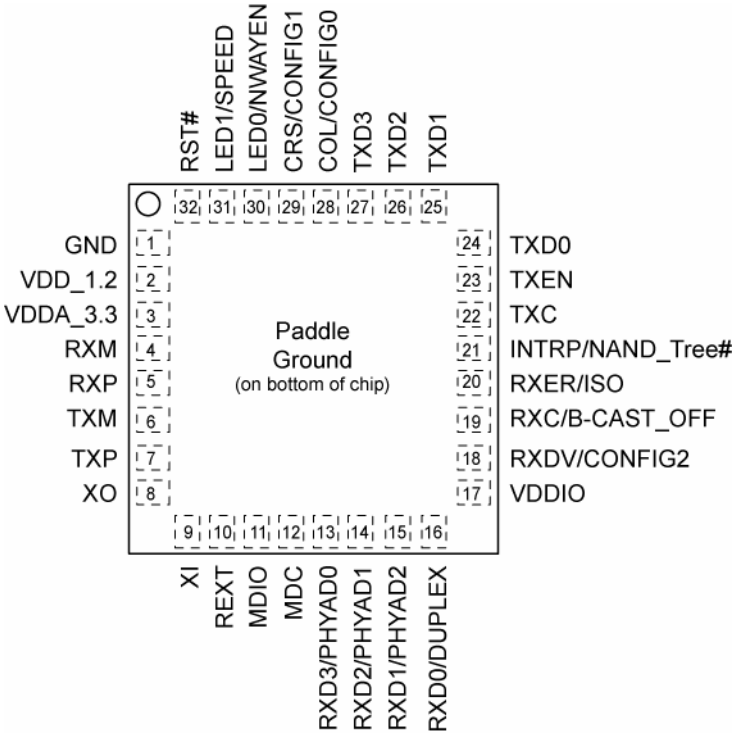
List of Figures

Figure 1. Auto-Negotiation Flow Chart 21
Figure 2. KSZ8051MNL MII Interface 23
Figure 3. KSZ8051RNL RMII Interface (25MHz Clock Mode) 26
Figure 4. KSZ8051RNL RMII Interface (50MHz Clock Mode) 26
Figure 5. KSZ8051MNL/RNL and KSZ8041FTL Back-to-Back Media Converter 27
Figure 6. Typical Straight Cable Connection 29
Figure 7. Typical Crossover Cable Connection 30
Figure 8. KSZ8051MNL/RNL Power and Ground Connections 33
Figure 9. MII SQE Timing (10Base-T) 46
Figure 10. MII Transmit Timing (10Base-T) 47
Figure 11. MII Receive Timing (10Base-T) 48
Figure 12. MII Transmit Timing (100Base-TX) 49
Figure 13. MII Receive Timing (100Base-TX) 50
Figure 14. RMII Timing – Data Received from RMII 51
Figure 15. RMII Timing – Data Input to RMII 51
Figure 16. Auto-Negotiation Fast Link Pulse (FLP) Timing 52
Figure 17. MDC/MDIO Timing 53
Figure 18. Reset Timing 54
Figure 19. Recommended Reset Circuit 55
Figure 20. Recommended Reset Circuit for interfacing with CPU/FPGA Reset Output 55
Figure 21. Reference Circuits for LED Strapping Pins 56
Figure 22. 25MHz Crystal / Oscillator Reference Clock Connection 57
Figure 23. 50MHz Oscillator Reference Clock Connection 58

List of Tables

Table 1. MII Signal Definition 22
Table 2. RMII Signal Description 24
Table 3. MII Signal Connection for MII Back-to-Back Mode (100Base-TX Copper Repeater) 27
Table 4. RMII Signal Connection for RMII Back-to-Back Mode (100Base-TX Copper Repeater) 28
Table 5. MII Management Frame Format – for KSZ8051MNL/RNL 28
Table 6. MDI/MDI-X Pin Definition 29
Table 7. NAND Tree Test Pin Order – for KSZ8051MNL 31
Table 8. NAND Tree Test Pin Order – for KSZ8051RNL 31
Table 9. KSZ8051MNL/RNL Power Pin Description 33
Table 10. MII SQE Timing (10Base-T) Parameters 46
Table 11. MII Transmit Timing (10Base-T) Parameters 47
Table 12. MII Receive Timing (10Base-T) Parameters 48
Table 13. MII Transmit Timing (100Base-TX) Parameters 49
Table 14. MII Receive Timing (100Base-TX) Parameters 50
Table 15. RMII Timing Parameters – KSZ8051RNL (25MHz input to XI pin, 50MHz output from REF_CLK pin) 51
Table 16. RMII Timing Parameters – KSZ8051RNL (50MHz input to XI pin) 51
Table 17. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters 52
Table 18. MDC/MDIO Timing Parameters 53
Table 19. Reset Timing Parameters 54
Table 20. Magnetics Selection Criteria 57
Table 21. Qualified Single Port 10/100 Magnetics 57
Table 22. 25MHz Crystal / Reference Clock Selection Criteria 58
Table 23. 50MHz Oscillator / Reference Clock Selection Criteria 58

Pin Configuration – KSZ8051MNL



32-Pin (5mm x 5mm) QFN

Pin Description – KSZ8051MNL

Pin Number	Pin Name	Type[1]	Pin Function
1	GND	Gnd	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8051MNL) Decouple with 2.2uF and 0.1uF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RXM	I/O	Physical receive or transmit signal (- differential)
5	RXP	I/O	Physical receive or transmit signal (+ differential)
6	TXM	I/O	Physical transmit or receive signal (- differential)
7	TXP	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback – for 25 MHz crystal This pin is a no connect if oscillator or external clock source is used.
9	XI	I	Crystal / Oscillator / External Clock Input 25MHz +/-50ppm
10	REXT	I	Set physical transmit output current Connect a 6.49KΩ resistor to ground on this pin.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This clock pin is synchronous to the MDIO data pin.
13	RXD3 / PHYAD0	Ipu/O	MII Mode: MII Receive Data Output[3][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See “Strapping Options” section for details.
14	RXD2 / PHYAD1	Ipd/O	MII Mode: MII Receive Data Output[2][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See “Strapping Options” section for details.
15	RXD1 / PHYAD2	Ipd/O	MII Mode: MII Receive Data Output[1][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See “Strapping Options” section for details.
16	RXD0 / DUPLEX	Ipu/O	MII Mode: MII Receive Data Output[0][2] / Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See “Strapping Options” section for details.
17	VDDIO	P	3.3V, 2.5V or 1.8V digital V_{DD}
18	RXDV / CONFIG2	Ipd/O	MII Mode: MII Receive Data Valid Output / Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See “Strapping Options” section for details.
19	RXC / B-CAST_OFF	Ipd/O	MII Mode: MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See “Strapping Options” section for details.
20	RXER / ISO	Ipd/O	MII Mode: MII Receive Error Output / Config Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See “Strapping Options” section for details.
21	INTRP /	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td></td><td>NAND_Tree#</td><td></td><td>Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>22</td><td>TXC</td><td>I/O</td><td>MII Mode: MII Transmit Clock Output
MII Back-to-Back Mode: MII Transmit Clock Input</td></tr>
<tr><td>23</td><td>TXEN</td><td>I</td><td>MII Mode: MII Transmit Enable Input</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>MII Mode: MII Transmit Data Input[0](3)</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>MII Mode: MII Transmit Data Input[1](3)</td></tr>
<tr><td>26</td><td>TXD2</td><td>I</td><td>MII Mode: MII Transmit Data Input[2](3)</td></tr>
<tr><td>27</td><td>TXD3</td><td>I</td><td>MII Mode: MII Transmit Data Input[3](3)</td></tr>
<tr><td>28</td><td>COL /
CONFIG0</td><td>Ipd/O</td><td>MII Mode: MII Collision Detect Output /
Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>CRS /
CONFIG1</td><td>Ipd/O</td><td>MII Mode: MII Carrier Sense Output /
Config Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>30</td><td>LED0 /
NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output /
Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset. See “Strapping Options” section for details.
The LED0 pin is programmable via register 1Fh bits [5:4], and is defined as follows.
<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
</table>
LED mode = [10], [11] Reserved</td></tr>
<tr><td>31</td><td>LED1 /
SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output /
Config Mode: Latched as SPEED (register 0h, bit 13) at the de-assertion of reset. See “Strapping Options” section for details.
The LED1 pin is programmable via register 1Fh bits [5:4], and is defined as follows.
<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10Base-T</td><td>High</td><td>OFF</td></tr>
<tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr>
</table>
<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>High</td><td>OFF</td></tr>
</table></td></tr>
</table>

Pin Number	Pin Name	Type[1]	Pin Function
			Activity | Toggle | Blinking **LED mode = [10], [11]** Reserved
32	RST#	I	Chip Reset (active low)
PADDLE	GND	Gnd	Ground

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.
2. MII Rx Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC. RXD[3:0] is invalid data from the PHY when RXDV is de-asserted.
3. MII Tx Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] presents valid data from the MAC. TXD[3:0] has no effect on the PHY when TXEN is de-asserted.

Strapping Options – KSZ8051MNL

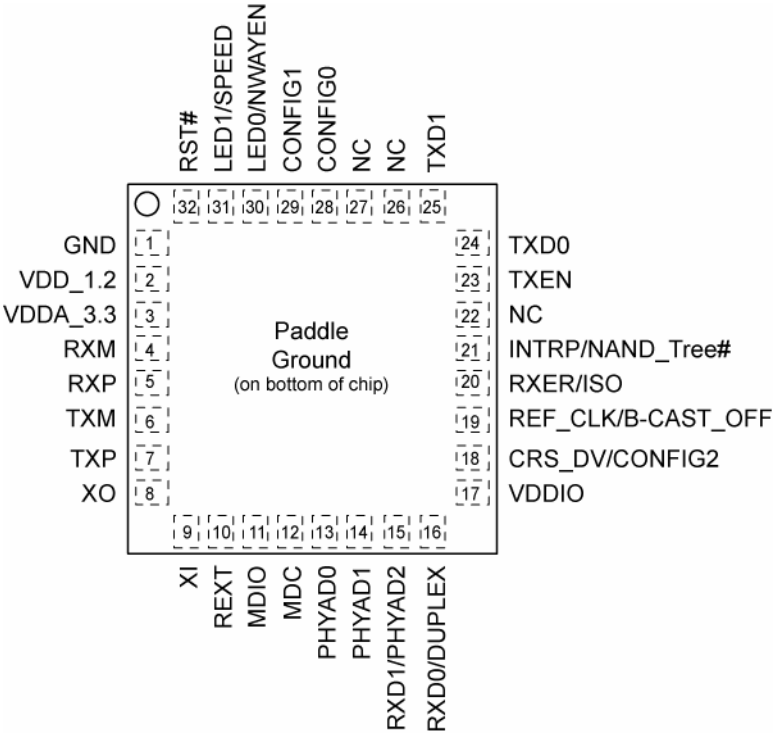
Pin Number	Pin Name	Type[1]	Pin Function
15 14 13	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7. The default PHY Address is 00001. PHY Address 00000 is enabled only if the B-CAST_OFF strapping pin is pulled high. PHY Address bits [4:3] are set to '00' by default.
18 29 28	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset. **CONFIG[2:0]** / **Mode** 000 / MII (default) 110 / MII Back-to-Back 001 – 101, 111 / Reserved – not used
20	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable At the de-assertion of reset, this pin value is latched into register 0h bit 10.
31	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps At the de-assertion of reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
16	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex At the de-assertion of reset, this pin value is latched into register 0h bit 8.
30	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation At the de-assertion of reset, this pin value is latched into register 0h bit 12.
19	B-CAST_OFF	Ipd/O	Broadcast Off – for PHY Address 0 Pull-up = PHY Address 0 is set as an unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
21	NAND_Tree#	Ipu/Opu	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Note:

1. Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to the unintended high/low states. In this case, external pull-ups (4.7K) or pull-downs (1.0K) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

Pin Configuration – KSZ8051RNL



32-Pin (5mm x 5mm) QFN

Pin Description – KSZ8051RNL

Pin Number	Pin Name	Type[1]	Pin Function
1	GND	Gnd	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8051RNL) Decouple with 2.2uF and 0.1uF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RXM	I/O	Physical receive or transmit signal (- differential)
5	RXP	I/O	Physical receive or transmit signal (+ differential)
6	TXM	I/O	Physical transmit or receive signal (- differential)
7	TXP	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback – for 25 MHz crystal This pin is a no connect if oscillator or external clock source is used.
9	XI	I	25MHz Mode: 25MHz +/-50ppm Crystal / Oscillator / External Clock Input 50MHz Mode: 50MHz +/-50ppm Oscillator / External Clock Input
10	REXT	I	Set physical transmit output current Connect a 6.49KΩ resistor-to-ground on this pin.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This clock pin is synchronous to the MDIO data pin.
13	PHYAD0	Ipu/O	The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See “Strapping Options” section for details.
14	PHYAD1	Ipd/O	The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See “Strapping Options” section for details.
15	RXD1 / PHYAD2	Ipd/O	RMII Mode: RMII Receive Data Output[1][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See “Strapping Options” section for details.
16	RXD0 / DUPLEX	Ipu/O	RMII Mode: RMII Receive Data Output[0][2] / Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See “Strapping Options” section for details.
17	VDDIO	P	3.3V, 2.5V or 1.8V digital V_{DD}
18	CRS_DV / CONFIG2	Ipd/O	RMII Mode: RMII Carrier Sense/Receive Data Valid Output / Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See “Strapping Options” section for details.
19	REF_CLK / B-CAST_OFF	Ipd/O	RMII Mode: 25MHz Mode: This pin provides the 50MHz RMII reference clock output to the MAC. See also XI (pin 9). 50MHz Mode: This pin is a no connect. See also XI (pin 9). Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See “Strapping Options” section for details.
20	RXER / ISO	Ipd/O	RMII Mode: RMII Receive Error Output / Config Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See “Strapping Options” section for details.
21	INTRP /	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td></td><td>NAND_Tree#</td><td></td><td>Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>22</td><td>NC</td><td>O</td><td>No connect- It is recommended to tie this unused pin directly to ground.</td></tr>
<tr><td>23</td><td>TXEN</td><td>I</td><td>RMII Transmit Enable Input</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>RMII Transmit Data Input[0](3)</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>RMII Transmit Data Input[1](3)</td></tr>
<tr><td>26</td><td>NC</td><td>I</td><td>No connect- It is recommended to tie this unused pin directly to ground.</td></tr>
<tr><td>27</td><td>NC</td><td>I</td><td>No connect- It is recommended to tie this unused pin directly to ground.</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>30</td><td>LED0 / NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output /
Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset. See “Strapping Options” section for details.
The LED0 pin is programmable via register 1Fh bits [5:4], and is defined as follows.

<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
</table>

LED mode = [10], [11] Reserved</td></tr>
<tr><td>31</td><td>LED1 / SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output /
Config Mode: Latched as SPEED (register 0h, bit 13) at the de-assertion of reset. See “Strapping Options” section for details.
The LED1 pin is programmable via register 1Fh bits [5:4], and is defined as follows.

<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10Base-T</td><td>High</td><td>OFF</td></tr>
<tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr>
</table>

<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>High</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

LED mode = [10], [11] Reserved</td></tr>
</table>

Pin Number	Pin Name	Type(1)	Pin Function
32	RST#	I	Chip Reset (active low)
PADDLE	GND	Gnd	Ground

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.
2. RMII Rx Mode: The RXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.
3. RMII Tx Mode: The TXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock . For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

Strapping Options – KSZ8051RNL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>15
14
13</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7.
The default PHY Address is 00001.
PHY Address 00000 is enabled only if the B-CAST_OFF strapping pin is pulled high.
PHY Address bits [4:3] are set to ‘00’ by default.</td></tr>
<tr><td>18
29
28</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.
<table>
<tr><th>CONFIG[2:0]</th><th>Mode</th></tr>
<tr><td>001</td><td>RMII</td></tr>
<tr><td>101</td><td>RMII Back-to-Back</td></tr>
<tr><td>000, 010 – 100, 110, 111</td><td>Reserved – not used</td></tr>
</table></td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>ISOLATE mode
Pull-up = Enable
Pull-down (default) = Disable
At the de-assertion of reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>SPEED mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
At the de-assertion of reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>DUPLEX mode
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
At the de-assertion of reset, this pin value is latched into register 0h bit 8.</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway Auto-Negotiation Enable
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
At the de-assertion of reset, this pin value is latched into register 0h bit 12.</td></tr>
<tr><td>19</td><td>B-CAST_OFF</td><td>Ipd/O</td><td>Broadcast Off – for PHY Address 0
Pull-up = PHY Address 0 is set as an unique PHY address
Pull-down (default) = PHY Address 0 is set as a broadcast PHY address
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
<tr><td>21</td><td>NAND_Tree#</td><td>Ipu/Opu</td><td>NAND Tree Mode
Pull-up (default) = Disable
Pull-down = Enable
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched to the unintended high/low states. In this case, external pull-ups (4.7K) or pull-downs (1.0K) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

Functional Description: 10Base-T/100Base-TX Transceiver

The KSZ8051MNL/RNL is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8051MNL/RNL supports 10Base-T and 100Base-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8051MNL offers the Media Independent Interface (MII) and the KSZ8051RNL offers the Reduced Media Independent Interface (RMII) for direct connection with MII/RMII compliant Ethernet MAC processors and switches.

The MII management bus option gives the MAC processor complete access to the KSZ8051MNL/RNL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP and RXM inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8051MNL/RNL decodes a data frame. The receive clock is kept active during idle periods in between data reception.

Scrambler/De-scrambler (100Base-TX only)

The scrambler is used to spread the power spectrum of the transmitted signal to reduce EMI and baseline wander, and the de-scrambler is needed to recover the scrambled signal.

SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

PLL Clock Synthesizer

The KSZ8051MNL/RNL generates all internal clocks and all external clocks for system timing from an external 25MHz crystal, oscillator, or reference clock. For the KSZ8051RNL in RMII 50MHz clock mode, these clocks are generated from an external 50MHz oscillator or system clock.

Auto-Negotiation

The KSZ8051MNL/RNL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8051MNL/RNL link partner is forced to bypass auto-negotiation, then the KSZ8051MNL/RNL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8051MNL/RNL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (NWAYEN, pin 30) or software (register 0h, bit 12).

By default, auto-negotiation is enabled after power-up or hardware reset. Afterwards, auto-negotiation can be enabled or disabled by register 0h, bit 12. If auto-negotiation is disabled, the speed is set by register 0h, bit 13, and the duplex is set by register 0h, bit 8.

The auto-negotiation link up process is shown in the following flow chart.

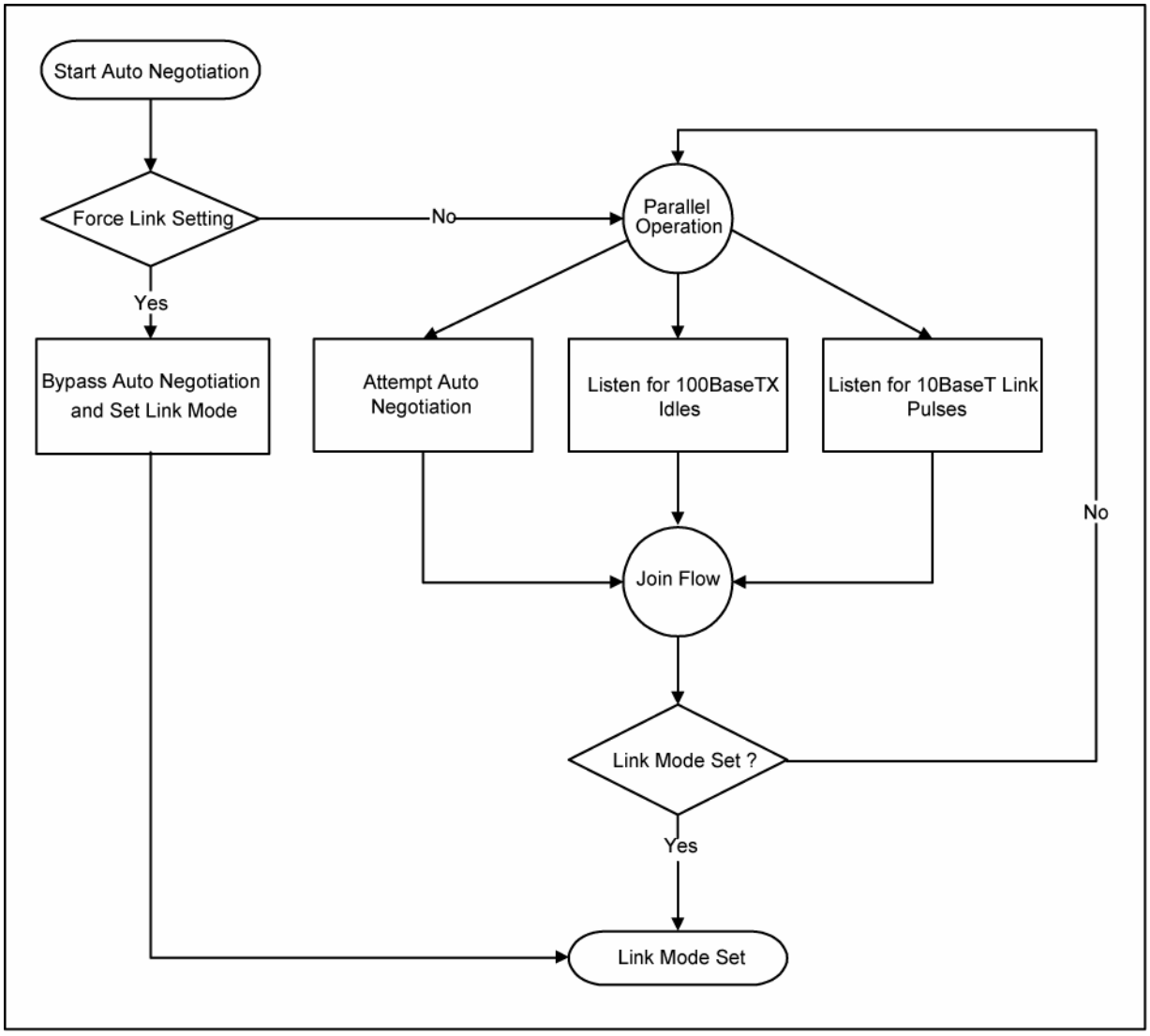


Figure 1. Auto-Negotiation Flow Chart

MII Data Interface (KSZ8051MNL only)

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 15 pins (6 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10Mbps and 100Mbps data rates are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

By default, the KSZ8051MNL is configured to MII mode after it is powered up or hardware reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to ‘000’ (default setting).

MII Signal Definition

The following table describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

MII Signal Name	Direction (with respect to PHY, KSZ8051MNL signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

Table 1. MII Signal Definition

Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

Transmit Data [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is ”00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY’s reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY’s reference clock.

RXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), “5D”, and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

Receive Data[3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g., a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based upon the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

MII Signal Diagram

The KSZ8051MNL MII pin connections to the MAC are shown in the following figure.

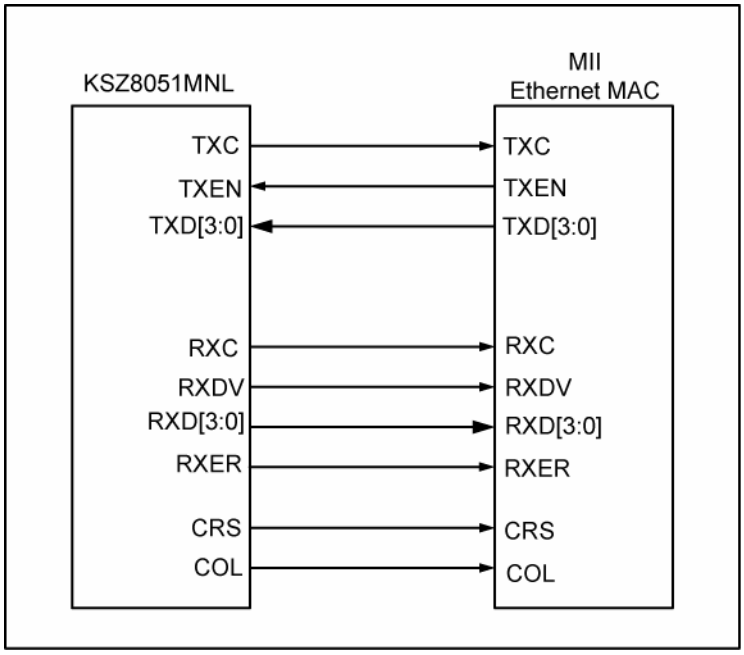


Figure 2. KSZ8051MNL MII Interface

RMII Data Interface (KSZ8051RNL only)

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, 1 pin for the 50MHz reference clock).
- 10Mbps and 100Mbps data rates are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2-bit wide, a dibit.

RMII – 25MHz Clock Mode

The KSZ8051RNL is configured to RMII – 25MHz Clock Mode after it is powered up or hardware reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to '001'.
- Register 1Fh, bit 7 is set to '0' (default value) to select 25MHz Clock Mode.

RMII – 50MHz Clock Mode

The KSZ8051RNL is configured to RMII – 50MHz Clock Mode after it is powered up or hardware reset with the following:

- An external 50MHz clock source (oscillator) connected to XI (pin 9).
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to '001'.
- Register 1Fh, bit 7 is set to '1' to select 50MHz Clock Mode.

RMII Signal Definition

The following table describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.

RMII Signal Name	Direction (with respect to PHY, KSZ8051RNL signal)	Direction (with respect to MAC)	Description
REF_CLK	Output (25MHz clock mode) / <no connect> (50MHz clock mode)	Input / Input or <no connect>	Synchronous 50 MHz reference clock for receive, transmit and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RXER	Output	Input, or (not required)	Receive Error

Table 2. RMII Signal Description

Reference Clock (REF_CLK)

REF_CLK is a continuous 50MHz clock that provides the timing reference for TX_EN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For 25MHz Clock Mode, the KSZ8051RNL generates and outputs the 50MHz RMII REF_CLK to the MAC at REF_CLK (pin 19).

For 50MHz Clock Mode, the KSZ8051RNL takes in the 50MHz RMII REF_CLK from the MAC or system board at XI (pin 9) and has the REF_CLK (pin 19) left as a no connect.

Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII, and is negated prior to the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

Transmit Data [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TXEN is asserted, TXD[1:0] are accepted for transmission by the PHY.

TXD[1:0] is ”00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[1:0] while TXEN is de-asserted are ignored by the PHY.

Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of carrier. This is when squelch is passed in 10Mbps mode, and when 2 non-contiguous zeroes in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

So long as carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit, and it is negated prior to the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is "00" until proper receive signal decoding takes place.

Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously with respect to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] is "00" to indicate idle when CRS_DV is de-asserted. Values other than “00” on RXD[1:0] while CRS_DV is de-asserted are ignored by the MAC.

Receive Error (RXER)

RXER is asserted for one or more REF_CLK periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER has no effect on the MAC.

Collision Detection

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

RMII Signal Diagram

The KSZ8051RNL RMII pin connections to the MAC are shown in the following figures for 25MHz Clock Mode and 50MHz Clock Mode.