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KSZ8061MNX/MNG

10BASE-T/100 BASE-TX Physical Layer Transceiver

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Quiet-WIRE® technology to reduce line emissions and enhance immunity
- Ultra-Deep Sleep standby mode
- AEC-Q100 Grade 2 Automotive

Target Applications

- Industrial control
- Vehicle on-board diagnostics (OBD)
- Automotive gateways
- Camera and sensor networking
- Infotainment

Features

- Quiet-WIRE programmable EMI filter
- MII interface with MDC/MDIO management interface for register configuration
- On-chip termination resistors for the differential pairs
- LinkMD®+ receive signal quality indicator
- Fast start-up and link
- Ultra-Deep Sleep standby mode: CPU or signal detect activated.
- Loopback modes for diagnostics
- Programmable interrupt output

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8061MNX/MNG is a single-chip, 10BASE-T/100BASE-TX, Ethernet physical layer transceiver for transmission and reception of data over unshielded twisted pair (UTP) cable.

The KSZ8061MNX/MNG features Quiet-WIRE® internal filtering to reduce line emissions. It is ideal for applications, such as automotive or industrial networks, where stringent radiated emission limits need to be met. Quiet-WIRE can use low-cost unshielded cable, where previously only shielded cable solutions were possible. The KSZ8061MNX/MNG also features enhanced immunity to environmental EM noise.

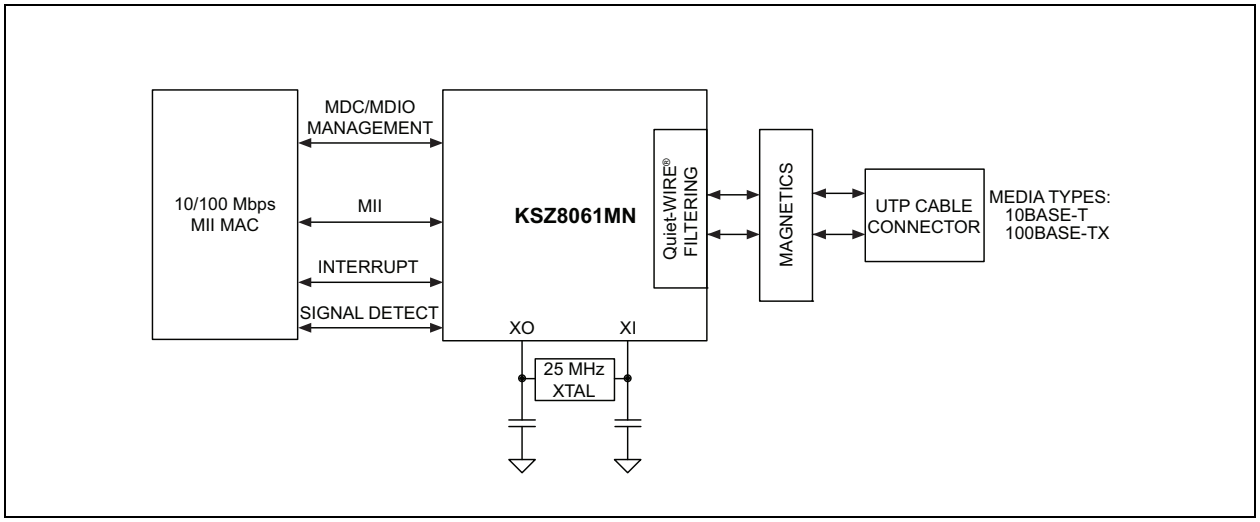
The KSZ8061MNX/MNG offers the Media Independent Interface (MII) for direct connection with MII-compliant Ethernet MAC processors and switches.

It is designed to exceed Automotive AEC-Q100 and EMC requirements, and features an extended temperature range of –40°C to +105°C.

The KSZ8061MNX is supplied in a 32-lead, 5 mm × 5 mm QFN or WQFN package, while the KSZ8061MNG is in a 48-lead, 7 mm × 7 mm QFN package.

The KSZ8061RNB and KSZ8061RND devices have an RMII interface and are described in a separate data sheet.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 32-QFN OR WQFN KSZ8061MNX PIN ASSIGNMENT (TOP VIEW)

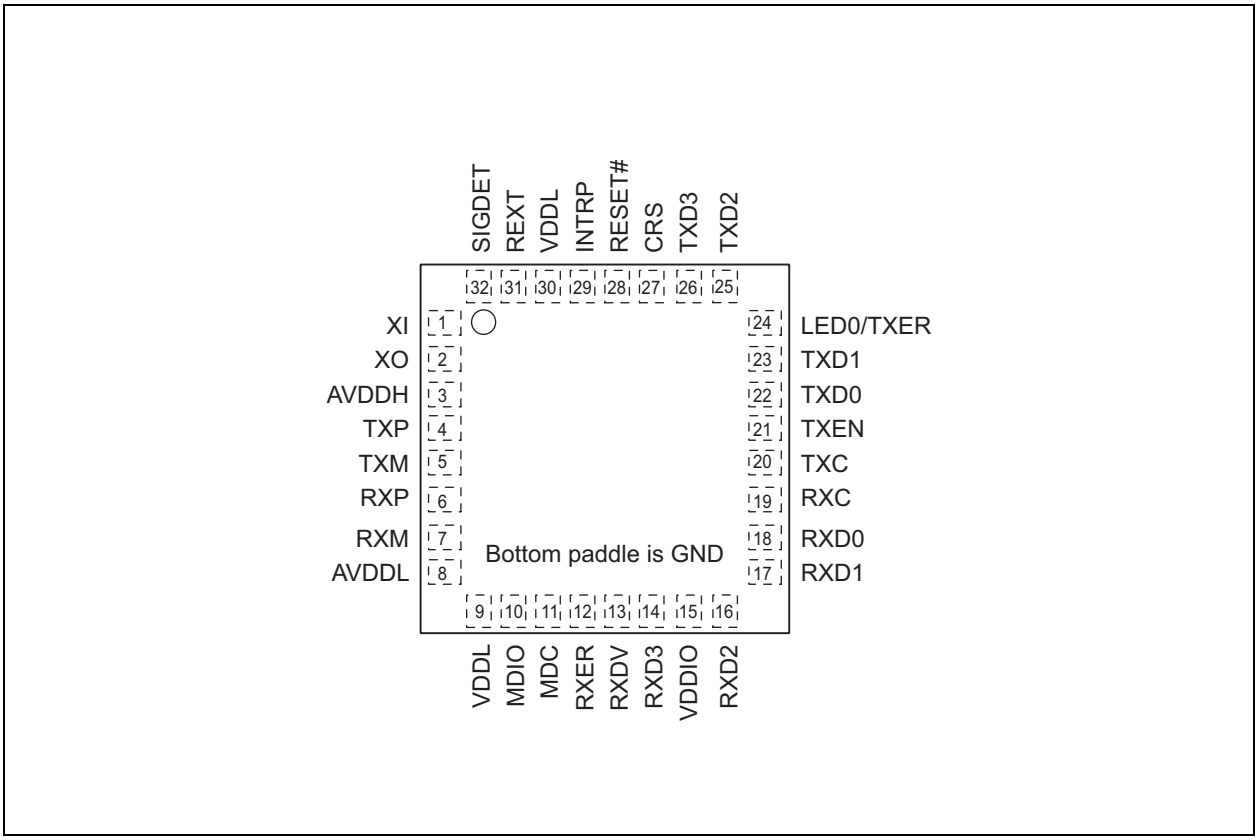


TABLE 2-1: SIGNALS - KSZ8061MNX (32-PIN PACKAGES)

Pin Number	Name	Type Note 2-1	Description
1	XI	I	Crystal/Oscillator/External Clock Input 25 MHz ±50ppm. This input references the AVDDH power supply.
2	XO	O	Crystal feedback for 25 MHz crystal This pin is a no connect if oscillator or external clock source is used.
3	AVDDH	Pwr	3.3V supply for analog TX drivers and XI/XO oscillator circuit.
4	TXP	I/O	Physical transmit or receive signal (+ differential) Transmit when in MDI mode; Receive when in MDI-X mode
5	TXM	I/O	Physical transmit or receive signal (– differential) Transmit when in MDI mode; Receive when in MDI-X mode
6	RXP	I/O	Physical receive or transmit signal (+ differential) Receive when in MDI mode; Transmit when in MDI-X mode

TABLE 2-1: SIGNALS - KSZ8061MNX (32-PIN PACKAGES) (CONTINUED)

Pin Number	Name	Type Note 2-1	Description
7	RXM	I/O	Physical receive or transmit signal (– differential) Receive when in MDI mode; Transmit when in MDI-X mode
8	AVDDL	Pwr	1.2V (nominal) supply for analog core
9	VDDL	Pwr	1.2V (nominal) supply for digital core
10	MDIO	Ipu/Opu	Management Interface (MIIM) Data I/O This pin has a weak pull-up, is open-drain like, and requires an external 1.0 kΩ pull-up resistor.
11	MDC	Ipu	Management Interface (MIIM) Clock Input This clock pin is synchronous to the MDIO data pin.
12	RXER/QWF	Ipd/O	MII Receive Error Output Config Mode: The pull-up/pull-down value is latched as QWF at the de-assertion of reset. See Table 2-2 for details.
13	RXDV/ CONFIG2	Ipd/O	MII Receive Data Valid Output Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See Table 2-2 for details.
14	RXD3/ PHYAD0	Ipu/O	MII Receive Data Output[3] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See Table 2-2 for details.
15	VDDIO	Pwr	3.3V, 2.5V, or 1.8V supply for digital I/O
16	RXD2/ PHYAD1	Ipd/O	MII Receive Data Output[2] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See Table 2-2 for details.
17	RXD1/ PHYAD2	Ipd/O	MII Receive Data Output[1] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See Table 2-2 for details.
18	RXD0/ AUTONEG	Ipu/O	MII Receive Data Output[0] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as AUTONEG at the de-assertion of reset. See Table 2-2 for details.
19	RXC/ CONFIG0	Ipd/O	MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See Table 2-2 for details.
20	TXC	O	MII Transmit Clock Output
21	TXEN	I	MII Transmit Enable Input
22	TXD0	I	MII Transmit Data Input[0] (Note 2-3)
23	TXD1	I	MII Transmit Data Input[1] (Note 2-3)
24	LED0	O	LED0 Output
25	TXD2	I	MII Transmit Data Input[2] (Note 2-3)
26	TXD3	I	MII Transmit Data Input[3] (Note 2-3)

TABLE 2-1: SIGNALS - KSZ8061MNX (32-PIN PACKAGES) (CONTINUED)

Pin Number	Name	Type Note 2-1	Description
27	CRS/ CONFIG1	Ipd/O	MII Carrier Sense Output Config Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See Table 2-2 for details.
28	RESET#	Ipu	Chip Reset (active low)
29	INTRP/ NAND_Tree#	Ipu/O	Programmable Interrupt Output (active low (default) or active high) This pin has a weak pull-up, is open drain like, and requires an external 1.0 kΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset. See Table 2-2 for details.
30	VDDL	Pwr	1.2V (nominal) supply for digital (and analog)
31	REXT	I	Set PHY transmit output current Connect a 6.04 kΩ 1% resistor from this pin to ground.
32	SIGDET	O	Signal Detect, active high
Bottom Paddle	GND	Gnd	Ground

Note 2-1 Pwr = power supply
Gnd = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value).
Ipd = Input with internal pull-down (see Section 6.0, "Electrical Characteristics" for value).
Ipu/O = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input and output with internal pull-up (see Section 6.0, "Electrical Characteristics" for value).

Note 2-2 MII Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC device.

Note 2-3 MII Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] accepts valid data from the MAC device.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to the unintended high/low states. In this case, external pull-up or pull-down resistors (4.7 kΩ) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8061MNX (32-PIN PACKAGES)

Pin Number	Pin Name	Type Note 2-1	Description
17 16 14	RXD1/PHYAD2 RXD2/PHYAD1 RXD3/PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are set to 00 by default.
13 27 19	RXDV/CONFIG2 CRS/CONFIG1 RXC/CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.

CONFIG[2:0]	Mode
000 (default)	MII normal mode; Auto MDI/MDI-X disabled.
001	Reserved, not used.
010	MII normal mode; Auto MDI/MDI-X enabled.
011 - 101	Reserved, not used.
110	MII Back-to-Back; Auto MDI/MDI-X enabled.
111	Reserved, not used.

18	RXD0/ AUTONEG	Ipu/O	Auto-Negotiation Disable Pull-up (default) = Disable Auto-Negotiation Pull-down = Enable Auto-Negotiation At the de-assertion of reset, this pin value is inverted, and then latched into register 0h, bit [12].
29	INTRP/ NAND_Tree#	Ipu/O	NAND Tree Mode Pull-up (default) = Disable NAND Tree (normal operation) Pull-down = Enable NAND Tree At the de-assertion of reset, this pin value is latched by the chip.
12	RXER/QWF	Ipd/O	Quiet-WIRE® Filtering Disable Pull-up = Disable Quiet-WIRE Filtering Pull-down (default) = Enable Quiet-WIRE Filtering At the de-assertion of reset, this pin value is latched by the chip.

Note 2-1 Ipu/O = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.

FIGURE 2-2: 48-QFN KSZ8061MNG PIN ASSIGNMENT (TOP VIEW)

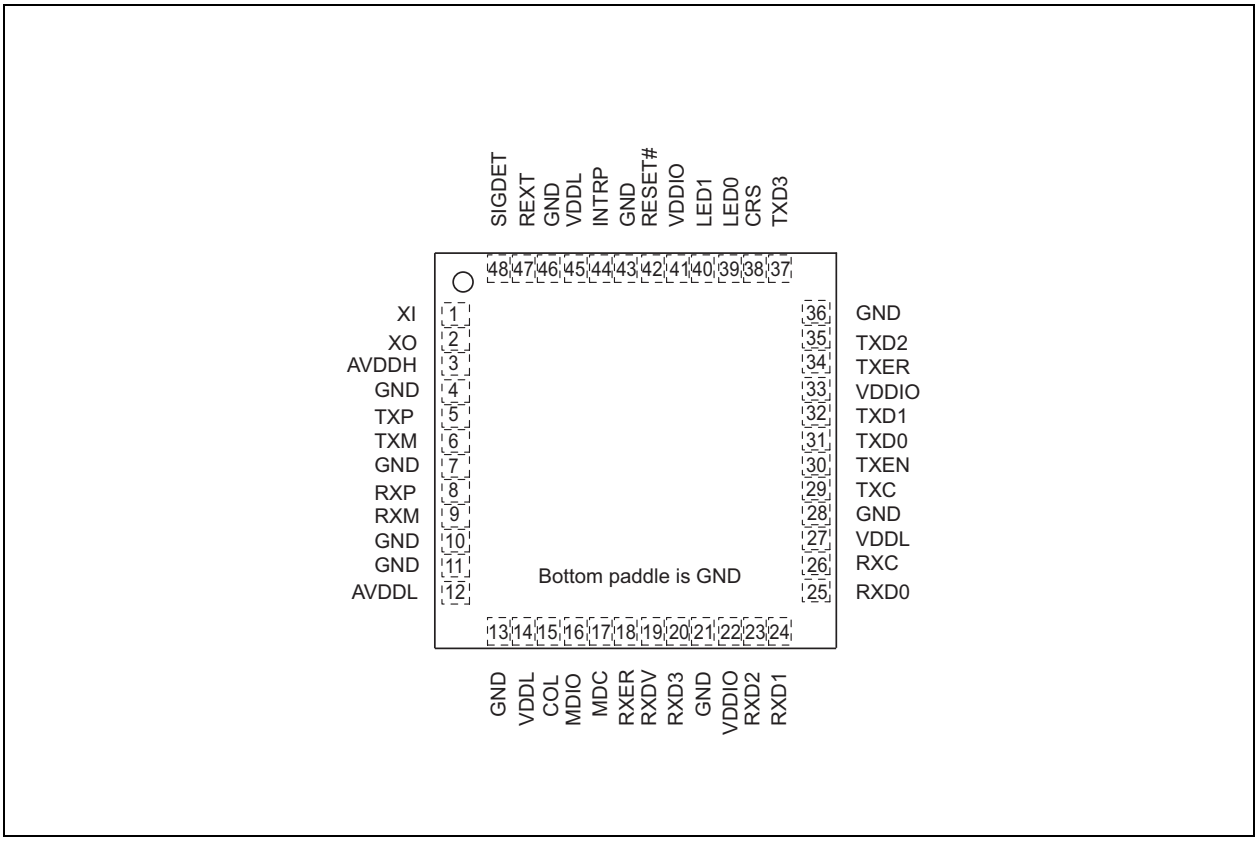


TABLE 2-3: SIGNALS - KSZ8061MNG (48-PIN PACKAGE)

Pin Number	Pin Name	Type Note 2-1	Description
1	XI	I	Crystal/Oscillator/External Clock Input 25 MHz ±50 ppm. This input references the AVDDH power supply.
2	XO	O	Crystal feedback for 25 MHz crystal This pin is a no connect if oscillator or external clock source is used.
3	AVDDH	Pwr	3.3V supply for analog TX drivers and XI/XO oscillator circuit.
4	GND	Gnd	Ground.
5	TXP	I/O	Physical transmit or receive signal (+ differential).
6	TXM	I/O	Physical transmit or receive signal (– differential).
7	GND	Gnd	Ground.
8	RXP	I/O	Physical receive or transmit signal (+ differential).
9	RXM	I/O	Physical receive or transmit signal (– differential).
10	GND	Gnd	Ground.
11	GND	Gnd	Ground.
12	AVDDL	Pwr	1.2V (nominal) supply for analog core.
13	GND	Gnd	Ground.
14	VDDL	Pwr	1.2V (nominal) supply for digital core.

TABLE 2-3: SIGNALS - KSZ8061MNG (48-PIN PACKAGE) (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
15	COL/B-CAST_OFF	Ipd/O	MII Collision Detect Output Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See Table 2-4 for details.
16	MDIO	Ipu/Opu	Management Interface (MIIM) Data I/O This pin has a weak pull-up, is open-drain like, and requires an external 1.0 kΩ pull-up resistor.
17	MDC	Ipu	Management Interface (MIIM) Clock Input This clock pin is synchronous to the MDIO data pin.
18	RXER/QWF	Ipd/O	MII Receive Error Output Config Mode: The pull-up/pull-down value is latched as QWF at the de-assertion of reset. See Table 2-4 for details.
19	RXDV/ CONFIG2	Ipd/O	MII Receive Data Valid Output Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See Table 2-4 for details.
20	RXD3/PHYAD0	Ipu/O	MII Receive Data Output[3] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See Table 2-4 for details.
21	GND	Gnd	Ground.
22	VDDIO	Pwr	3.3V, 2.5V, or 1.8V supply for digital I/O.
23	RXD2/PHYAD1	Ipd/O	MII Receive Data Output[2] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See Table 2-4 for details.
24	RXD1/PHYAD2	Ipd/O	MII Receive Data Output[1] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See Table 2-4 for details.
25	RXD0/ DUPLEX	Ipu/O	MII Receive Data Output[0] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See Table 2-4 for details.
26	RXC/CONFIG0	Ipd/O	MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See Table 2-4 for details.
27	VDDL	Pwr	1.2V (nominal) supply for digital core.
28	GND	Gnd	Ground.
29	TXC	O	MII Transmit Clock Output.
30	TXEN	I	MII Transmit Enable Input.
31	TXD0	I	MII Transmit Data Input[0]. (Note 2-3)
32	TXD1	I	MII Transmit Data Input[1]. (Note 2-3)
33	VDDIO	Pwr	3.3V, 2.5V, or 1.8V supply for digital I/O.
34	TXER	Ipd	MII Transmit Error Input If the MAC does not provide a TXER output signal, this pin may be unconnected.
35	TXD2	I	MII Transmit Data Input[2]. (Note 2-3)
36	GND	Gnd	Ground.
37	TXD3	I	MII Transmit Data Input[3]. (Note 2-3)
38	CRS/CONFIG1	Ipd/O	MII Carrier Sense Output Config Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See Table 2-4 for details.

TABLE 2-3: SIGNALS - KSZ8061MNG (48-PIN PACKAGE) (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
39	LED0/ AUTONEG	Ipu/O	LED0 Active low. Its function is programmable; by default it indicates link/ activity. Config Mode: The pull-up/pull-down value is latched as AUTONEG at the de-assertion of reset. See Table 2-4 for details.
40	LED1/SPEED	Ipu/O	LED1 Active low. Its function is programmable; by default it indicates link speed. Config Mode: The pull-up/pull-down value is latched as SPEED at the de-assertion of reset. See Table 2-4 for details.
41	VDDIO	Pwr	3.3V, 2.5V, or 1.8V supply for digital I/O.
42	RESET#	Ipu	Chip Reset (active low).
43	GND	Gnd	Ground.
44	INTRP/ NAND_Tree#	Ipu/O	Programmable Interrupt Output [active low (default) or active high] This pin has a weak pull-up, is open drain like, and requires an external 1.0 kΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset. See Table 2-4 for details.
45	VDDL	Pwr	1.2V (nominal) supply for digital (and analog).
46	GND	Gnd	Ground.
47	REXT	I	Set PHY transmit output current. Connect a 6.04 kΩ 1% resistor from this pin to ground.
48	SIGDET	O	Signal Detect, active high.
Bottom Paddle	GND	Gnd	Ground.

Note 2-1 Pwr = power supply
Gnd = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value).
Ipd = Input with internal pull-down (see Section 6.0, "Electrical Characteristics" for value).
Ipu/O = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input and output with internal pull-up (see Section 6.0, "Electrical Characteristics" for value).

Note 2-2 MII Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC device.

Note 2-3 MII Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] accepts valid data from the MAC device.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to the unintended high/low states. In this case, external pull-ups or pull-down resistors (4.7 kΩ) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

TABLE 2-4: STRAP-IN OPTIONS - KSZ8061MNG (48-PIN PACKAGE)

Pin Number	Pin Name	Type Note 2-1	Description
24 23 20	RXD1/PHYAD2 RXD2/PHYAD1 RXD3/PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are set to 00 by default.
19 38 26	RXDV/CONFIG2 CRS/CONFIG1 RXC/CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset. **CONFIG[2:0]** — **Mode** 000 (default) — MII normal mode; Auto MDI/MDI-X disabled. 001 — Reserved, not used. 010 — MII normal mode; Auto MDI/MDI-X enabled. 011 - 101 — Reserved, not used. 110 — MII normal mode; Auto MDI/MDI-X enabled. 111 — Reserved, not used.
39	LED0/AUTONEG	Ipu/O	Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation At the de-assertion of reset, this pin value is latched into register 0h, bit [12].
44	INTRP/ NAND_Tree#	Ipu/O	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.
18	RXER/QWF	Ipd/O	Quiet-WIRE Filtering Disable Pull-up = Disable Quiet-WIRE Filtering Pull-down (default) = Enable Quiet-WIRE Filtering At the de-assertion of reset, this pin value is latched by the chip.
40	LED1/SPEED	Ipu/O	Speed mode Pull-up (default) = 100Mbps Pull-down = 10Mbps At the de-assertion of reset, this pin value is latched into register 0h, bit [13] as the speed select, and also is latched into register 4h (auto-negotiation advertisement) as the speed capability support.
25	RXD0/DUPLEX	Ipu/O	Duplex mode Pull-up (default) = Half-duplex Pull-down = Full-duplex At the de-assertion of reset, this pin value is inverted, and then latched into register 0h, bit [8].
15	COL/ B-CAST_OFF	Ipd/O	Broadcast off – for PHY Address 0 Pull-up = PHY Address 0 is set as a unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.

Note 2-1 Ipu/O = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8061MN is an integrated Fast Ethernet transceiver that features Quiet-WIRE® internal filtering to reduce line emissions. When Quiet-WIRE filtering is disabled, it is fully compliant with the IEEE 802.3 specification. The KSZ8061 also has high noise immunity.

On the copper media side, the KSZ8061MN supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 or similar unshielded twisted pair (UTP) cable and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8061MN offers the Media Independent Interface (MII) for direct connection with MII-compliant Ethernet MAC processors and switches.

The MII management bus gives the MAC processor complete access to the KSZ8061MN control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Auto-negotiation and Auto MDI/MDI-X can be disabled at power-on to significantly reduce initial time to link up.

A signal detect pin (SIGDET) is available to indicate when the link partner in inactive. An option is available for the KSZ8061MN to automatically enter Ultra-Deep Sleep mode automatically when SIGDET is de-asserted. Ultra-Deep Sleep mode may also be entered by command of the MAC processor. Additional low power modes are available.

3.1 Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion that converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by a precision external resistor on REXT for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler is used to spread the power spectrum of the transmitted signal to reduce EMI and baseline wander. The de-scrambler is needed to recover the scrambled signal.

3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10BASE-T signals with a typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP and RXM inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8061MN decodes a data frame. The receive clock is kept active during idle periods in between data reception.

3.1.6 SQE AND JABBER FUNCTION (10BASE-T ONLY; NOT SUPPORTED IN 32-PIN PACKAGE)

In 10BASE-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE test is required as part of the 10BASE-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10BASE-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10BASE-T transmitter is re-enabled and COL is de-asserted (returns to low).

3.1.7 PLL CLOCK SYNTHESIZER

The KSZ8061MN generates all internal clocks and all external clocks for system timing from an external 25 MHz crystal, oscillator, or reference clock.

3.1.8 AUTO-NEGOTIATION

The KSZ8061MN conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 specification. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

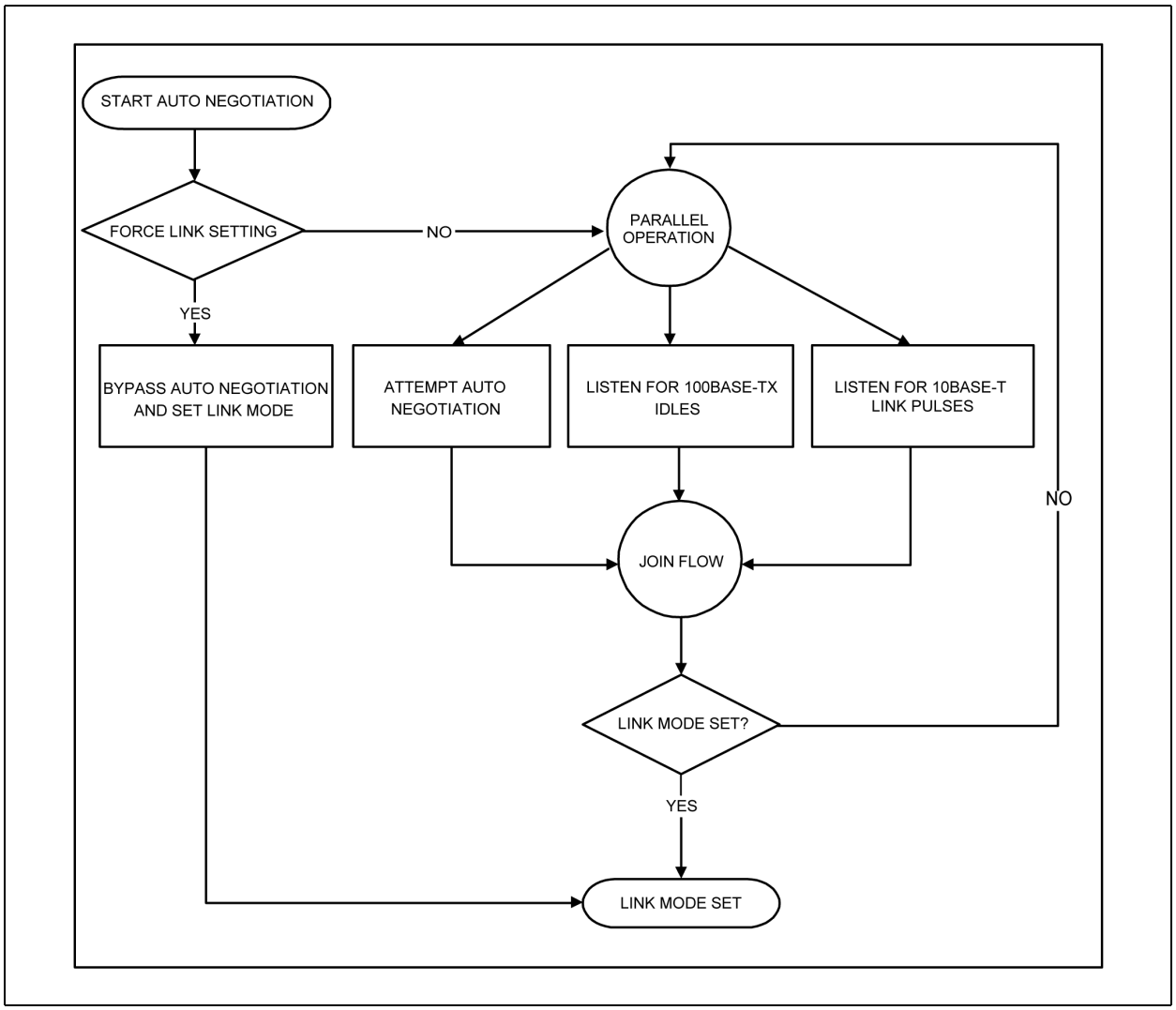
If the KSZ8061MN is using auto-negotiation, but its link partner is not, then the KSZ8061MN sets its operating speed by observing the signal at its receiver. This is known as parallel detection and allows the KSZ8061MN to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. Duplex is set by register 0h, bit [8] because the KSZ8061MN cannot determine duplex by parallel detection.

If auto-negotiation is disabled, the speed is set by register 0h, bit [13], and the duplex is set by register 0h, bit [8]. For the 48-pin device, these two bits are initialized at power-up/reset by strapping options on pins 40 and 25, respectively. For the 32-pin device, the default is 100BASE-TX, full-duplex, and there are no strapping options to change this default.

Auto-negotiation is enabled or disabled by hardware pin strapping (AUTONEG) and by software (register 0h, bit [12]). By default, auto-negotiation is enabled in the 48-pin device after power-up or hardware reset, but it may be disabled by pulling the LED0 pin low at that time. For the 32-pin device, auto-negotiation is disabled by default, but it may be enabled by pulling the RXD0 pin low during reset. Afterwards, auto-negotiation can be enabled or disabled by register 0h, bit [12]. When the link is 10BASE-T or the link partner is using auto-negotiation, and the Ultra-Deep Sleep mode is used, then the Signal Detect assertion timing delay bit, register 14h bit [1], must be set.

The auto-negotiation link up process is shown in Figure 3-1.

FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART



3.2 Quiet-WIRE® Filtering

Quiet-WIRE is a feature to enhance 100BASE-TX EMC performance by reducing both conducted and radiated emissions from the TXP/M signal pair. It can be used either to reduce absolute emissions, or to enable replacement of shielded cable with unshielded cable, all while maintaining interoperability with standard 100BASE-TX devices.

Quiet-WIRE filtering is implemented internally, with no additional external components required. It is enabled or disabled at power-up and reset by a strapping option on the RXER pin. Once the KSZ8061 is powered up, Quiet-WIRE can be disabled by writing to register 16h, bit [12].

The default setting for Quiet-WIRE reduces emissions primarily above 60 MHz, with less reduction at lower frequencies. Several dB of reduction is possible. Signal attenuation is approximately equivalent to increasing the cable length by 10 to 20 meters, thus reducing cable reach by that amount. For applications needing more modest improvement in emissions, the level of filtering can be reduced by writing a series of registers.

3.3 Fast Link-Up

Link-up time is normally determined by the time it takes to complete auto-negotiation. Additional time may be added by the auto MDI/MDI-X feature. The total link-up time from power-up or cable-connect is typically a second or more.

Fast link-up mode significantly reduces 100BASE-TX link-up time by disabling both auto-negotiation and auto MDI/MDI-X, and fixing the TX and RX channels. This is done via the CONFIG[2:0] and AUTONEG strapping options. Because these are strapping options, fast link-up is available immediately upon power-up. Fast link-up is available only for 100BASE-TX link speed. To force the link speed to 10BASE-TX requires a register write.

Fast link-up is intended for specialized applications where both link partners are known in advance. The link must also be known so that the fixed transmit channel of one device connects to the fixed receive channel of the other device, and vice versa.

If a device in fast link-up mode is connected to a normal device (auto-negotiate and auto-MDI/MDI-X), there will be no problems linking, but the speed advantage of fast link-up will not be realized.

3.4 Internal and External RX Termination

By default, the RX differential pair is internally terminated. This minimizes board component count by eliminating all components between the KSZ8061MN and the magnetics (transformer and common mode choke). The KSZ8061MN has the option to turn off the internal termination and allow the use of external termination. External termination does increase the external component count, but these external components can be of tighter tolerances than the internal termination resistors. Enabling or disabling of internal RX termination is controlled by register 14h, bit [2].

If external termination is used in place of the internal termination, it should consist of a 100Ω resistor between RXP and RXM, with a 0.1 µF or 1 µF capacitor at the midpoint.

3.5 MII Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

KSZ8061MNG (48-pin package) has full MII:

- Pin count is 16 pins (7 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10 Mbps and 100 Mbps data rates are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

KSZ8061MNX (32-pin package) has MII-Lite:

- Pin count is 15 pins (no COL signal).
- Full duplex only. Half duplex is not supported.

3.5.1 MII SIGNAL DEFINITION

Table 3-1 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 specification for detailed information.

TABLE 3-1: MII SIGNAL

MII Signal Name	Direction (KSZ8061MN Signal)	Direction (with respect to MAC device)	Description
TXC	Output	Input	Transmit Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
TXER	Input	Output	Transmit Error (not implemented)
RXC	Output	Input	Receive Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection (KSZ8061MNG only)

3.5.1.1 Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0]. When the PHY links at 10 Mbps, TXC is 2.5 MHz. When the PHY links at 100 Mbps, TXC is 25 MHz.

3.5.1.2 Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame. TXEN transitions synchronously with respect to TXC.

3.5.1.3 Transmit Error (TXER)

The TXER symbol error function for the transmitted frame onto the line is not implemented in this device.

3.5.1.4 Transmit Data [3:0] (TXD[3:0])

When TXEN is asserted, TXD[3:0] are the data nibbles accepted by the PHY for transmission. TXD[3:0] is 00 to indicate idle when TXEN is de-asserted. TXD[3:0] transitions synchronously with respect to TXC.

3.5.1.5 Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10 Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY's reference clock when the line is idle, or link is down.
- In 100 Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY's reference clock.

When the PHY links at 10 Mbps, RXC is 2.5 MHz. When the PHY links at 100 Mbps, RXC is 25 MHz.

3.5.1.6 Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10 Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), 5Dh, and remains asserted until the end of the frame.
- In 100 Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

3.5.1.7 Receive Data[3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

3.5.1.8 Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY. RXER transitions synchronously with respect to RXC.

3.5.1.9 Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10 Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based upon the reception of an end-of-frame (EOF) marker.
- In 100 Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

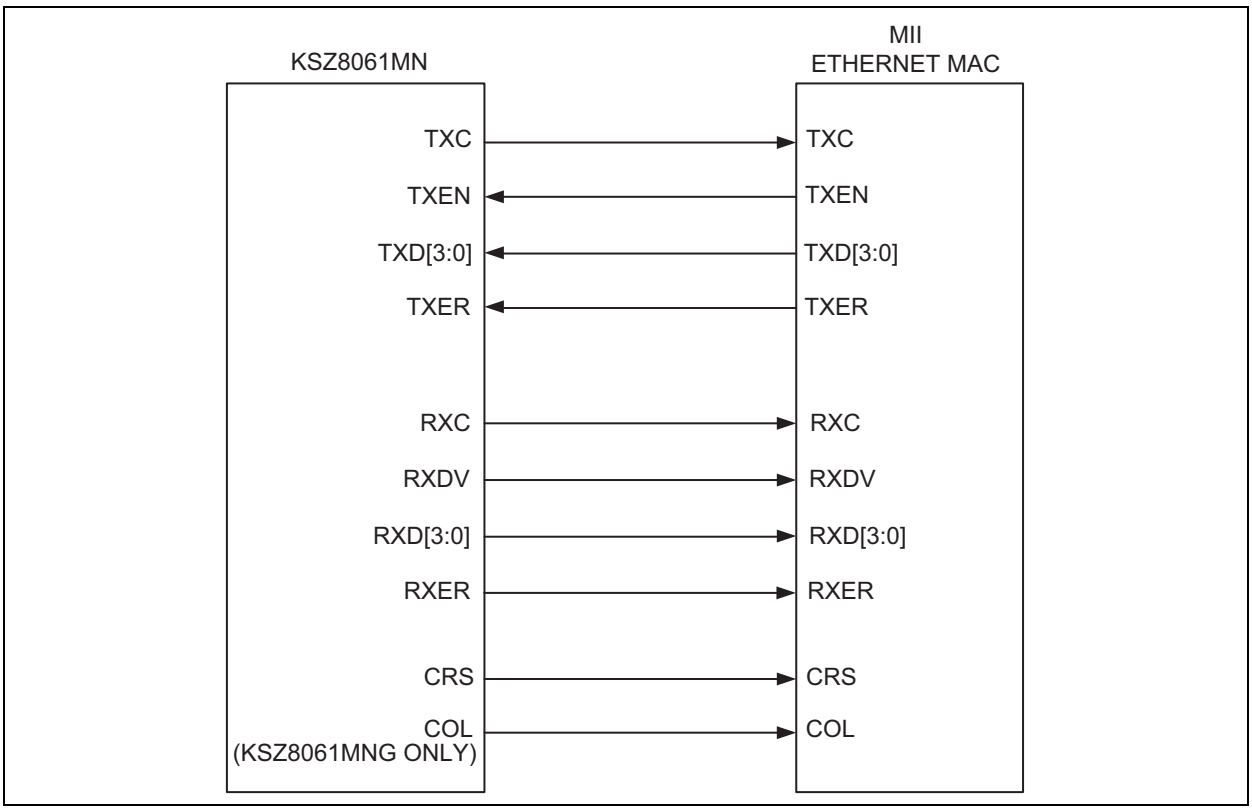
3.5.1.10 Carrier Sense (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This informs the MAC that a collision has occurred during its transmission to the PHY. COL is supported only in the 48-pin package option. Therefore the 32-pin package option does not support half duplex. When interfacing the 32-pin device to a MAC with a COL input, that input should be pulled low.

3.5.2 MII SIGNAL DIAGRAM

The KSZ8061MN MII pin connections to the MAC are shown in Figure 3-2.

FIGURE 3-2: KSZ8061MN MII INTERFACE



3.6 Back-to-Back Mode – 100 Mbps Repeater

Two KSZ8061MN devices can be connected back-to-back to form a 100BASE-TX to 100BASE-TX repeater. For testing purposes, it can also be used to loopback data on the MII bus by physically connecting the MII receive bus to the MII transmit bus.

FIGURE 3-3: KSZ8061MN TO KSZ8061MN BACK-TO-BACK REPEATER

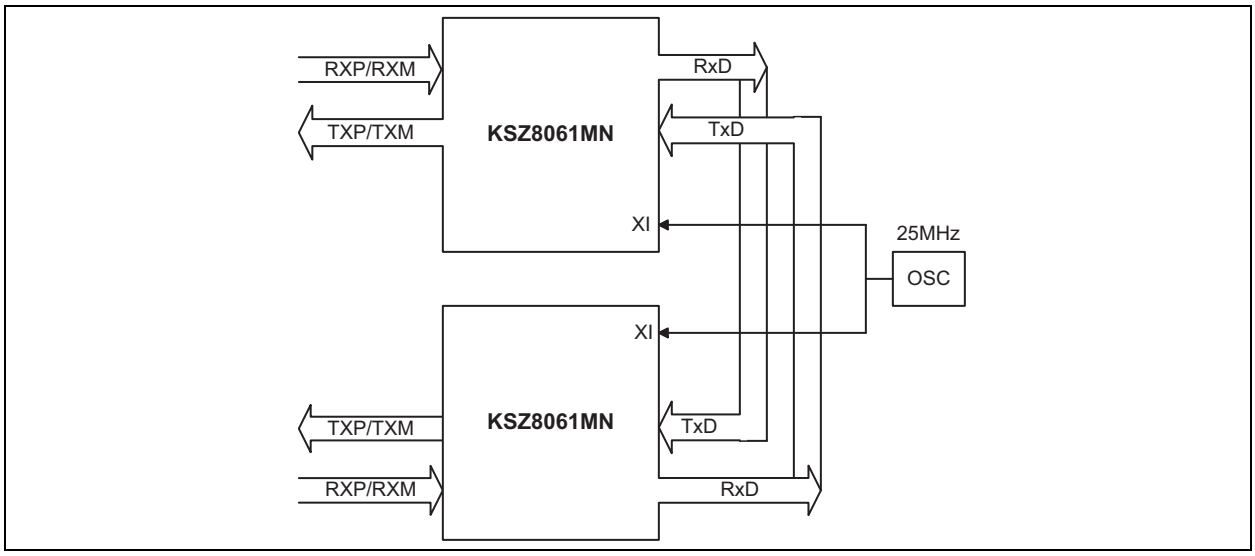
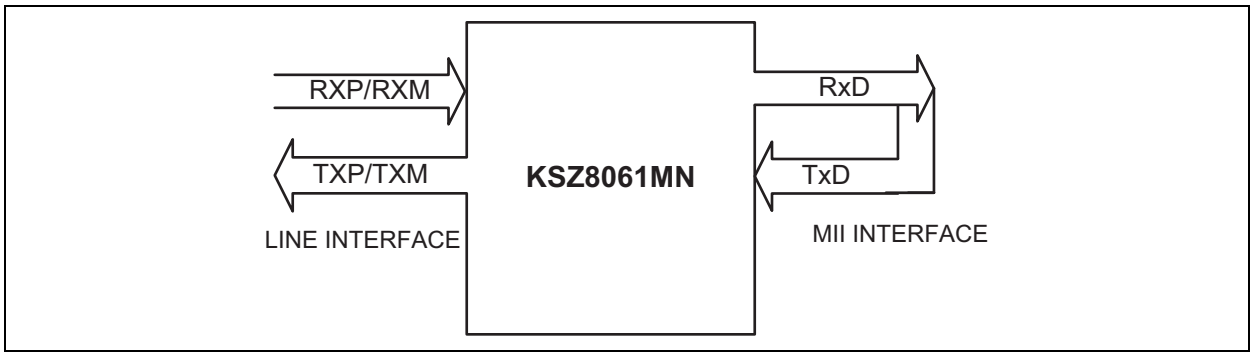


FIGURE 3-4: KSZ8061MN BACK-TO-BACK FOR MII BUS LOOPBACK



3.6.1 MII BACK-TO-BACK MODE

In MII Back-to-Back mode, a KSZ8061MN interfaces with another KSZ8061MN to provide a complete 100 Mbps repeater solution. RXC and TXC are not connected; they are both outputs.

The KSZ8061MN devices are configured to MII Back-to-Back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] set to ‘110’
- A common 25 MHz reference clock connected to XI of both KSZ8061MN devices
- MII signals connected as shown in Table 3-2.

TABLE 3-2: MII SIGNAL CONNECTION FOR MII BACK-TO-BACK MODE

KSZ8061MN (100BASE-TX) [Device 1]		KSZ8061MN (100BASE-TX) [Device 1 or 2]	
Pin Name	**Pin Type**	**Pin Name**	**Pin Type**
RXDV	Output	TXEN	Input
RXD3	Output	TXD3	Input
RXD2	Output	TXD2	Input
RXD1	Output	TXD1	Input
RXD0	Output	TXD0	Input
TXEN	Input	RXDV	Output
TXD3	Input	RXD3	Output
TXD2	Input	RXD2	Output
TXD1	Input	RXD1	Output
TXD0	Input	RXD0	Output

3.6.2 BACK-TO-BACK MODE AND 10BASE-T

If Back-to-Back mode is used and the line interface is operating at 10BASE-T, it is necessary to also set register 18h bit [6].

3.7 MII Management (MIIM) Interface

The KSZ8061MN supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface enables an upper-layer device, like a MAC processor, to monitor and control the state of the KSZ8061MN. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Supported registers [0:8] are standard registers, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See the Register Map section for details.

The KSZ8061MN supports unique PHY addresses 1 to 7, and broadcast PHY address 0. The broadcast address is defined per the IEEE 802.3 specification, and can be used to write to multiple KSZ8061MN devices simultaneously.

The PHYAD[2:0] strapping pins are used to assign a unique PHY address between 0 and 7 to each KSZ8061MN device.

Table 3-3 shows the MII Management frame format.

TABLE 3-3: MII MANAGEMENT FRAME FORMAT

	Preamble	**Start of Frame**	**Read/Write OP Code**	**PHY Address Bits [4:0]**	**REG Address Bits [4:0]**	**TA**	**Data Bits [15:0]**	**Idle**
Read	32 1’s	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1’s	01	10	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.8 LED Output Pins

The LED0 and LED1 pins indicate line status and are intended for driving LEDs. Bits [5:4] in register 1Fh allow the definition of these pins to be changed. The KSZ8061MNX and KSZ8061MNG have different default settings.

On the KSZ8061MNX, the default function for LED0 is Link Status. The KSZ8061MNX does not have an LED1 pin.

On the KSZ8061MNG, the default function for LED0 is Link/Activity and LED1 indicates Link Speed.

- Link Status: The LED indicates that the serial link is up.
- Link/Activity: When the link is up but there is no traffic, the LED will be on. When packets are being received or transmitted, the LED will blink.
- Activity: The LED blinks when packets are received or transmitted. It is off when there is no activity.
- Speed: When the link is up, the LED is on to indicate a 100BASE-TX link, and is off to indicate a 10BASE-T link.

3.9 Interrupt (INTRP)

INTRP is an interrupt output signal that may be used to inform the external controller that there has been a status update to the KSZ8061MN PHY register. This eliminates the need for the processor to poll the PHY for status changes such as link up or down.

Register 1Bh, bits [15:8] are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Register 1Bh, bits [7:0] are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Register 1Fh, bit [9] sets the interrupt level to active high or active low. The default is active low.

3.10 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the KSZ8061MN and its link partner. This feature allows the KSZ8061MN to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and then assigns transmit and receive pairs of the KSZ8061MN accordingly.

Auto MDI/MDI-X is initially either enabled or disabled at a hardware reset by strapping the hardware pin (CONFIG[2:0]). Afterwards, it can be enabled or disabled by register 1Fh, bit [13]. When Auto MDI/MDI-X is disabled, serial data is normally transmitted on the pin pair TXP/TXM, and data is received on RXP/RXM. However, this may be reversed by writing to register 1Fh, bit [14].

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 3-4 illustrates how the IEEE 802.3 Standard defines MDI and MDI-X.

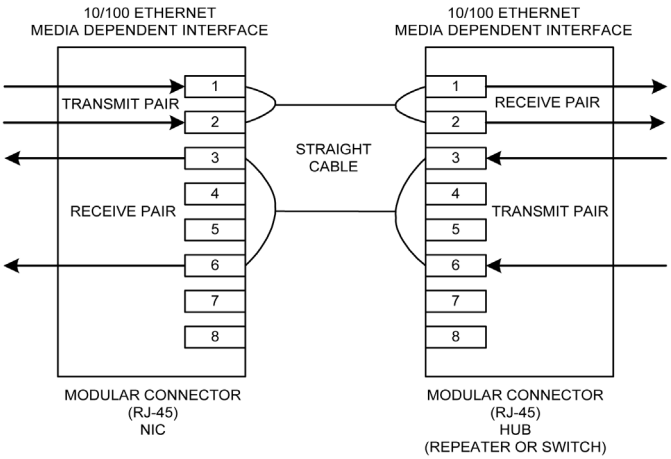
TABLE 3-4: MDI/MDI-X PIN DEFINITION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TX+	1	RX+
2	TX-	2	RX-
3	RX+	3	TX+
6	RX-	6	TX-

3.10.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or a MDI-X device to a MDI device. Table 3-5 depicts a typical straight cable connection between a NIC card (MDI device) and a switch, or hub (MDI-X device).

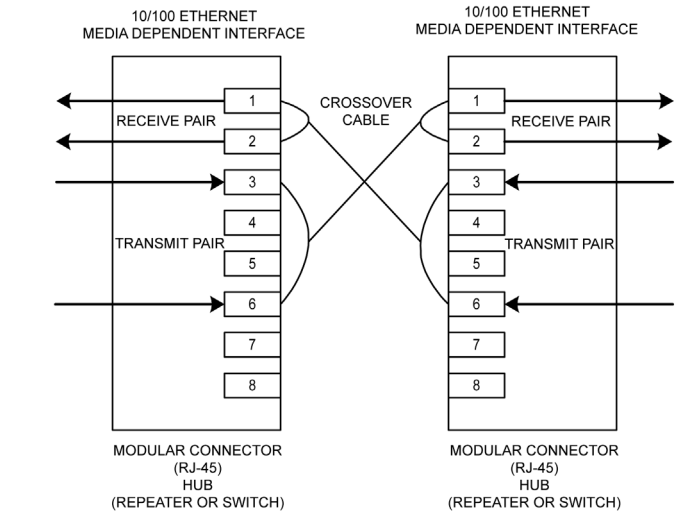
FIGURE 3-5: TYPICAL STRAIGHT CABLE CONNECTION



3.10.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-6 depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-6: TYPICAL CROSSOVER CABLE CONNECTION



3.11 Loopback Modes

The KSZ8061MN supports the following loopback operations to verify analog and/or digital data paths.

- Local (Digital) Loopback
- Remote (Analog) Loopback

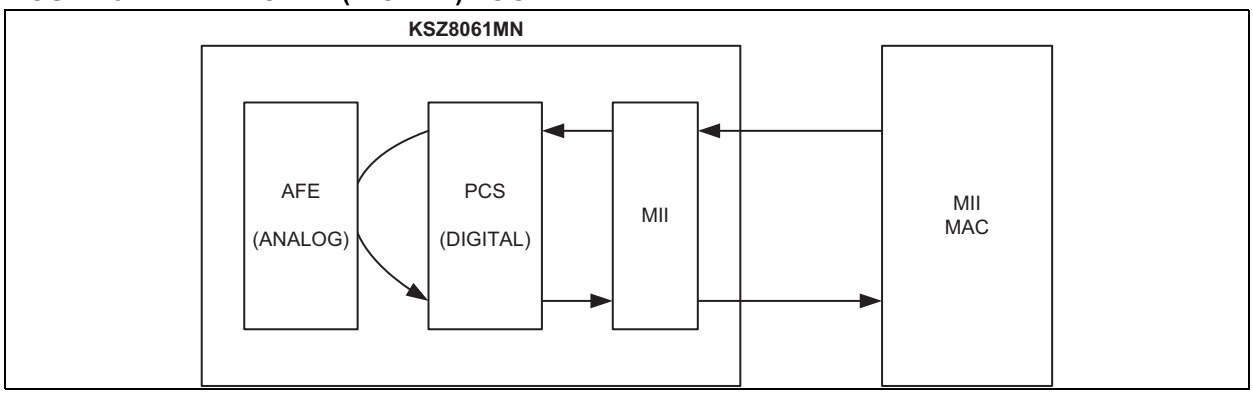
3.11.1 LOCAL (DIGITAL) LOOPBACK MODE

This loopback mode is a diagnostic mode for checking the MII transmit and receive data paths between KSZ8061MN and external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-7.

1. MII MAC transmits frames to KSZ8061MN.
2. Frames are wrapped around inside KSZ8061MN.
3. KSZ8061MN transmits frames back to MII MAC.

FIGURE 3-7: LOCAL (DIGITAL) LOOPBACK



The following programming steps and register settings are used for Local Loopback mode.

For 10/100 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable Local Loopback mode
   - Bit [13] = 0/1 // Select 10 Mbps/100 Mbps speed
   - Bit [12] = 0 // Disable Auto-Negotiation
   - Bit [8] = 1 // Select full-duplex mode
2. Set Register 1Ch,
   - Bit [5] = 1

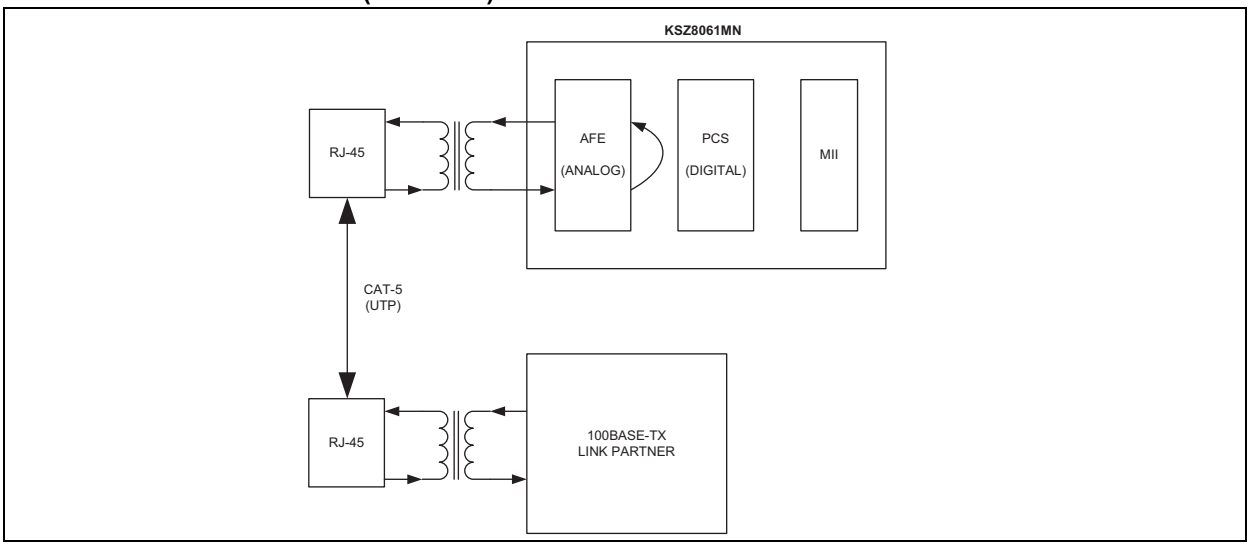
3.11.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ8061MN and its link partner, and is supported for 100BASE-TX full-duplex mode only.

The loopback data path is shown in the following Figure 3-8.

1. Fast Ethernet (100BASE-TX) PHY Link Partner transmits frames to KSZ8061MN.
2. Frames are wrapped around inside KSZ8061MN.
3. KSZ8061MN transmits frames back to Fast Ethernet (100BASE-TX) PHY Link Partner.

FIGURE 3-8: REMOTE (ANALOG) LOOPBACK



The following programming steps and register settings are used for Remote Loopback mode.

1. Set Register 0h,
   - Bit [13] = 1 // Select 100 Mbps speed
   - Bit [12] = 0 // Disable Auto-Negotiation
   - Bit [8] = 1 // Select full-duplex mode

Or just simply auto-negotiate and link up at 100BASE-TX full-duplex mode with link partner

2. Set Register 1Fh,
   - Bit [2] = 1 // Enable Remote Loopback mode

3.12 LinkMD® Cable Diagnostics

The LinkMD® function utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, and then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing the LinkMD Control/Status Register (register 1Dh) and the PHY Control 2 Register (register 1Fh). The latter register is used to disable auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

A two-step process is used to analyze the cable. The first step uses a small pulse (for short cables), while the second step uses a larger pulse (for long cables). The steps are shown here:

For short cables:

1. Write MMD address 1Bh, register 0, bits [7:4] = 0x2. Note that this is the power-up default value.
2. Write register 13h, bit [15] = 0. Note that this is the power-up default value.
3. Write register 1Fh. Disable auto MDI/MDI-X in bit [13], and select either MDI or MDI-X in bit [14] to specify the twisted pair to test.
4. Write register 1Dh bit [15] to initiate the LinkMD test.
5. Read register 1Dh to determine the result of the first step. Bit [15] = 0 indicates that the test is complete. After that, the result is read in bits [14:12]. Remember the result.

For long cables:

1. Write MMD address 1Bh, register 0, bits [7:4] = 0x7.
2. Write register 13h, bit [15] = 1.
3. Write register 1Dh bit [15] to initiate the LinkMD test.
4. Read register 1Dh to determine the result of the first step. Bit [15] = 0 indicates that the test is complete. After that, the result is read in bits [14:12].

If either test reveals a short, then there is a short. If either test reveals an open, then there is an open. If both tests indicate normal, then the cable is normal.

3.13 LinkMD®+ Enhanced Diagnostics: Receive Signal Quality Indicator

The KSZ8061MN provides a receive Signal Quality Indicator (SQI) feature that indicates the relative quality of the 100BASE-TX receive signal. It approximates a signal-to-noise ratio, and is affected by cable length, cable quality, and coupled of environmental noise.

The raw SQI value is available for reading at any time from indirect register: MMD 1Ch, register ACh, bits [14:8]. A lower value indicates better signal quality, while a higher value indicates worse signal quality. Even in a stable configuration in a low-noise environment, the value read from this register may vary. The value should therefore be averaged by taking multiple readings. The update interval of the SQI register is 2 µs, so measurements taken more frequently than 2 µs will be redundant. In a quiet environment, six to ten readings are suggested for averaging. In a noisy environment, individual readings are unreliable, so a minimum of thirty readings are suggested for averaging. The SQI circuit does not include any hysteresis.

Table 3-5 lists typical SQI values for various CAT5 cable lengths when linked to a typical 100BASE-TX device in a quiet environment. In a noisy environment or during immunity testing, the SQI value will increase.

TABLE 3-5: TYPICAL SQI VALUES

CAT5 Cable Length	Typical SQI Value (MMD 1Ch, Register ACh, Bits [14:8]
10m	2
30m	2
50m	3
80m	3
100m	4
130m	5

3.14 NAND Tree Support

The KSZ8061MN provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8061MN digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the CRS pin provides the output for the next NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving low each NAND tree input pin sequentially per the NAND tree pin order
- Checking the NAND tree output to ensure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 3-6 and Table 3-7 list the NAND tree pin order.

TABLE 3-6: KSZ8061MNX NAND TREE TEST PIN ORDER

Pin Number	Pin Name	NAND Tree Description
10	MDIO	Input
11	MDC	Input
12	RXER	Input
13	RXDV	Input
14	RXD3	Input
16	RXD2	Input
17	RXD1	Input
18	RXD0	Input
19	RXC	Input
20	TXC	Input
21	TXEN	Input
22	TXD0	Input
23	TXD1	Input
24	LED0	Input
25	TXD2	Input
26	TXD3	Input
29	INTRP	Input
27	CRS	Output