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KSZ8081MLX

10BASE-T/100BASE-TX Physical Layer Transceiver

Features

- Single-Chip 10BASE-T/100BASE-TX IEEE 802.3 Compliant Ethernet Transceiver
- MII Interface Support
- Back-to-Back Mode Support for a 100 Mbps Copper Repeater
- MDC/MDIO Management Interface for PHY Register Configuration
- Programmable Interrupt Output
- LED Outputs for Link and Activity Status Indication
- On-Chip Termination Resistors for the Differential Pairs
- Baseline Wander Correction
- HP Auto MDI/MDI-X to Reliably Detect and Correct Straight-Through and Crossover Cable Connections with Disable and Enable Option
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100 Mbps) and Duplex (Half/Full)
- Power-Down and Power-Saving Modes
- LinkMD[®] TDR-Based Cable Diagnostics to Identify Faulty Copper Cabling
- Parametric NAND Tree Support for Fault Detection Between Chip I/Os and the Board
- HBM ESD Rating (6 kV)
- Loopback Modes for Diagnostics
- Single 3.3V Power Supply with V_{DD} I/O Options for 1.8V, 2.5V, or 3.3V
- Built-In 1.2V Regulator for Core
- Available in 48-pin 7 mm x 7 mm LQFP Package

Target Applications

- Game Consoles
- IP Phones
- IP Set-Top Boxes
- IP TVs
- LOM
- Printers

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KSZ8081MLX

1.0 INTRODUCTION

1.1 General Description

The KSZ8081MLX is a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

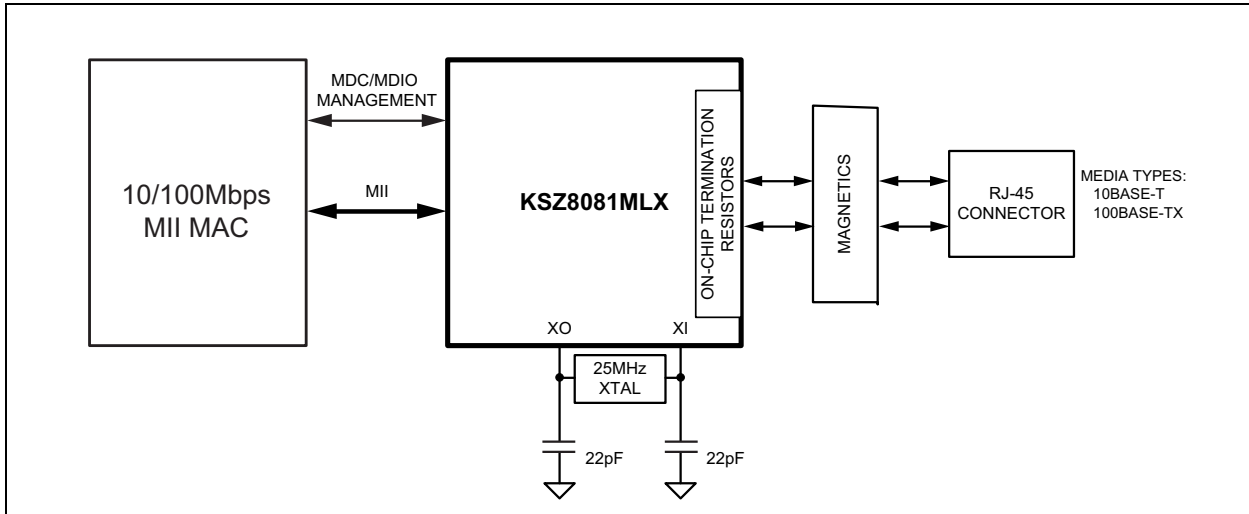
The KSZ8081MLX is a highly-integrated, compact solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs, by integrating a low-noise regulator to supply the 1.2V core, and by offering 1.8/2.5/3.3V digital I/O interface support.

The KSZ8081MLX offers the Media Independent Interface (MII) for direct connection with MII-compliant Ethernet MAC processors and switches.

The KSZ8081MLX provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ8081MLX I/Os and the board. LinkMD[®] TDR-based cable diagnostics identify faulty copper cabling.

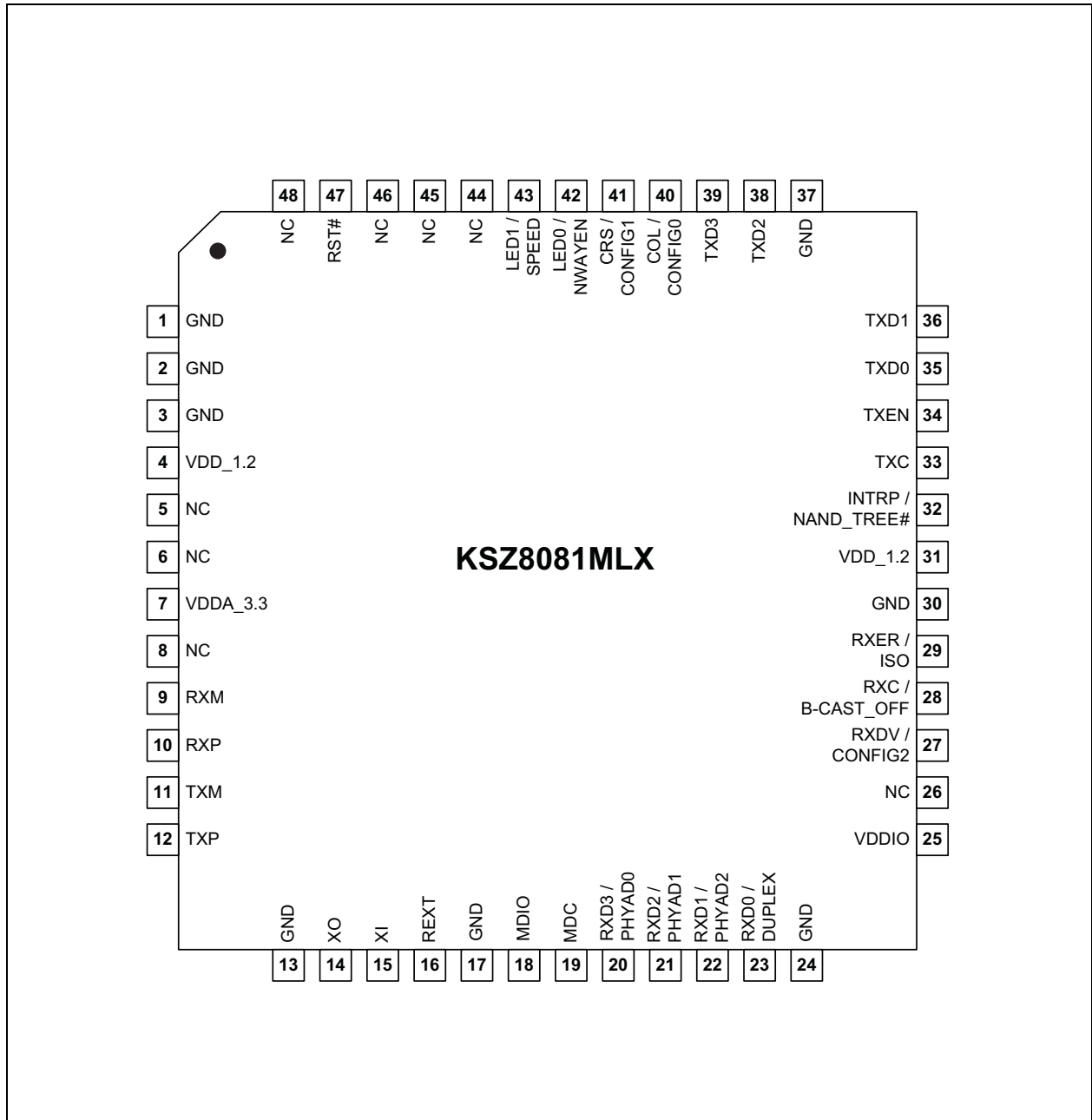
The KSZ8081MLX is available in the 48-pin, lead-free LQFP package.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 48-PIN 7 MM X 7 MM LQFP ASSIGNMENT (TOP VIEW)



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TABLE 2-1: SIGNALS - KSZ8081MLX

Pin Number	Pin Name	Type Note 2-1	Description
1	GND	GND	Ground.
2	GND	GND	Ground.
3	GND	GND	Ground.
4	VDD_!2	P	1.2V Core V _{DD} (power supplied by KSZ8081MLX). Decouple with 2.2 μF and 0.1 μF capacitors to ground, and join with Pin 31 by power trace or plane.
5	NC	—	No Connect. This pin is not bonded and can be left floating.
6	NC	—	No Connect. This pin is not bonded and can be left floating.
7	VDDA_3.3	P	3.3V Analog V _{DD} .
8	NC	—	No Connect. This pin is not bonded and can be left floating.
9	RXM	I/O	Physical Receive or Transmit Signal (– differential).
10	RXP	I/O	Physical Receive or Transmit Signal (+ differential).
11	TXM	I/O	Physical Transmit or Receive Signal (– differential).
12	TXP	I/O	Physical Transmit or Receive Signal (+ differential).
13	GND	GND	Ground.
14	XO	O	Crystal Feedback for 25 MHz Crystal. This pin is a no connect if an oscillator or external clock source is used.
15	XI	I	Crystal/Oscillator/External Clock Input (25 MHz ±50 ppm).
16	REXT	I	Set PHY Transmit Output Current. Connect a 6.49 kΩ resistor to ground on this pin.
17	GND	GND	Ground.
18	MDIO	Ipu/ Opu	Management Interface (MII) Data I/O. This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor.
19	MDC	Ipu	Management Interface (MII) Clock Input. This clock pin is synchronous to the MDIO data pin.
20	RXD3/ PHYAD0	Ipu/O	MII Mode: MII Receive Data Output[3] (Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.
21	RXD2/ PHYAD1	Ipd/O	MII Mode: MII Receive Data Output[2] (Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.
22	RXD1/ PHYAD2	Ipd/O	MII Mode: MII Receive Data Output[1] (Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.

TABLE 2-1: SIGNALS - KSZ8081MLX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
23	RXD0/ DUPLEX	Ipu/O	MII Mode: MII Receive Data Output[0] (Note 2-2) Config. Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.
24	GND	GND	Ground.
25	VDDIO	P	3.3V, 2.5V, or 1.8V Digital V _{DD} .
26	NC	—	No Connect. This pin is not bonded and can be left floating.
27	RXDV/ CONFIG2	Ipd/O	MII Mode: MII Receive Data Valid Output. Config. Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.
28	RXC/ B-CAST_OFF	Ipd/O	MII Mode: MII Receive Clock Output. Config. Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.
29	RXER/ ISO	Ipd/O	MII Mode: MII Receive Error output Config. Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.
30	GND	GND	Ground.
31	VDD_1.2	P	1.2V Core V _{DD} (power supplied by KSZ8081MLX). Decouple with 0.1 µF capacitor to ground, and join with Pin 4 by power trace or plane.
32	INTRP/ NAND_Tree#	Ipu/ Opu	Interrupt Output: Programmable interrupt output. This pin has a weak pull-up, is open drain, and requires an external 1.0 kΩ pull-up resistor. Config. Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.
33	TXC	Ipd/O	MII Mode: MII Transmit Clock Output. At the de-assertion of reset, this pin needs to latch in a pull-down value for normal operation. If MAC side pulls this pin high, see Register 16h, Bit [15] for solution. It is better having an external pull-down resistor to avoid MAC side pulls this pin high.
34	TXEN	I	MII Mode: MII Transmit Enable input.
35	TXD0	I	MII Mode: MII Transmit Data Input[0] (Note 2-3)
36	TXD1	I	MII Mode: MII Transmit Data Input[1] (Note 2-3)
37	GND	GND	Ground.
38	TXD2	I	MII Mode: MII Transmit Data Input[2] (Note 2-3)
39	TXD3	I	MII Mode: MII Transmit Data Input[3] (Note 2-3)

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TABLE 2-1: SIGNALS - KSZ8081MLX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description			
40	COL/ CONFIG0	lpd/O	MII Mode: MII Collision Detect output Config. Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.			
41	CRS/ CONFIG1	lpd/O	MII Mode: MII Carrier Sense Output Config. Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See the Strap-In Options - KSZ8081MLX section for details.			
42	LED0/ NWAYEN	lpu/O	LED Output: Programmable LED0 Output Config. Mode: Latched as auto-negotiation enable (Register 0h, Bit [12]) at the de-assertion of reset. See the Strap-In Options section for details. The LED0 pin is programmable using Register 1Fh Bits [5:4], and is defined as follows:			
			LED Mode = [00]			
			Link/Activity	Pin State	LED Definition	
			No Link	High	OFF	
			Link	Low	ON	
			Activity	Toggle	Blinking	
			LED Mode = [01]			
			Link	Pin State	LED Definition	
			No Link	High	OFF	
			Link	Low	ON	
			LED Mode = [10], [11] Reserved			
			43	LED1/ SPEED	lpu/O	LED Output: Programmable LED1 output Config. Mode: Latched as Speed (Register 0h, Bit [13]) at the de-assertion of reset. See the Strap-In Options section for details. The LED1 pin is programmable using Register 1Fh Bits [5:4], and is defined as follows:
						LED Mode = [00]
Speed	Pin State	LED Definition				
10BASE-T	High	OFF				
100BASE-TX	Low	ON				
LED Mode = [01]						
Activity	Pin State	LED Definition				
No Activity	High	OFF				
Activity	Toggle	Blinking				
LED Mode = [10], [11] Reserved						

TABLE 2-1: SIGNALS - KSZ8081MLX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
44	TEST/NC	lpd	No Connect for normal operation, an external pull-up resistor for NAND tree testing.
45	NC	—	No Connect. This pin is not bonded and can be left floating.
46	NC	—	No Connect. This pin is not bonded and can be left floating.
47	RST#	lpu	Chip Reset (active low).
48	NC	—	No Connect. This pin is not bonded and can be left floating.

Note 2-1 P = power supply
 GND = ground
 I = input
 O = output
 I/O = bi-directional
 lpu = Input with internal pull-up (see [Electrical Characteristics](#) for value).
 lpu/O = Input with internal pull-up (see [Electrical Characteristics](#) for value) during power-up/reset; output pin otherwise.
 lpd/O = Input with internal pull-down (see [Electrical Characteristics](#) for value) during power-up/reset; output pin otherwise.
 lpu/Opu = Input with internal pull-up (see [Electrical Characteristics](#) for value) and output with internal pull-up (see [Electrical Characteristics](#) for value).

Note 2-2 MII RX Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC.

Note 2-3 MII TX Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] presents valid data from the MAC.

2.1 Strap-In Options

The PHYAD[1:0] strap-in pin is latched at the de-assertion of reset. In some systems, the RMII MAC receive input pins may drive high/low during power-up or reset, and consequently cause the PHYAD[1:0] strap-in pin, a shared pin with the RMII CRS_DV signal, to be latched to the unintended high/low state. In this case an external pull-up (4.7 kΩ) or pull-down (1.0 kΩ) should be added on the PHYAD[1:0] strap-in pin to ensure that the intended value is strapped-in correctly.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8081MLX

Pin Number	Pin Name	Type Note 2-4	Description	
22	PHYAD2	lpd/O	The PHY address is latched at de-assertion of reset and is configurable to any value from 0 to 7. The default PHY address is 00001. PHY address 00000 is enabled only if the B-CAST_OFF strap-in pin is pulled high. PHY address Bits [4:3] are set to 00 by default.	
21	PHYAD1			
20	PHYAD0			
27	CONFIG2	lpd/O	The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.	
41	CONFIG1		CONFIG[2:0]	Mode
			000	MI1 (default)
40	CONFIG0		110	MI1 back-to-back
		001 – 101, 111	Reserved, not used	

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TABLE 2-2: STRAP-IN OPTIONS - KSZ8081MLX (CONTINUED)

Pin Number	Pin Name	Type Note 2-4	Description
29	ISO	lpd/O	Isolate Mode: Pull-up = Enable Pull-down (default) = Disable At the de-assertion of reset, this pin value is latched into Register 0h, Bit [10].
43	SPEED	lpu/O	Speed Mode: Pull-up (default) = 100 Mbps Pull-down = 10 Mbps At the de-assertion of reset, this pin value is latched into Register 0h, Bit [13] as the speed select, and also is latched into Register 4h (auto-negotiation advertisement) as the speed capability support.
23	DUPLEX	lpu/O	Duplex Mode: Pull-up (default) = Half-duplex Pull-down = Full-duplex At the de-assertion of reset, this pin value is latched into Register 0h, Bit [8].
42	NWAYEN	lpu/O	Nway Auto-Negotiation Enable: Pull-up (default) = Enable auto-negotiation Pull-down = Disable auto-negotiation At the de-assertion of reset, this pin value is latched into Register 0h, Bit [12].
28	B-CAST_OFF	lpd/O	Broadcast Off – for PHY Address 0: Pull-up = PHY Address 0 is set as an unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
32	NAND_Tree#	lpu/Opu	NAND Tree Mode: Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Note 2-4 lpu/O = Input with internal pull-up (see [Electrical Characteristics](#) for value) during power-up/reset; output pin otherwise.
 lpd/O = Input with internal pull-down (see [Electrical Characteristics](#) for value) during power-up/reset; output pin otherwise.
 lpu/Opu = Input with internal pull-up (see [Electrical Characteristics](#) for value) and output with internal pull-up (see [Electrical Characteristics](#) for value).

3.0 FUNCTIONAL DESCRIPTION

The KSZ8081MLX is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8081MLX supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8081MLX offers the Media Independent Interface (MII) for direct connection with MII compliant Ethernet MAC processors and switches.

The MII management bus option gives the MAC processor complete access to the KSZ8081MLX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

3.1 10BASE-T/100BASE-TX Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49 k Ω 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10BASE-T signals with typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV, or with short pulse widths, to prevent

KSZ8081MLX

noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8081MLX decodes a data frame. The receive clock is kept active during idle periods between data receptions.

3.1.6 SQE AND JABBER FUNCTION (10BASE-T ONLY)

In 10BASE-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE test is needed to test the 10BASE-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10BASE-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10BASE-T transmitter is re-enabled and COL is de-asserted (returns to low).

3.1.7 PLL CLOCK SYNTHESIZER

The KSZ8081MLX generates all internal clocks and all external clocks for system timing from an external 25 MHz crystal, oscillator, or reference clock.

3.1.8 AUTO-NEGOTIATION

The KSZ8081MLX conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

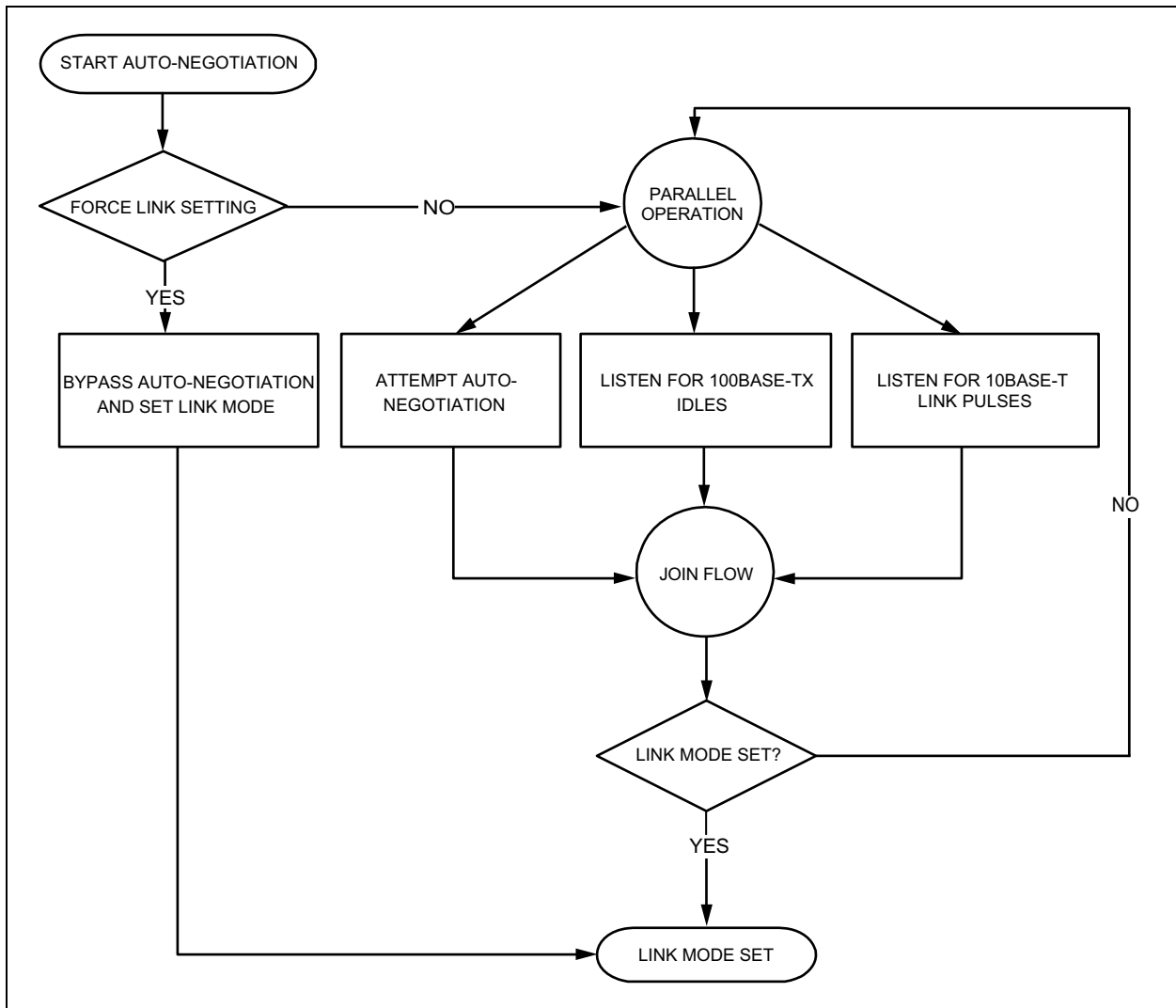
If auto-negotiation is not supported or the KSZ8081MLX link partner is forced to bypass auto-negotiation, then the KSZ8081MLX sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8081MLX to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (NWAYEN, Pin 42) or software (Register 0h, Bit [12]).

By default, auto-negotiation is enabled after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled by Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bit [13], and the duplex is set by Register 0h, Bit [8].

The auto-negotiation link-up process is shown in [Figure 3-1](#).

FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART



3.2 MII Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 15 pins (6 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4 bits wide, a nibble.

By default, the KSZ8081MLX is configured to MII mode after it is powered up or hardware reset with the following:

- A 25 MHz crystal connected to XI, XO (Pins 15, 14), or an external 25 MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (Pins 27, 41, 40) set to 000 (default setting).

3.2.1 MII SIGNAL DEFINITION

[Table 3-1](#) describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

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TABLE 3-1: MII SIGNAL DEFINITION

MII Signal Name	Direction with Respect to PHY, KSZ8081 Signal	Direction with Respect to MAC	Description
TXC	Output	Input	Transmit Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data[3:0]
RXC	Output	Input	Receive Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data[3:0]
RXER	Output	Input or not required	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

3.2.1.1 Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.2.1.2 Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII. It is negated before the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

3.2.1.3 Transmit Data[3:0] (TXD[3:0])

When TXEN is asserted, TXD[3:0] are the data nibbles accepted by the PHY for transmission. TXD[3:0] is 00 to indicate idle when TXEN is de-asserted.

TXD[3:0] transitions synchronously with respect to TXC.

3.2.1.4 Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

In 10 Mbps mode, RXC is recovered from the line while the carrier is active. RXC is derived from the PHY's reference clock when the line is idle or the link is down.

In 100 Mbps mode, RXC is continuously recovered from the line. If the link is down, RXC is derived from the PHY's reference clock.

RXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.2.1.5 Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

In 10 Mbps mode, RXDV is asserted with the first nibble of the start-of-frame delimiter (SFD), 5D, and remains asserted until the end of the frame.

In 100 Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

3.2.1.6 Receive Data[3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

3.2.1.7 Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to RXC.

3.2.1.8 Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

In 10 Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.

In 100 Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

3.2.1.9 Collision Detection (COL)

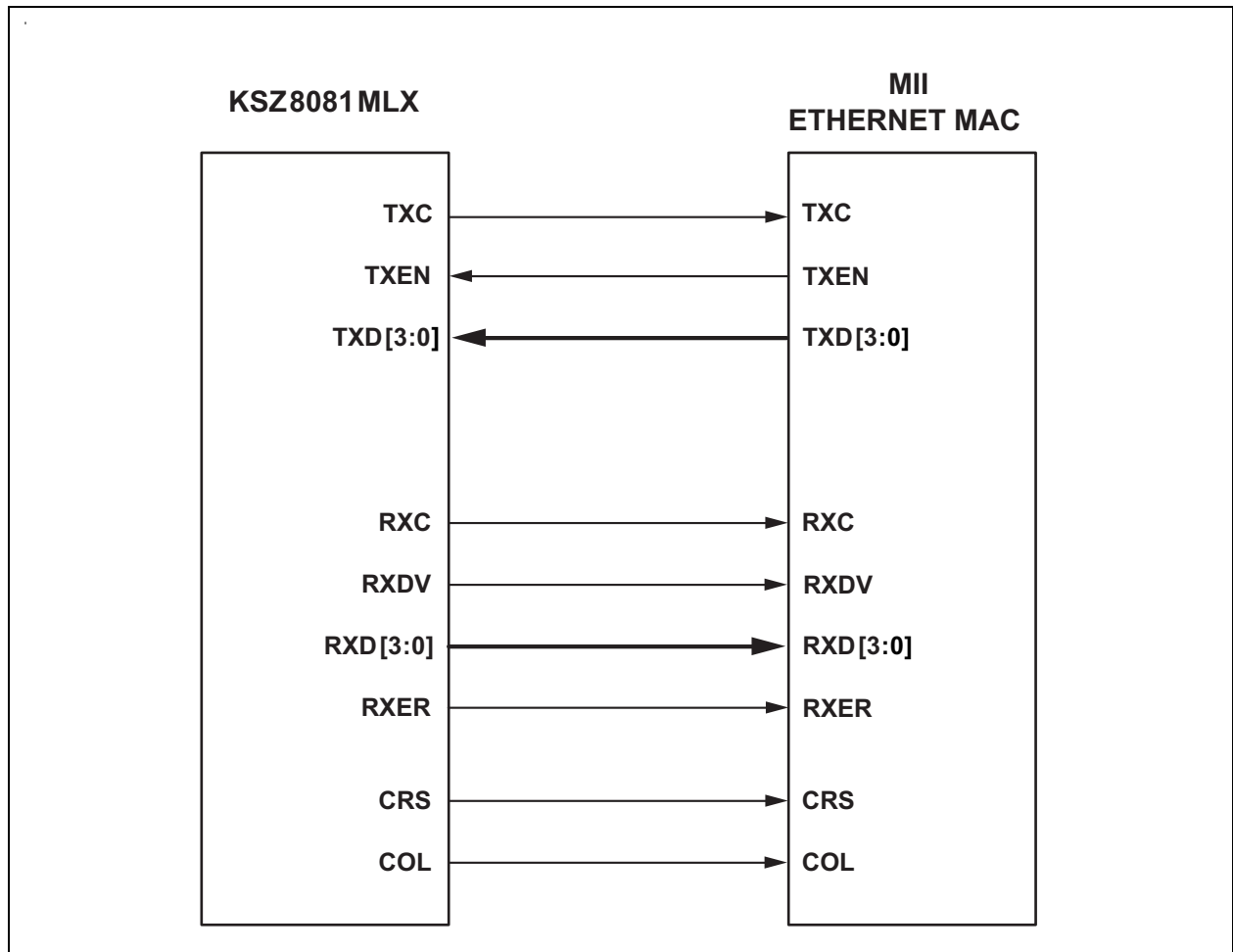
COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This informs the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

3.2.2 MII SIGNAL DIAGRAM

The KSZ8081MLX MII pin connections to the MAC are shown in [Figure 3-2](#).

FIGURE 3-2: KSZ8081MLX MII INTERFACE

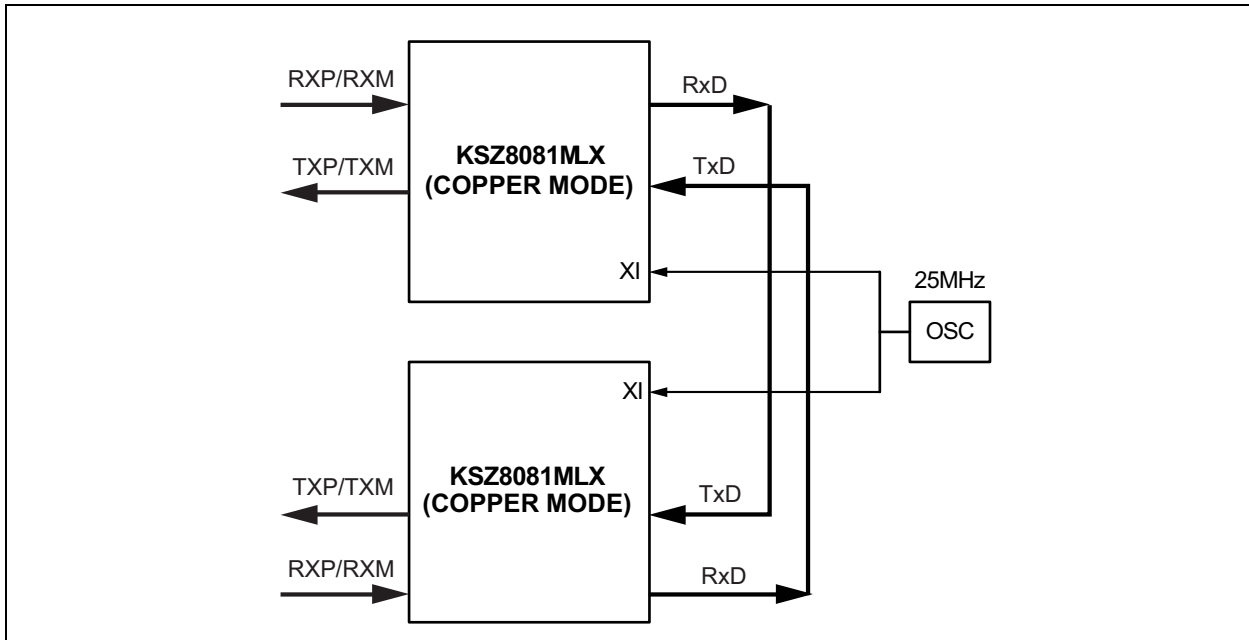


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3.3 Back-to-Back Mode – 100 Mbps Copper Repeater

Two KSZ8081MLX devices can be connected back-to-back to form a 100BASE-TX to 100BASE-TX copper repeater.

FIGURE 3-3: KSZ8081MLX TO KSZ8081MLX BACK-TO-BACK COPPER REPEATER



3.3.1 MII BACK-TO-BACK MODE

In MII back-to-back mode, a KSZ8081MLX interfaces with another KSZ8081MLX to provide a complete 100 Mbps copper repeater solution.

The KSZ8081MLX devices are configured to MII back-to-back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] (Pins 27, 41, 40) set to 110.
- A common 25 MHz reference clock connected to XI (Pin 15) of both KSZ8081MLX devices.
- MII signals connected as shown in [Table 3-2](#).

TABLE 3-2: MII SIGNAL CONNECTION FOR MII BACK-TO-BACK MODE (100BASE-TX COPPER REPEATER)

KSZ8081MLX (100BASE-TX Copper) [Device 1]			KSZ8081MLX (100BASE-TX Copper) [Device 2]		
Pin Name	Pin Number	Pin Type	Pin Name	Pin Number	Pin Type
RXDV	27	Output	TXEN	34	Input
RXD3	20	Output	TXD3	39	Input
RXD2	21	Output	TXD2	38	Input
RXD1	22	Output	TXD1	36	Input
RXD0	23	Output	TXD0	35	Input
TXEN	34	Input	RXDV	27	Output
TXD3	39	Input	RXD3	20	Output
TXD2	38	Input	RXD2	21	Output
TXD1	36	Input	RXD1	22	Output
TXD0	35	Input	RXD0	23	Output

3.4 MII Management (MIIM) Interface

The KSZ8081MLX supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8081MLX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Registers [0:8] are standard registers, and their functions are defined in the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See the Register Map section for details.

As the default, the KSZ8081MLX supports unique PHY addresses 1 to 7, and broadcast PHY address 0. The latter is defined in the IEEE 802.3 Specification, and can be used to read/write to a single KSZ8081MLX device, or write to multiple KSZ8081MLX devices simultaneously.

PHY address 0 can optionally be disabled as the broadcast address by either hardware pin strapping (B-CAST_OFF, Pin 28) or software (Register 16h, Bit [9]), and assigned as a unique PHY address.

The PHYAD[2:0] strapping pins are used to assign a unique PHY address between 0 and 7 to each KSZ8081MLX device.

The MIIM interface can operate up to a maximum clock speed of 10 MHz MAC clock.

Table 3-3 shows the MII management frame format for the KSZ8081MLX.

TABLE 3-3: MII MANAGEMENT FRAME FORMAT FOR THE KSZ8081MLX

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	000AA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	000AA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.5 Interrupt (INTRP)

INTRP (Pin 32) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8081MLX PHY Register. Bits [15:8] of Register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of Register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [9] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8081MLX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

3.6 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8081MLX and its link partner. This feature allows the KSZ8081MLX to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs of the KSZ8081MLX accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a '1' to Register 1Fh, Bit [13]. MDI and MDI-X mode is selected by Register 1Fh, Bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 3-4 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

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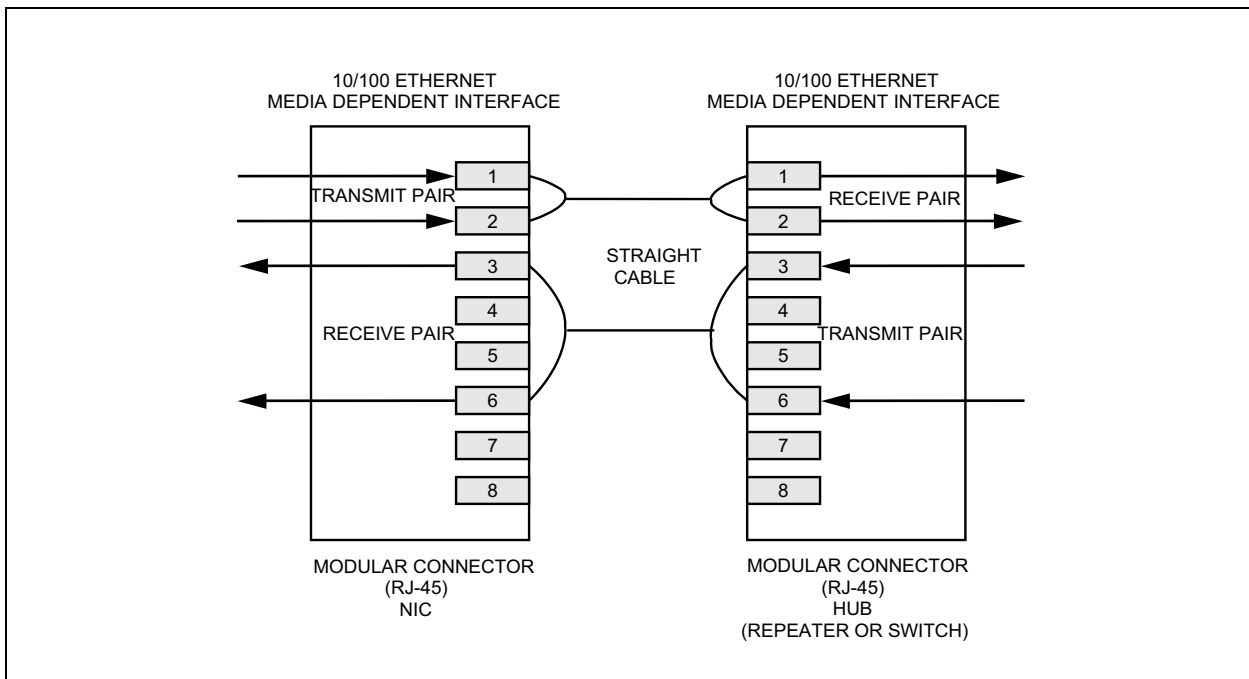
TABLE 3-4: MDI/MDI-X PIN DESCRIPTION

MDI		MDI-X	
RJ-45 Pin	Signal	RJ-45 Pin	Signal
1	TX+	1	RX+
2	TX-	2	RX-
3	RX+	3	TX+
6	RX-	6	TX-

3.6.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. [Figure 3-4](#) shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).

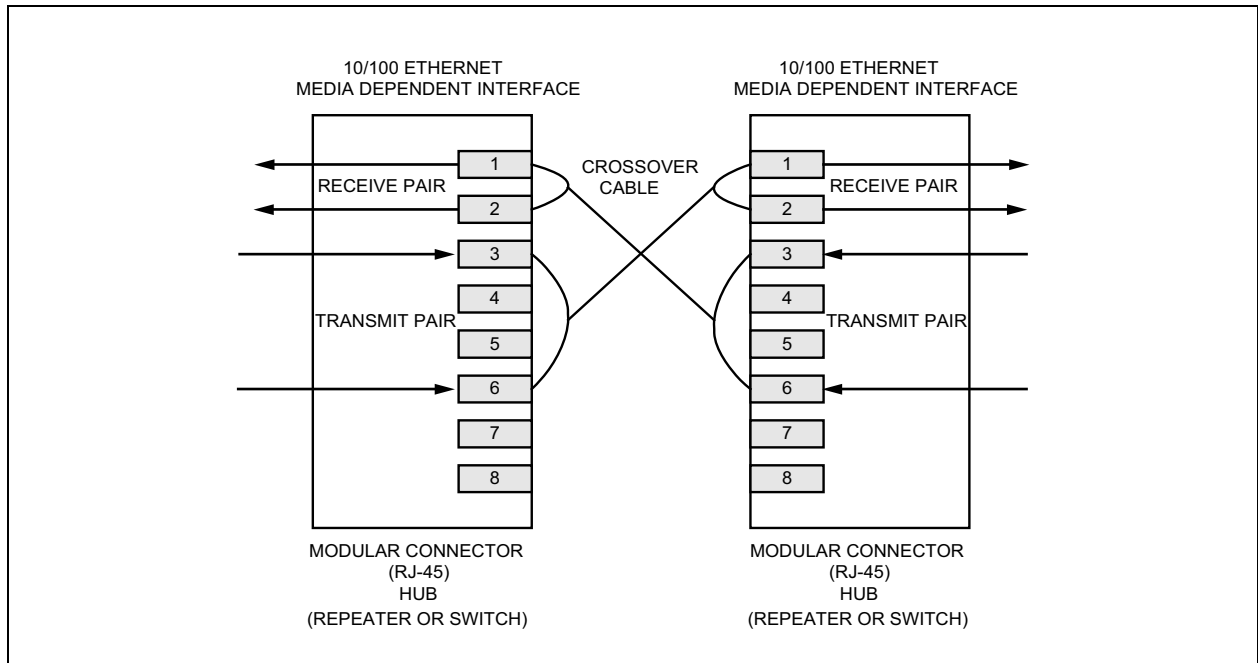
FIGURE 3-4: TYPICAL STRAIGHT CABLE CONNECTION



3.6.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. [Figure 3-5](#) shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-5: TYPICAL CROSSOVER CABLE CONNECTION



3.7 Loopback Mode

The KSZ8081MLX supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

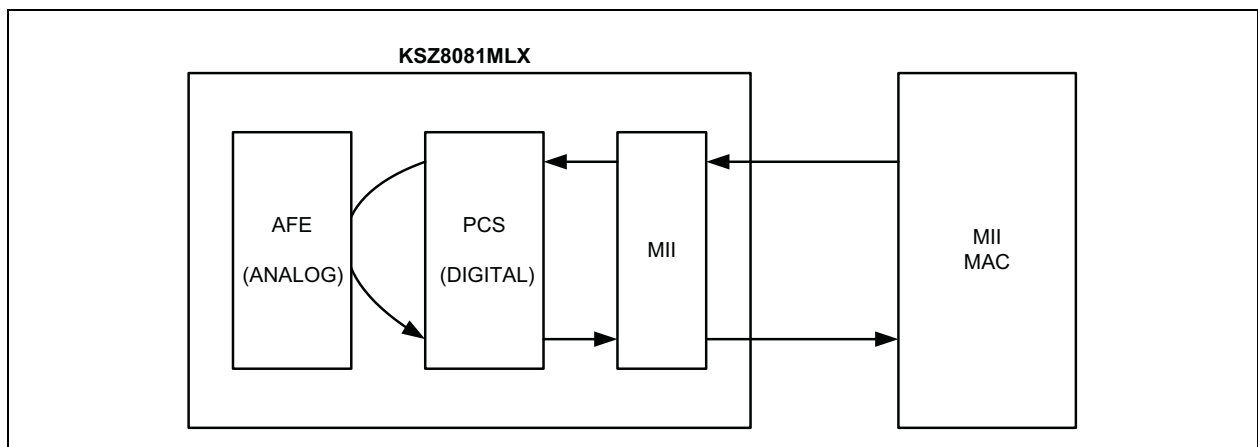
3.7.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the MII transmit and receive data paths between the KSZ8081MLX and the external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in [Figure 3-6](#).

1. The MII MAC transmits frames to the KSZ8081MLX.
2. Frames are wrapped around inside the KSZ8081MLX.
3. The KSZ8081MLX transmits frames back to the MII MAC.

FIGURE 3-6: LOCAL (DIGITAL) LOOPBACK



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The following programming action and register settings are used for local loopback mode:

For 10/100 Mbps loopback:

Set Register 0h,

Bit [14] = 1 // Enable local loopback mode

Bit [13] = 0/1 // Select 10 Mbps/100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

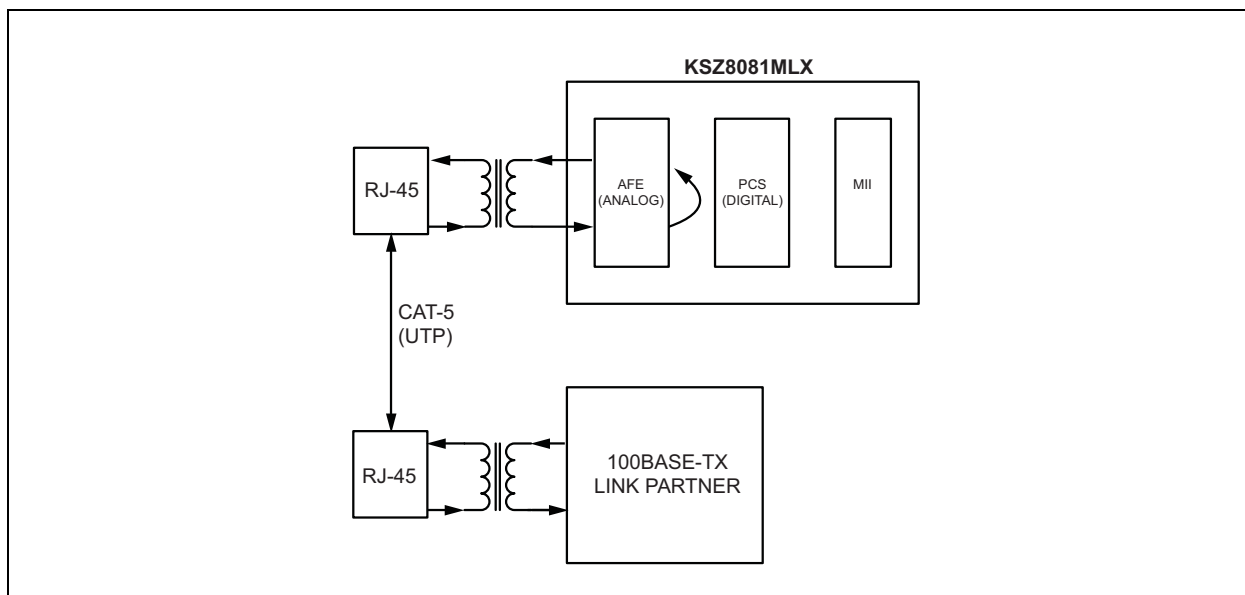
3.7.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8081MLX and its link partner, and is supported for 100BASE-TX full-duplex mode only.

The loopback data path is shown in [Figure 3-7](#).

1. The Fast Ethernet (100BASE-TX) PHY link partner transmits frames to the KSZ8081MLX.
2. Frames are wrapped around inside the KSZ8081MLX.
3. The KSZ8081MLX transmits frames back to the Fast Ethernet (100BASE-TX) PHY link partner.

FIGURE 3-7: REMOTE (ANALOG) LOOPBACK



The following programming steps and register settings are used for remote loopback mode:

1. Set Register 0h,

Bits [13] = 1 // Select 100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

Or just auto-negotiate and link up at 100BASE-TX full-duplex mode with the link partner.

2. Set Register 1Fh,

Bit [2] = 1 // Enable remote loopback mode

3.8 LinkMD[®] Cable Diagnostic

The LinkMD function uses time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems. These include open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing Register 1Dh, the LinkMD Control/Status register, in conjunction with Register 1Fh, the PHY Control 2 register. The latter register is used to disable Auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

3.8.1 USAGE

The following is a sample procedure for using LinkMD with Registers 1Dh and 1Fh:

1. Disable auto MDI/MDI-X by writing a '1' to Register 1Fh, bit [13].
2. Start cable diagnostic test by writing a '1' to Register 1Dh, bit [15]. This enable bit is self-clearing.
3. Wait (poll) for Register 1Dh, bit [15] to return a '0', and indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 1Dh, bits [14:13]. The results are as follows:
 - 00 = normal condition (valid test)
 - 01 = open condition detected in cable (valid test)
 - 10 = short condition detected in cable (valid test)
 - 11 = cable diagnostic test failed (invalid test)

The '11' case, invalid test, occurs when the device is unable to shut down the link partner. In this instance, the test is not run because it would be impossible for the device to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating Register 1Dh, bits [8:0] and multiplying the result by a constant of 0.38. The distance to the cable fault can be determined by the following formula:

EQUATION 3-1:

$$D(\text{Distance to cable fault in meters}) = 0.38 \times (\text{Register 1Dh, bits}[8:0])$$

Concatenated value of Registers 1Dh bits [8:0] should be converted to decimal before multiplying by 0.38.

The constant (0.38) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.9 NAND Tree Support

The KSZ8081MLX provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8081MLX digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the CRS/CONFIG1 pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving each NAND tree input pin low, sequentially, according to the NAND tree pin order
- Checking the NAND tree output to make sure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 3-5 lists the NAND tree pin order.

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TABLE 3-5: NAND TREE TEST PIN ORDER FOR KSZ8081MLX

Pin Number	Pin Name	NAND Tree Description
18	MDIO	Input
19	MDC	Input
20	RXD3	Input
21	RXD2	Input
22	RXD1	Input
23	RXD0	Input
27	RXDV	Input
28	RXC	Input
29	RXER	Input
32	INTRP	Input
33	TXC	Input
34	TXEN	Input
35	TXD0	Input
36	TXD1	Input
38	TXD2	Input
39	TXD3	Input
42	LED0	Input
43	LED1	Input
40	COL	Input
41	CRS	Output

3.9.1 NAND TREE I/O TESTING

Use the following procedure to check for faults on the KSZ8081MLX digital I/O pin connections to the board:

1. Enable NAND tree mode using either a hardware strap-in pin (NAND_Tree#, Pin 32) or software (Register 16h, Bit [5]). Pin 44 TEST/NC has to use a pull-up resistor for normal NAND tree testing.
2. Use board logic to drive all KSZ8081MLX NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, in KSZ8081MLX NAND tree pin order, as follows:
 - a) Toggle the first pin (MDIO) from high to low, and verify that the CRS/CONFIG1 pin switches from high to low to indicate that the first pin is connected properly.
 - b) Leave the first pin (MDIO) low.
 - c) Toggle the second pin (MDC) from high to low, and verify that the CRS/CONFIG1 pin switches from low to high to indicate that the second pin is connected properly.
 - d) Leave the first pin (MDIO) and the second pin (MDC) low.
 - e) Toggle the third pin from high to low, and verify that the CRS/CONFIG1 pin switches from high-to-low to indicate that the third pin is connected properly.
 - f) Continue with this sequence until all KSZ8081MLX NAND tree input pins have been toggled.

Each KSZ8081MLX NAND tree input pin must cause the CRS/CONFIG1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the CRS pin fails to toggle when the KSZ8081MLX input pin toggles from high to low, the input pin has a fault.

3.10 Power Management

The KSZ8081MLX incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

3.10.1 POWER-SAVING MODE

Power-saving mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a '1' to Register 1Fh, Bit [10], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ8081MLX shuts down all transceiver blocks, except for the transmitter, energy detect, and PLL circuits.

By default, power-saving mode is disabled after power-up.

3.10.2 ENERGY-DETECT POWER-DOWN MODE

Energy-detect power-down (EDPD) mode is used to further reduce transceiver power consumption when the cable is unplugged. It is enabled by writing a '0' to Register 18h, Bit [11], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

EDPD mode works with the PLL off (set by writing a '1' to Register 10h, Bit [4] to automatically turn the PLL off in EDPD mode) to turn off all KSZ8081MLX transceiver blocks, except for the transmitter and energy-detect circuits.

Power can be reduced further by extending the time interval between transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure two link partners in the same low-power state, with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them.

By default, energy-detect power-down mode is disabled after power-up.

3.10.3 POWER-DOWN MODE

Power-down mode is used to power down the KSZ8081MLX device when it is not in use after power-up. It is enabled by writing a '1' to Register 0h, Bit [11].

In this mode, the KSZ8081MLX disables all internal functions except the MII management interface. The KSZ8081MLX exits (disables) power-down mode after Register 0h, Bit [11] is set back to '0'.

3.10.4 SLOW-OSCILLATOR MODE

Slow-oscillator mode is used to disconnect the input reference crystal/clock on XI (Pin 15) and select the on-chip slow oscillator when the KSZ8081MLX device is not in use after power-up. It is enabled by writing a '1' to Register 11h, Bit [5].

Slow-oscillator mode works in conjunction with power-down mode to put the KSZ8081MLX device in the lowest power state with all internal functions disabled except the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable slow-oscillator mode by writing a '0' to Register 11h, Bit [5].
2. Disable power-down mode by writing a '0' to Register 0h, Bit [11].
3. Initiate software reset by writing a '1' to Register 0h, Bit [15].

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3.11 Reference Circuit for Power and Ground Connections

The KSZ8081MLX is a single 3.3V supply device with a built-in regulator to supply the 1.2V core. The power and ground connections are shown in Figure 3-8 and Table 3-6 for 3.3V V_{DDIO} .

FIGURE 3-8: KSZ8081MLX POWER AND GROUND CONNECTIONS

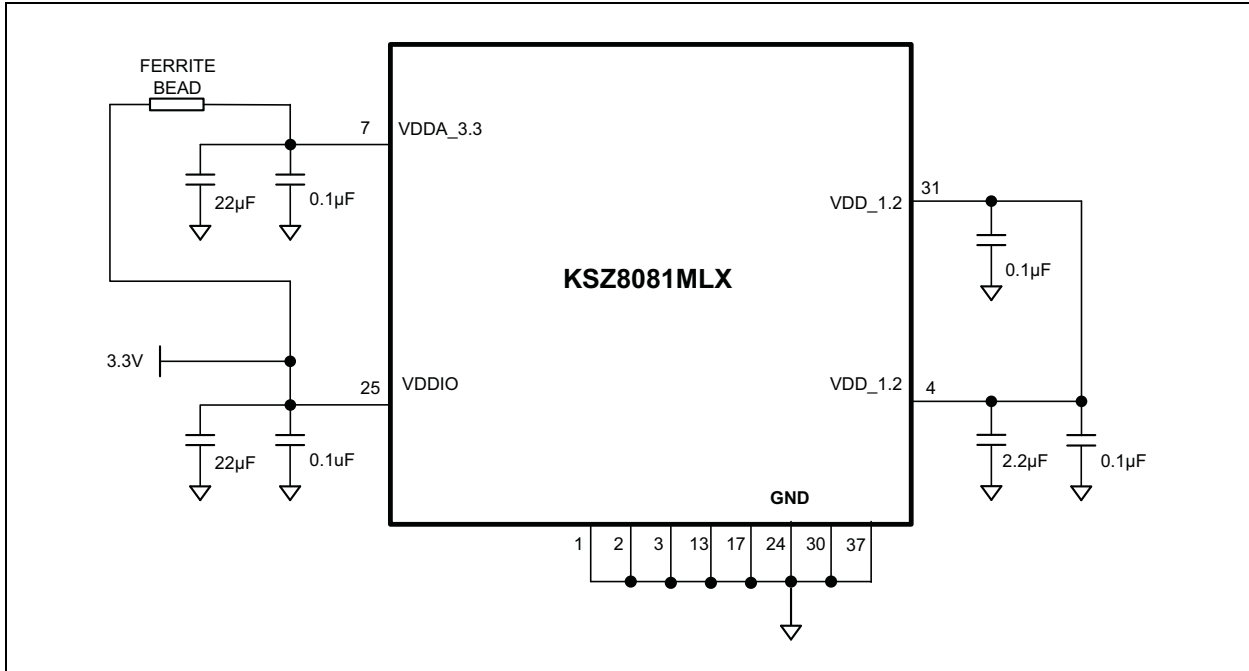


TABLE 3-6: KSZ8081MLX POWER PIN DESCRIPTION

Power Pin	Pin Number	Description
VDD_1.2	4	Connect with Pin 31 by power trace or plane. Decouple with 2.2 μ F and 0.1 μ F capacitors to ground.
VDDA_3.3	7	Connect to board's 3.3V supply through a ferrite bead. Decouple with 22 μ F and 0.1 μ F capacitors to ground.
VDDIO	25	Connect to board's 3.3V supply for 3.3V V_{DDIO} . Decouple with 22 μ F and 0.1 μ F capacitors to ground.
VDD_1.2	31	Connect with Pin 4 by power trace or plane. Decouple with 0.1 μ F capacitor to ground.

3.12 Typical Current/Power Consumption

Table 3-7, Table 3-8, and Table 3-9 show typical values for current consumption by the transceiver ($V_{DDA_3.3}$) and digital I/O (V_{DDIO}) power pins and typical values for power consumption by the KSZ8081MLX device for the indicated nominal operating voltages. These current and power consumption values include the transmit driver current and on-chip regulator current for the 1.2V core.

TABLE 3-7: TYPICAL CURRENT/POWER CONSUMPTION ($V_{DDA_3.3} = 3.3V$, $V_{DDIO} = 3.3V$)

Condition	3.3V Transceiver ($V_{DDA_3.3}$)	3.3V Digital I/Os (V_{DDIO})	Total Chip Power
100BASE-TX Link-up (no traffic)	34 mA	12 mA	152 mW
100BASE-TX Full-duplex @ 100% utilization	34 mA	13 mA	155 mW
10BASE-T Link-up (no traffic)	14 mA	11 mA	82.5 mW
10BASE-T Full-duplex @ 100% utilization	30 mA	11 mA	135 mW

TABLE 3-7: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 3.3V)

Condition	3.3V Transceiver (VDDA_3.3)	3.3V Digital I/Os (VDDIO)	Total Chip Power
Power-saving mode (Reg. 1Fh, Bit [10] = 1)	14 mA	10 mA	79.2 mW
EDPD mode (Reg. 18h, Bit [11] = 0)	10 mA	10 mA	66 mW
EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1)	3.77 mA	1.54 mA	1.75 mW
Software power-down mode (Reg. 0h, Bit [11] = 1)	2.59 mA	1.51 mA	13.5 mW
Software power-down mode (Reg. 0h, Bit [11] = 1) and slow-oscillator mode (Reg. 11h, Bit [5] = 1)	1.36 mA	0.45 mA	5.97 mW

TABLE 3-8: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 2.5V)

Condition	3.3V Transceiver (VDDA_3.3)	2.5V Digital I/Os (VDDIO)	Total Chip Power
100BASE-TX Link-up (no traffic)	34 mA	11 mA	140 mW
100BASE-TX Full-duplex @ 100% utilization	34 mA	12 mA	142 mW
10BASE-T Link-up (no traffic)	15 mA	10 mA	74.5 mW
10BASE-T Full-duplex @ 100% utilization	27 mA	10 mA	114 mW
Power-saving mode (Reg. 1Fh, Bit [10] = 1)	15 mA	10 mA	74.5 mW
EDPD mode (Reg. 18h, Bit [11] = 0)	11 mA	10 mA	61.3 mW
EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1)	3.55 mA	1.35 mA	15.1 mW
Software power-down mode (Reg. 0h, Bit [11] = 1)	2.29 mA	1.34 mA	10.9 mW
Software power-down mode (Reg. 0h, Bit [11] = 1) and slow-oscillator mode (Reg. 11h, Bit [5] = 1)	1.15 mA	0.29 mA	4.52 mW

TABLE 3-9: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 1.8V)

Condition	3.3V Transceiver (VDDA_3.3)	1.8V Digital I/Os (VDDIO)	Total Chip Power
100BASE-TX Link-up (no traffic)	34 mA	11 mA	132 mW
100BASE-TX Full-duplex @ 100% utilization	34 mA	12 mA	134 mW
10BASE-T Link-up (no traffic)	15 mA	9 mA	65.7 mW
10BASE-T Full-duplex @ 100% utilization	27 mA	9 mA	105 mW
Power-saving mode (Reg. 1Fh, Bit [10] = 1)	15 mA	9 mA	65.7 mW
EDPD mode (Reg. 18h, Bit [11] = 0)	11 mA	9 mA	52.5 mW
EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1)	4.05 mA	1.21 mA	15.5 mW
Software power-down mode (Reg. 0h, Bit [11] = 1)	2.79 mA	1.21 mA	11.4 mW
Software power-down mode (Reg. 0h, Bit [11] = 1) and slow-oscillator mode (Reg. 11h, Bit [5] = 1)	1.65 mA	0.19 mA	5.79 mW