Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

KSZ8081MNX/RNB

10BASE-T/100BASE-TX Physical Layer Transceiver

Features

- Single-chip 10Base-T/100Base-TX IEEE 802.3 compliant Ethernet transceiver
- MII interface support (KSZ8081MNX)
- RMII v1.2 Interface support with a 50 MHz reference clock output to MAC, and an option to input a 50 MHz reference clock (KSZ8081RNB)
- Back-to-back mode support for a 100 Mbps copper repeater
- MDC/MDIO management interface for PHY register configuration
- Programmable interrupt output
- LED outputs for link, activity, and speed status indication
- On-chip termination resistors for the differential pairs
- Baseline wander correction
- HP Auto MDI/MDI-X to reliably detect and correct straight-through and crossover cable connections with disable and enable option
- Auto-negotiation to automatically select the highest link-up speed (10/100 Mbps) and duplex (half/full)
- Power-down and power-saving modes
- LinkMD TDR-based cable diagnostics to identify faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and the board
- HBM ESD rating (6 kV)
- Loopback modes for diagnostics
- Single 3.3V power supply with VDD I/O options for 1.8V, 2.5V, or 3.3V
- Built-in 1.2V regulator for core
- Available in 32-pin (5 mm × 5 mm) QFN package

Applications

- Game console
- IP phone
- IP set-top box
- IP TV
- LOM
- Printer

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8081 is a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081 is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core.

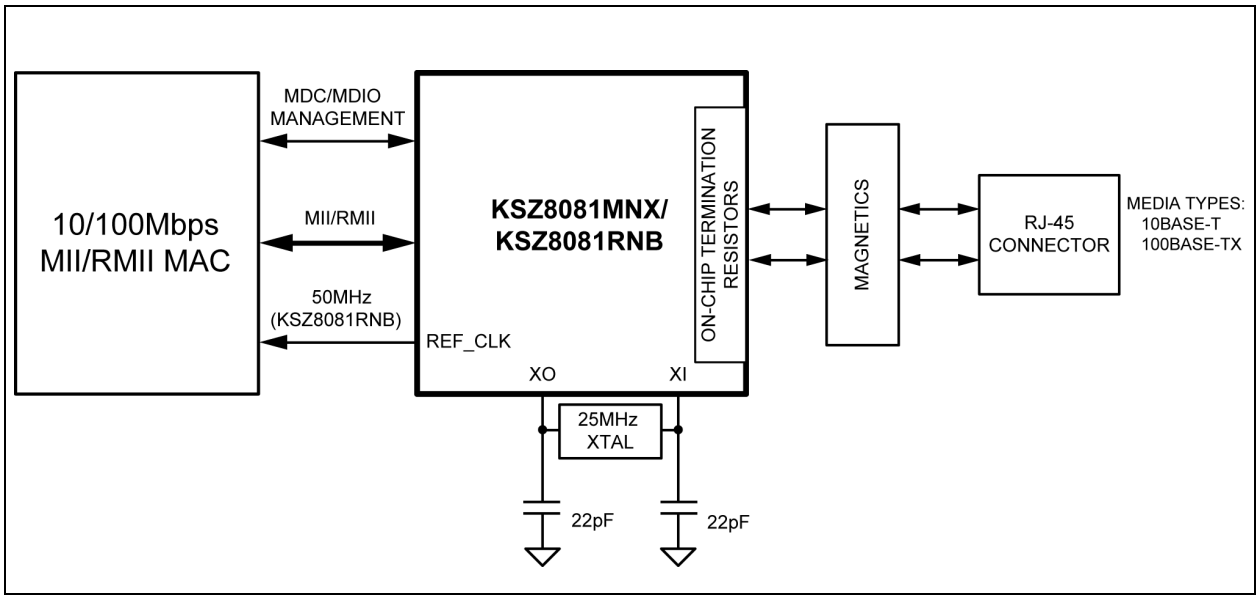
The KSZ8081MNX offers the Media Independent Interface (MII) and the KSZ8081RNB offers the Reduced Media Independent Interface (RMII) for direct connection with MII/RMII-compliant Ethernet MAC processors and switches.

A 25 MHz crystal is used to generate all required clocks, including the 50 MHz RMII reference clock output for the KSZ8081RNB.

The KSZ8081 provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ8081 I/Os and the board. LinkMD® TDR-based cable diagnostics identify faulty copper cabling.

The KSZ8081MNX and KSZ8081RNB are available in 32-pin, lead-free QFN packages.

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: KSZ8081MNX 32-QFN PIN ASSIGNMENT (TOP VIEW)

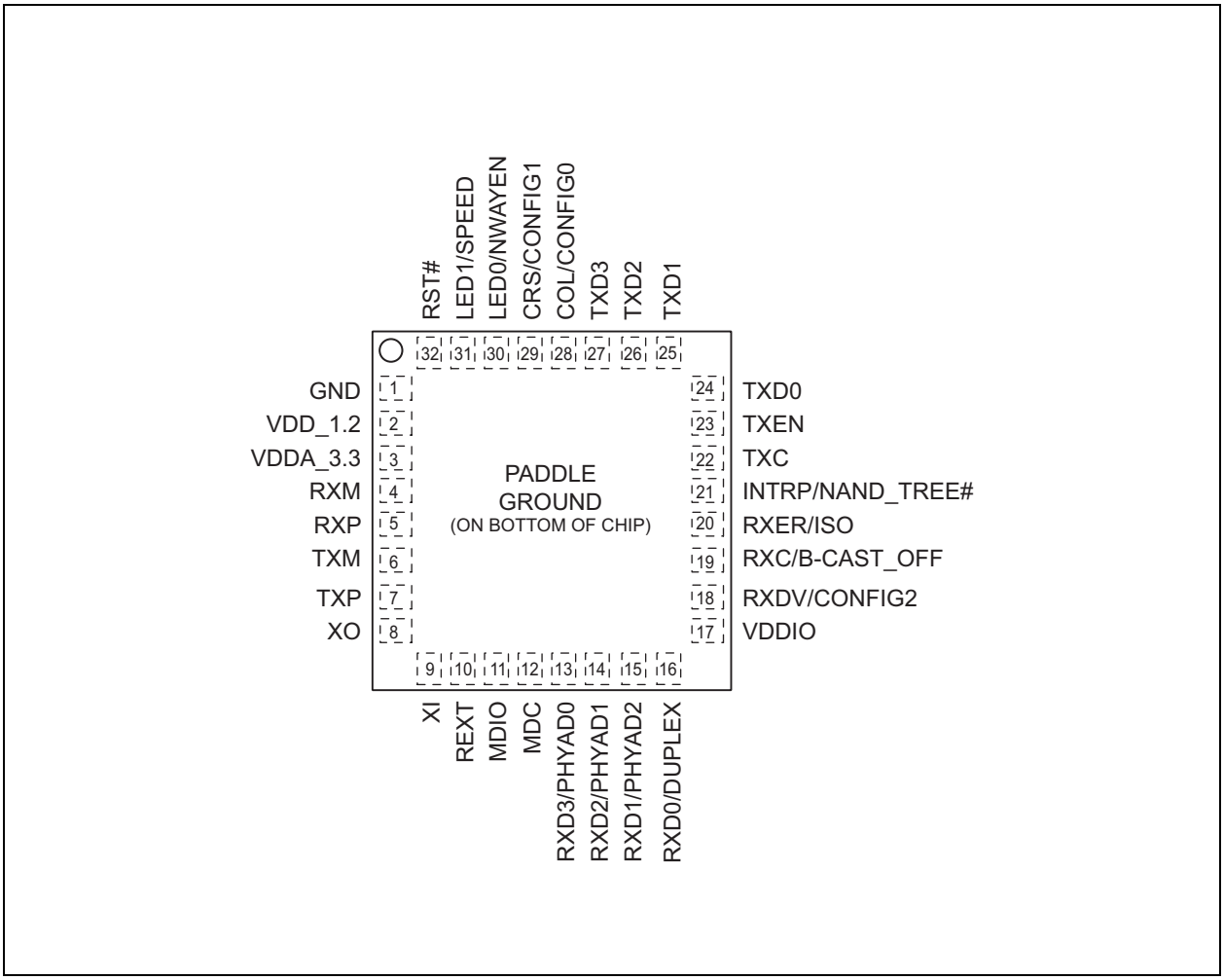


TABLE 2-1: PIN DESCRIPTION — KSZ8081MNX

Pin Number	Name	Buffer Type (Note 2-1)	Description
1	GND	GND	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8081MNX). Decouple with 2.2 µF and 0.1 µF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}.
4	RXM	I/O	Physical receive or transmit signal (– differential).
5	RXP	I/O	Physical receive or transmit signal (+ differential).
6	TXM	I/O	Physical transmit or receive signal (– differential).
7	TXP	I/O	Physical transmit or receive signal (+ differential).

TABLE 2-1: PIN DESCRIPTION — KSZ8081MNX (CONTINUED)

Pin Number	Name	Buffer Type (Note 2-1)	Description
8	XO	O	Crystal feedback for 25 MHz crystal. This pin is a no connect if an oscillator or external clock source is used.
9	XI	I	Crystal / Oscillator / External Clock Input. 25 MHz ±50 ppm.
10	REXT	I	Set PHY transmit output current. Connect a 6.49 kΩ resistor to ground on this pin.
11	MDIO	Ipu/Opu	Management Interface (MII) Data I/O This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor.
12	MDC	Ipu	Management Interface (MII) Clock Input. This clock pin is synchronous to the MDIO data pin.
13	PHYAD0	Ipu/O	MII Mode: MII Receive Data Output[3]. Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See the Strap-In Options – KSZ8081MNX section for details.
14	PHYAD1	Ipd/O	MII Mode: MII Receive Data Output[2] (Note 2-2) Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See the section Strap-In Options – KSZ8081MNX for details.
15	RXD1/ PHYAD2	Ipd/O	MII Mode: MII Receive Data Output[1] (Note 2-2). Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See the section Strap-In Options – KSZ8081MNX for details.
16	RXD0/ DUPLEX	Ipu/O	MII Mode: MII Receive Data Output[0] (Note 2-2). Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See the section Strap-In Options – KSZ8081MNX for details.
17	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DD}.
18	RXDV/ CONFIG2	Ipd/O	MII Mode: MII Receive Data Valid Output. Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See the section Strap-In Options – KSZ8081MNX for details.
19	RXC/ B-CAST_OFF	Ipd/O	MII Mode: MII Receive Clock Output. Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See the section Strap-In Options – KSZ8081MNX for details.
20	RXER/ ISO	Ipd/O	MII mode: MII Receive Error Output. Config Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See the section Strap-In Options – KSZ8081MNX for details.

TABLE 2-1: PIN DESCRIPTION — KSZ8081MNX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Buffer Type (Note 2-1)</th><th>Description</th></tr>
<tr><td>21</td><td>INTRP/

NAND_Tree#</td><td>Ipu/Opu</td><td>Interrupt Output: Programmable Interrupt Output.
This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor.
Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.
See the section Strap-In Options – KSZ8081MNX for details.</td></tr>
<tr><td>22</td><td>TXC</td><td>Ipd/O</td><td>MII Mode: MII Transmit Clock Output.
At the de-assertion of reset, this pin needs to latch in a pull-down value for normal operation. If MAC side pulls this pin high, see Register 16h, Bit [15] for solution. It is better having an external pull-down resistor to avoid MAC side pulls this pin high.</td></tr>
<tr><td>23</td><td>TXEN</td><td>I</td><td>MII Mode: MII Transmit Enable input.</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>MII Mode: MII Transmit Data Input[0] (Note 2-4).</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>MII Mode: MII Transmit Data Input[1] (Note 2-4).</td></tr>
<tr><td>26</td><td>TXD2</td><td>I</td><td>MII Mode: MII Transmit Data Input[2] (Note 2-4).</td></tr>
<tr><td>27</td><td>TXD3</td><td>I</td><td>MII Mode: MII Transmit Data Input[3] (Note 2-4).</td></tr>
<tr><td>28</td><td>COL/
CONFIG0</td><td>Ipd/O</td><td>MII Mode: MII Collision Detect output.
Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset.
See the section Strap-In Options – KSZ8081MNX for details.</td></tr>
<tr><td>29</td><td>CRS/
CONFIG1</td><td>Ipd/O</td><td>MII mode: MII Carrier Sense output
Config mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset.
See the section Strap-In Options – KSZ8081MNX for details.</td></tr>
<tr><td>30</td><td>LED0/
NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output.
Config Mode: Latched as auto-negotiation enable (Register 0h, Bit [12]) at the de-assertion of reset.
See the Strap-In Options – KSZ8081MNX section for details.
The LED0 pin is programmable using Register 1Fh bits [5:4], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01]</th></tr>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
</table>

LED Mode = [10], [11] Reserved</td></tr>
</table>

TABLE 2-1: PIN DESCRIPTION — KSZ8081MNX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Buffer Type (Note 2-1)</th><th>Description</th></tr>
<tr><td>31</td><td>LED1/
SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output.
Config Mode: Latched as Speed (Register 0h, Bit [13]) at the de-assertion of reset.
See the Strap-In Options – KSZ8081MNX section for details.
The LED1 pin is programmable using Register 1Fh bits [5:4], and is defined as follows:
:
<table><tr><th colspan="3">LED Mode = [00]</th></tr><tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>10Base-T</td><td>High</td><td>OFF</td></tr><tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr></table>
<table><tr><th colspan="3">LED Mode = [01]</th></tr><tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No activity</td><td>High</td><td>OFF</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
LED Mode = [10], [11]Reserved</td></tr>
<tr><td>32</td><td>RST#</td><td>Ipu</td><td>Chip Reset (active low).</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>GND</td><td>Ground.</td></tr>
</table>

Note 2-1 P = Power supply.
GND = Ground.
I = Input.
O = Output.
I/O = Bi-directional.
Ipu = Input with internal pull-up (see Electrical Characteristics for value).
Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value).
NC = Pin is not bonded to the die.

Note 2-2 RMII RX Mode: The RXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.

Note 2-3 RMII TX Mode: The TXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

Note 2-4 MII TX Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] presents valid data from the MAC. TXD[3:0] has no effect on the PHY when TXEN is de-asserted.

STRAP-IN OPTIONS – KSZ8081MNX

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC RMII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched to unintended high/low states. In this case, external pull-ups (4.7 kΩ) or pull-downs (1.0 kΩ) should be added on these PHY strap-in pins to ensure that the intended values are strapped-in correctly.

TABLE 2-2: STRAP-IN OPTIONS – KSZ8081MNX

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Pin Function</th></tr>
<tr><td>15
14
13</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>PHYAD[2:0] is latched at de-assertion of reset and is configurable to any value from 0 to 7 with PHY Address 1 as the default value.
PHY Address 0 is assigned by default as the broadcast PHY address, but it can be assigned as a unique PHY address after pulling the B-CAST_OFF strap-in pin high or writing a ‘1’ to Register 16h, Bit [9].
PHY Address bits [4:3] are set to 00 by default.</td></tr>
<tr><td rowspan="4">18
29
28</td><td rowspan="4">CONFIG2
CONFIG1
CONFIG0</td><td rowspan="4">Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.</td></tr>
<tr><td>
<table>
<tr><th>CONFIG [2:0]</th><th>Mode</th></tr>
<tr><td>000</td><td>MII</td></tr>
<tr><td>110</td><td>MII back-to-back</td></tr>
<tr><td>001-100, 111</td><td>Reserved - not used</td></tr>
</table>
</td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>Isolate mode
Pull-up = Enable
Pull-down (default) = Disable
At the de-assertion of reset, this pin value is latched into Register 0h, Bit [10].</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>Speed Mode:
Pull-up (default) = 100 Mbps
Pull-down = 10 Mbps
At the de-assertion of reset, this pin value is latched into Register 0h, Bit [13] as the speed select, and also is latched into Register 4h (auto-negotiation advertisement) as the speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>Duplex Mode:
Pull-up (default) = Half-duplex
Pull-down = Full-duplex
At the de-assertion of reset, this pin value is latched into Register 0h, Bit [8].</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway auto-negotiation enable
Pull-up (default) = Enable auto-negotiation
Pull-down = Disable auto-negotiation
At the de-assertion of reset, this pin value is latched into Register 0h, Bit [12].</td></tr>
<tr><td>19</td><td>B-CAST_OFF</td><td>Ipd/O</td><td>Broadcast off – for PHY Address 0
Pull-up = PHY Address 0 is set as an unique PHY address
Pull-down (default) = PHY Address 0 is set as a broadcast PHY address
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
<tr><td>21</td><td>NAND_Tree#</td><td>Ipu/
Opu</td><td>NAND tree mode
Pull-up (default) = Disable
Pull-down = Enable
At the de-assertion of reset, this pin value is latched by the chip.</td></tr>
</table>

Note 2-1 Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value).

FIGURE 2-2: KSZ8081RNB 32-QFN PIN ASSIGNMENT (TOP VIEW)

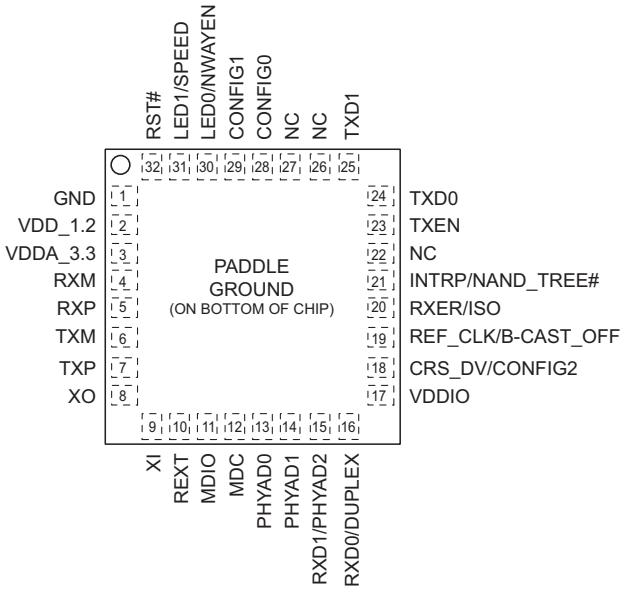


TABLE 2-3: PIN DESCRIPTION — KSZ8081RNB

Pin Number	Pin Name	Type (Note 2-1)	Pin Function
1	GND	GND	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8081RNB). Decouple with 2.2 µF and 0.1 µF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}.
4	RXM	I/O	Physical receive or transmit signal (– differential).
5	RXP	I/O	Physical receive or transmit signal (+ differential).
6	TXM	I/O	Physical transmit or receive signal (– differential).
7	TXP	I/O	Physical transmit or receive signal (+ differential).
8	XO	O	Crystal feedback for 25 MHz crystal. This pin is a no connect if an oscillator or external clock source is used.
9	XI	I	25 MHz Mode: 25 MHz ±50 ppm Crystal / Oscillator / External Clock Input 50 MHz Mode: 50 MHz ±50 ppm Oscillator / External Clock Input
10	REXT	I	Set PHY transmit output current. Connect a 6.49 kΩ resistor to ground on this pin.
11	MDIO	Ipu/Opu	Management Interface (MII) Data I/O. This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor.
12	MDC	Ipu	Management Interface (MII) Clock Input. This clock pin is synchronous to the MDIO data pin.
13	PHYAD0	Ipu/O	The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.

TABLE 2-3: PIN DESCRIPTION — KSZ8081RNB (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Pin Function
14	PHYAD1	Ipd/O	The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.
15	RXD1/ PHYAD2	Ipd/O	RMII Mode: RMII Receive Data Output[1] (Note 2-2). Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.
16	RXD0/ DUPLEX	Ipu/O	RMII Mode: RMII Receive Data Output[0] (Note 2-2). Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.
17	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DD}.
18	CRS_DV/ CONFIG2	Ipd/O	RMII Mode: RMII Carrier Sense/Receive Data Valid Output. Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.
19	REF_CLK/ B-CAST_OFF	Ipd/O	RMII Mode: 25 MHz Mode: This pin provides the 50 MHz RMII reference clock output to the MAC. See also XI (Pin 9). 50 MHz mode: This pin is a no connect. See also XI (Pin 9). Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.
20	RXER/ ISO	Ipd/O	RMII Mode: RMII Receive Error Output. Config Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.
21	INTRP/ NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output. This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.
22	NC	—	No Connect. This pin is not bonded and can be left floating.
23	TXEN	I	RMII Transmit Enable input.
24	TXD0	I	RMII Transmit Data Input[0] (Note 2-3).
25	TXD1	I	RMII Transmit Data Input[1] (Note 2-3).
26	NC	—	No Connect. This pin is not bonded and can be left floating.
27	NC	—	No Connect. This pin is not bonded and can be left floating.

TABLE 2-3: PIN DESCRIPTION — KSZ8081RNB (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Pin Function</th></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.</td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See the Strap-in Options – KSZ8081RNB section for details.</td></tr>
<tr><td>30</td><td>LED0/
NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output.
Config Mode: Latched as auto-negotiation enable (Register 0h, Bit [12]) at the de-assertion of reset.
See the Strap-in Options – KSZ8081RNB section for details.
The LED0 pin is programmable using Register 1Fh bits [5:4], and is defined as follows:
<table><tr><th colspan="3">LED Mode = [00]</th></tr><tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No link</td><td>High</td><td>OFF</td></tr><tr><td>Link</td><td>Low</td><td>ON</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
<table><tr><th colspan="3">LED Mode = [01]</th></tr><tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No link</td><td>High</td><td>OFF</td></tr><tr><td>Link</td><td>Low</td><td>ON</td></tr></table>
LED Mode = [10], [11] Reserved</td></tr>
<tr><td>31</td><td>LED1/ SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output.
Config Mode: Latched as Speed (Register 0h, Bit [13]) at the de-assertion of reset.
See the Strap-in Options – KSZ8081RNB section for details.
The LED1 pin is programmable using Register 1Fh bits [5:4], and is defined as follows:
<table><tr><th colspan="3">LED Mode = [00]</th></tr><tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>10Base-T</td><td>High</td><td>OFF</td></tr><tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr></table>
<table><tr><th colspan="3">LED Mode = [01]</th></tr><tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No activity</td><td>High</td><td>OFF</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
LED Mode = [10], [11] Reserved</td></tr>
<tr><td>32</td><td>RST#</td><td>Ipu</td><td>Chip Reset (active low).</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>GND</td><td>Ground.</td></tr>
</table>

Note 2-1 P = Power supply. GND = Ground. I = Input. O = Output. I/O = Bi-directional. Ipu = Input with internal pull-up (see Electrical Characteristics for value). Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise. Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise. Ipu/Opu

= Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value). NC = Pin is not bonded to the die.

Note 2-2 RMII RX Mode: The RXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.

Note 2-3 RMII TX Mode: The TXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock. For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

STRAP-IN OPTIONS – KSZ8081RNB

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC RMII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched to unintended high/low states. In this case, external pull-ups (4.7 kΩ) or pull-downs (1.0 kΩ) should be added on these PHY strap-in pins to ensure that the intended values are strapped-in correctly.

TABLE 2-4: STRAP-IN OPTIONS

Pin Number	Pin Name	Type (Note 2-1)	Pin Function
15 14 13	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	PHYAD[2:0] is latched at de-assertion of reset and is configurable to any value from 0 to 7 with PHY Address 1 as the default value. PHY Address 0 is assigned by default as the broadcast PHY address, but it can be assigned as a unique PHY address after pulling the B-CAST_OFF strapping pin high or writing a '1' to Register 16h, Bit [9]. PHY Address bits [4:3] are set to 00 by default.
18 29 28	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset. **CONFIG[2:0]** / **Mode** 001 / RMII 101 / RMII back-to-back 000, 010 – 100, 110, 111 / Reserved – not used
20	ISO	Ipd/O	Isolate mode Pull-up = Enable Pull-down (default) = Disable At the de-assertion of reset, this pin value is latched into Register 0h, Bit [10].
31	SPEED	Ipu/O	Speed mode Pull-up (default) = 100 Mbps Pull-down = 10 Mbps At the de-assertion of reset, this pin value is latched into Register 0h, Bit [13] as the speed select, and also is latched into Register 4h (auto-negotiation advertisement) as the speed capability support.
16	DUPLEX	Ipu/O	Duplex mode Pull-up (default) = Half-duplex Pull-down = Full-duplex At the de-assertion of reset, this pin value is latched into Register 0h, Bit [8].
30	NWAYEN	Ipu/O	Nway auto-negotiation enable Pull-up (default) = Enable auto-negotiation Pull-down = Disable auto-negotiation At the de-assertion of reset, this pin value is latched into Register 0h, Bit [12].
19	B-CAST_OFF	Ipd/O	Broadcast off – for PHY Address 0 Pull-up = PHY Address 0 is set as an unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
21	NAND_Tree#	Ipu/ Opu	NAND tree mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Note 2-1 Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value).

3.0 FUNCTIONAL DESCRIPTION

3.1 10BASE-T/100BASE-TX Transceiver

The KSZ8081 is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8081 supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI–X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8081MNX offers the Media Independent Interface (MII) and the KSZ8081RNB offers the Reduced Media Independent Interface (RMII) for direct connection with MII and RMII compliant Ethernet MAC processors and switches, respectively.

The MII management bus option gives the MAC processor complete access to the KSZ8081 control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

The KSZ8081MNX/RNB is used to refer to both KSZ8081MNX and KSZ8081RNB versions in this datasheet.

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal to NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave shaping and pre-emphasis, and output 10BASE-T signals with a typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV, or with short pulse widths, to prevent noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8081MNX/RNB decodes a data frame. The receive clock is kept active during idle periods between data receptions.

3.1.6 SQE AND JABBER FUNCTION (10BASE-T ONLY)

In 10BASE-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE test is needed to test the 10BASE-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10BASE-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10BASE-T transmitter is re-enabled and COL is de-asserted (returns to low).

3.1.7 PLL CLOCK SYNTHESIZER

The KSZ8081MNX/RNB generates all internal clocks and all external clocks for system timing from an external 25 MHz crystal, oscillator, or reference clock. For the KSZ8081RNB in RMII 50 MHz clock mode, these clocks are generated from an external 50 MHz oscillator or system clock.

3.1.8 AUTO-NEGOTIATION

The KSZ8081MNX/RNB conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full–duplex
- Priority 2: 100BASE-TX, half–duplex
- Priority 3: 10BASE-T, full–duplex
- Priority 4: 10BASE-T, half–duplex

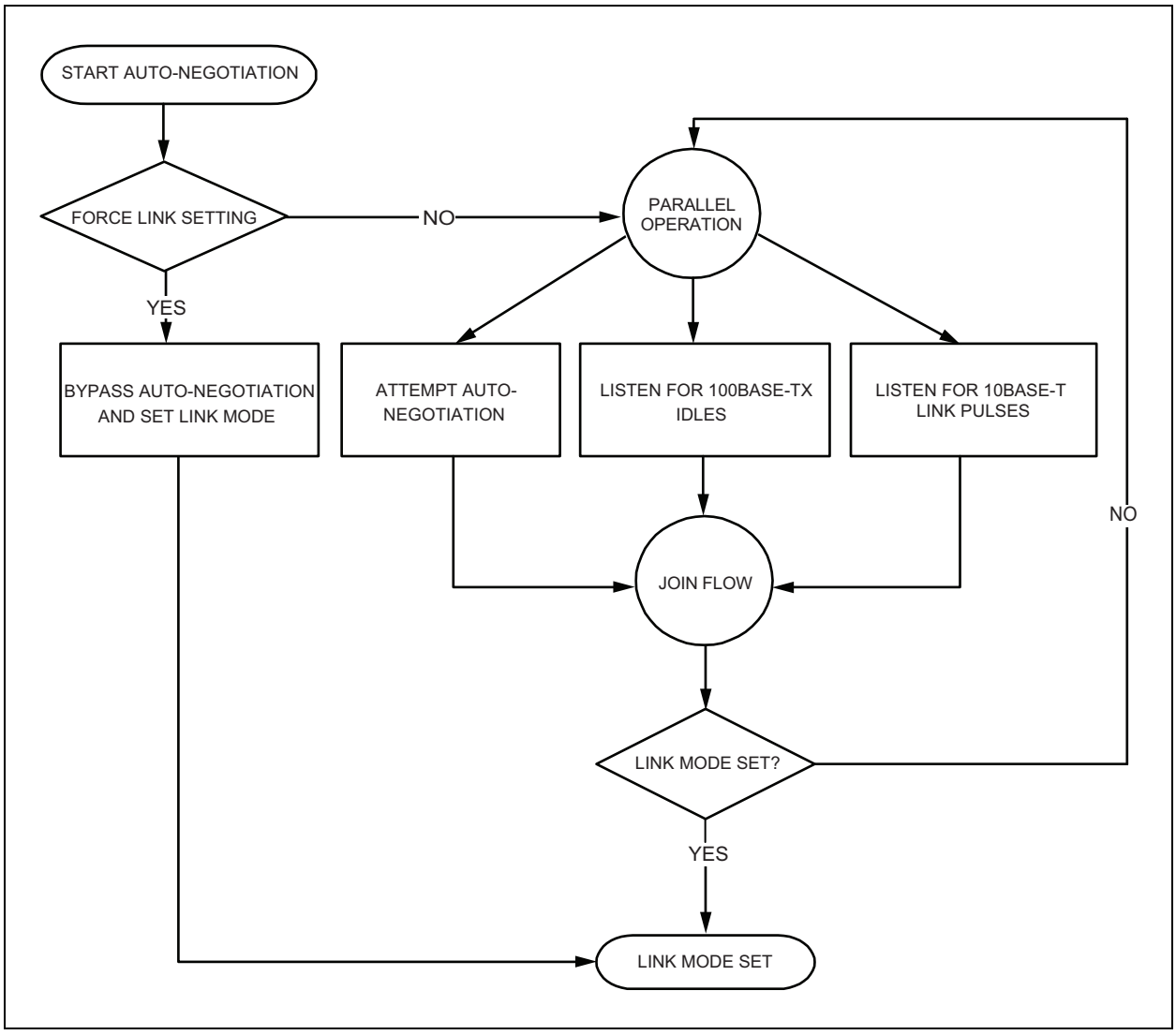
If auto-negotiation is not supported or the KSZ8081MNX/RNB link partner is forced to bypass auto-negotiation, then the KSZ8081MNX/RNB sets its operating mode by observing the signal at its receiver. This is known as parallel detection, which allows the KSZ8081MNX/RNB to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (NWAYEN, Pin 42) or software (Register 0h, Bit [12]).

By default, auto-negotiation is enabled after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled by Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bit [13], and the duplex is set by Register 0h, Bit [8].

The auto-negotiation link-up process is shown in Figure 3-1.

FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART



3.2 MII Interface (KSZ8081MNX Only)

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 15 pins (6 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4 bits wide, a nibble.

By default, the KSZ8081MNX is configured to MII mode after it is powered up or hardware reset with the following:

A 25 MHz crystal connected to XI, XO (pins 9, 8), or an external 25 MHz clock source (oscillator) connected to XI.

The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to 000 (default setting).

3.2.1 MII SIGNAL DEFINITION

Table 3-1 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

TABLE 3-1: MII SIGNAL DEFINITION

MII Signal Name	Direction (with respect to PHY, KSZ8081MNX signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data[3:0]
RXC	Output	Input	Receive Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data[3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

3.2.2 TRANSMIT CLOCK (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0]. TXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.2.3 TRANSMIT ENABLE (TXEN)

TXEN indicates that the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII. It is negated before the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

3.2.4 TRANSMIT DATA[3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted by the PHY for transmission. TXD[3:0] is 00 to indicate idle when TXEN is de-asserted. Values other than 00 on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

3.2.5 RECEIVE CLOCK (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10 Mbps mode, RXC is recovered from the line while the carrier is active. RXC is derived from the PHY's reference clock when the line is idle or the link is down.
- In 100 Mbps mode, RXC is continuously recovered from the line. If the link is down, RXC is derived from the PHY's reference clock.

RXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.2.6 RECEIVE DATA VALID (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10 Mbps mode, RXDV is asserted with the first nibble of the start-of-frame delimiter (SFD), 5D, and remains asserted until the end of the frame.
- In 100 Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

3.2.7 RECEIVE DATA[3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

3.2.8 RECEIVE ERROR (RXER)

RXER is asserted for one or more RXC periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

3.2.9 CARRIER SENSE (CRS)

CRS is asserted and de-asserted as follows:

- In 10 Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100 Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

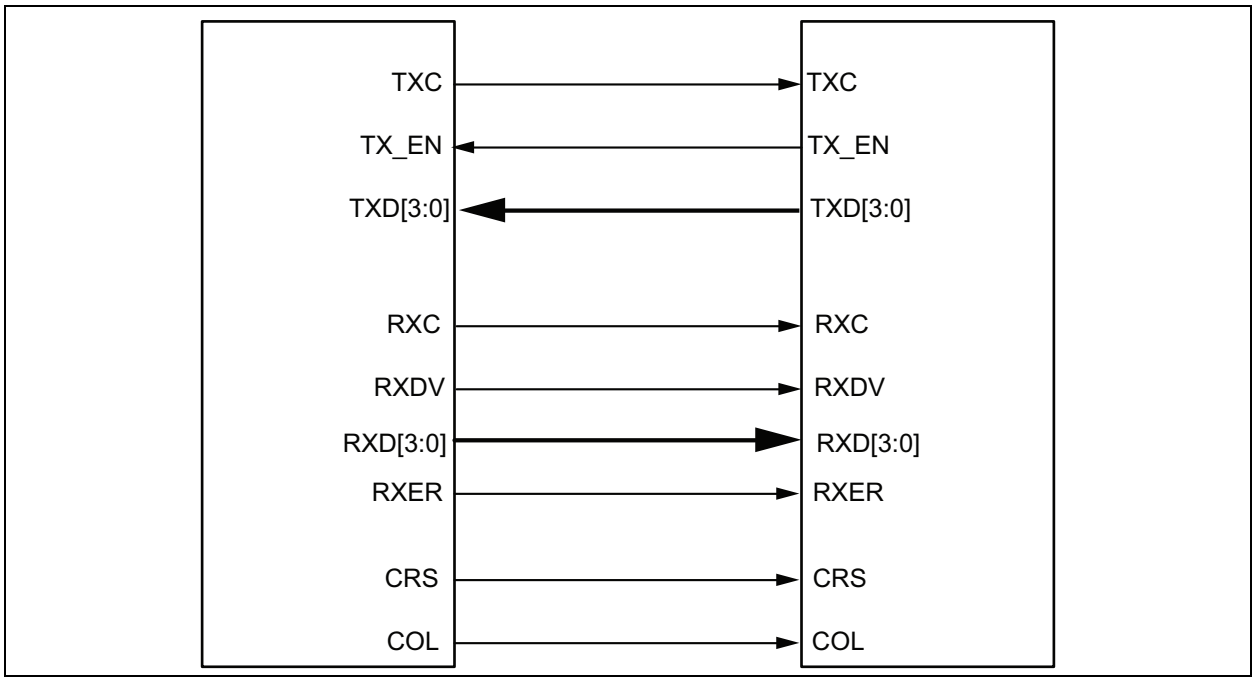
3.2.10 COLLISION (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This informs the MAC that a collision has occurred during its transmission to the PHY. COL transitions asynchronously with respect to TXC and RXC.

3.2.11 MII SIGNAL DIAGRAM

The KSZ8081MNX MII pin connections to the MAC are shown in Figure 3-2.

FIGURE 3-2: KSZ8081MNX MII INTERFACE



3.3 RMII Data Interface (KSZ8081RNB Only)

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, and 1 pin for the 50 MHz reference clock).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2 bits wide, a dibit.

3.3.1 RMII – 25 MHZ CLOCK MODE

The KSZ8081RNB is configured to RMII – 25 MHz clock mode after it is powered up or hardware reset with the following:

- A 25 MHz crystal connected to XI, XO (pins 9, 8), or an external 25 MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to 001.
- Register 1Fh, Bit [7] is set to 0 (default value) to select 25 MHz clock mode.

3.3.2 RMII – 50 MHZ CLOCK MODE

The KSZ8081RNB is configured to RMII – 50 MHz clock mode after it is powered up or hardware reset with the following:

- An external 50 MHz clock source (oscillator) connected to XI (Pin 9).
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to 001.
- Register 1Fh, Bit [7] is set to 1 to select 50 MHz clock mode.

3.3.3 RMII SIGNAL DEFINITION

Table 3-2 describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.

TABLE 3-2: RMII SIGNAL DEFINITION

MII Signal Name	Direction (with respect to PHY, KSZ8081MNX signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data[3:0]
RXC	Output	Input	Receive Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data[3:0]

3.3.4 REFERENCE CLOCK (REF_CLK)

REF_CLK is a continuous 50 MHz clock that provides the timing reference for TXEN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For 25 MHz clock mode, the KSZ8081RNB generates and outputs the 50 MHz RMII REF_CLK to the MAC at REF_CLK (Pin 19).

For 50 MHz clock mode, the KSZ8081RNB takes in the 50 MHz RMII REF_CLK from the MAC or system board at XI (Pin 9) and leaves the REF_CLK (Pin 19) as a no connect.

3.3.5 TRANSMIT ENABLE (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII. It is negated before the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

3.3.6 TRANSMIT DATA[1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TXEN is asserted, the PHY accepts TXD[1:0] for transmission.

TXD[1:0] is 00 to indicate idle when TXEN is de-asserted. The PHY ignores values other than 00 on TXD[1:0] while TXEN is de-asserted.

3.3.7 CARRIER SENSE/RECEIVE DATA VALID (CRS_DV)

The PHY asserts CRS_DV when the receive medium is non-idle. It is asserted asynchronously when a carrier is detected. This happens when squelch is passed in 10 Mbps mode, and when two non-contiguous 0s in 10 bits are detected in 100 Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

While carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit. It is negated before the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid after CRS_DV is asserted. However, because the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is 00 until receive signals are properly decoded.

3.3.8 RECEIVE DATA[1:0] (RXD[1:0])

RXD[1:0] transitions synchronously with respect to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] is 00 to indicate idle when CRS_DV is de-asserted. The MAC ignores values other than 00 on RXD[1:0] while CRS_DV is de-asserted.

3.3.9 RECEIVE ERROR (RXER)

RXER is asserted for one or more REF_CLK periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to REF_CLK. . While CRS_DV is de-asserted, RXER has no effect on the MAC.

3.3.10 COLLISION DETECTION (COL)

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

3.3.11 RMII SIGNAL DIAGRAM

The KSZ8081RNB RMII pin connections to the MAC for 25 MHz clock mode are shown in Figure 3-3. The connections for 50 MHz clock mode are shown in Figure 3-4.

FIGURE 3-3: KSZ8081RNB RMII INTERFACE (25 MHZ CLOCK MODE)

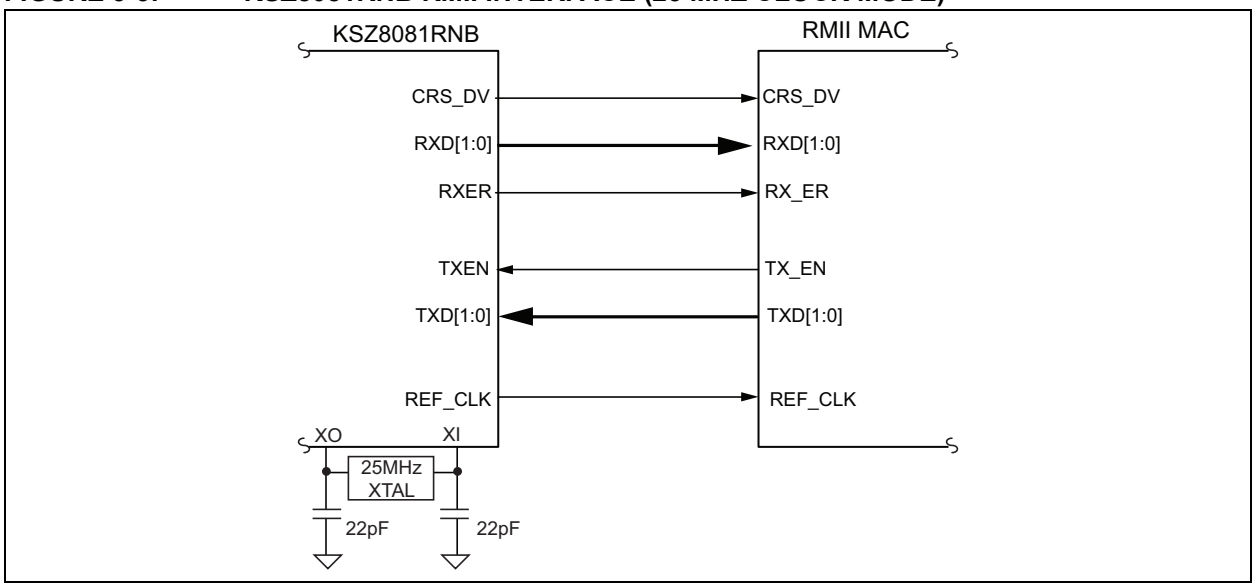
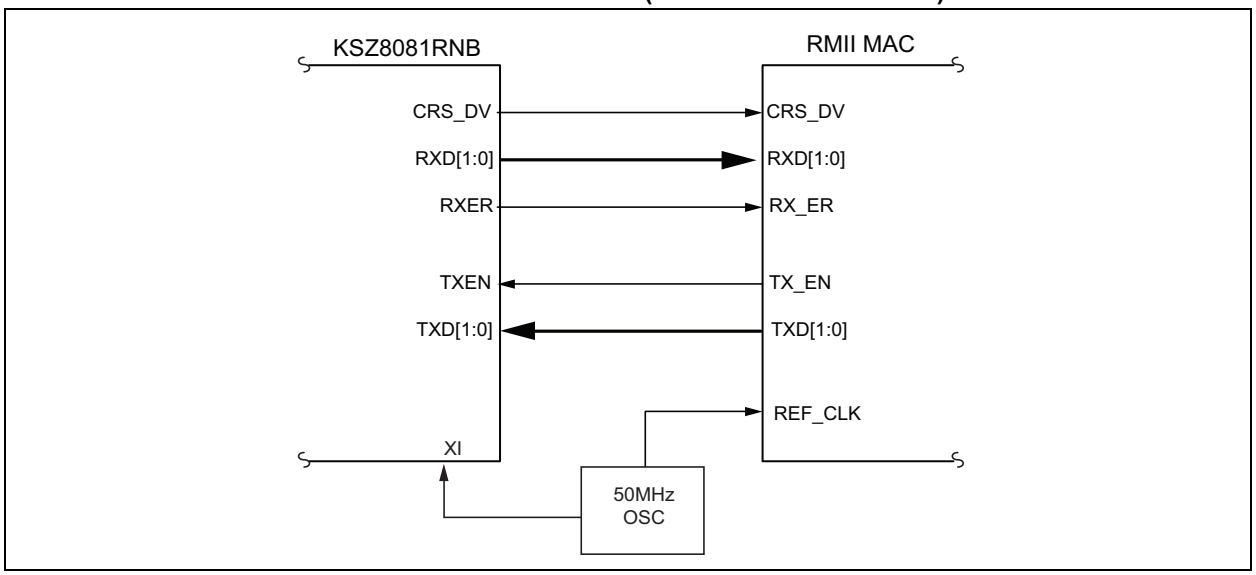


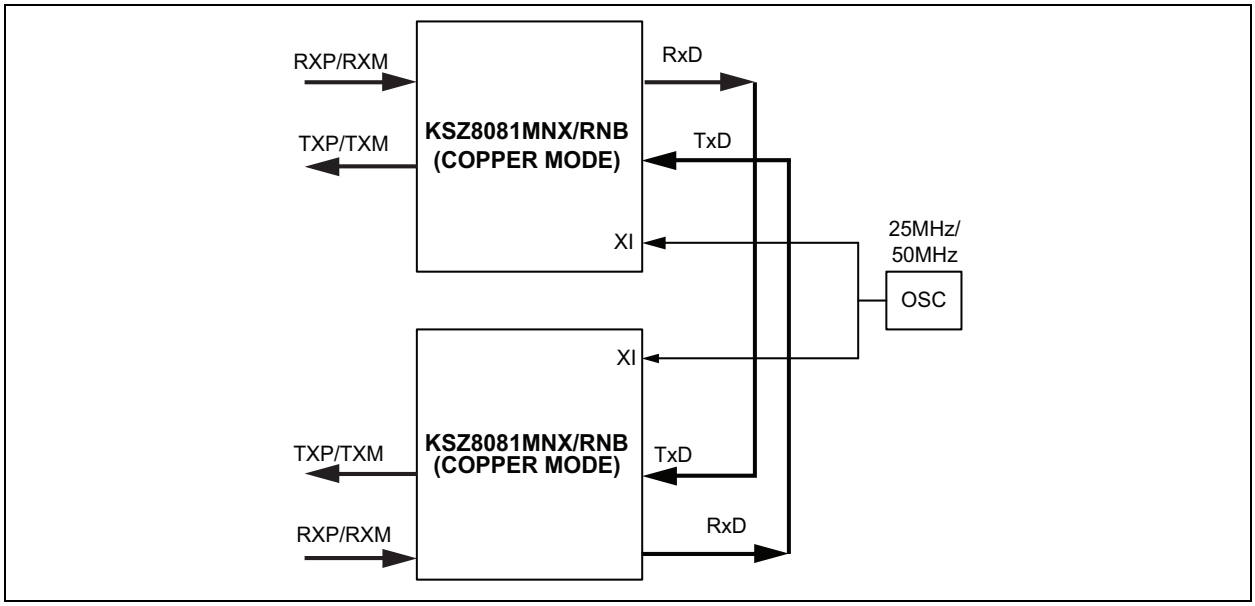
FIGURE 3-4: KSZ8081RNB RMII INTERFACE (50 MHZ CLOCK MODE)



3.4 Back-to-Back Mode – 100 Mbps Copper Repeater

Two KSZ8081MNX/RNB devices can be connected back-to-back to form a 100BASE-TX copper repeater.

FIGURE 3-5: KSZ8081MNX/RNB TO KSZ8081MNX/RNB BACK-TO-BACK COPPER REPEATER



3.4.1 MII BACK-TO-BACK MODE (KSZ8081MNX ONLY)

In MII back-to-back mode, a KSZ8081MNX interfaces with another KSZ8081MNX to provide a complete 100 Mbps copper repeater solution.

The KSZ8081MNX devices are configured to MII back-to-back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] (Pins 18, 29, 28) set to 110
- A common 25 MHz reference clock connected to XI (Pin 9) of both KSZ8081MNX devices
- MII signals connected as shown in Table 3-3.

TABLE 3-3: MII SIGNAL CONNECTION FOR MII BACK-TO-BACK MODE (100BASE-TX COPPER REPEATER)

KSZ8081MNX (100BASE-TX copper) [Device 1]			KSZ8081MNX (100BASE-TX copper) [Device 2]		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
RXDV	18	Output	TXEN	23	Input
RXD3	13	Output	TXD3	27	Input
RXD2	14	Output	TXD2	26	Input
RXD1	15	Output	TXD1	25	Input
RXD0	16	Output	TXD0	24	Input
TXEN	23	Input	RXDV	18	Output
TXD3	27	Input	RXD3	13	Output
TXD2	26	Input	RXD2	14	Output
TXD1	25	Input	RXD1	15	Output
TXD0	24	Input	RXD0	16	Output

3.5 MII Management (MIIM) Interface

The KSZ8081MNX/RNB supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8081MNX/RNB. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Registers [0:8] are standard registers, and their functions are defined in the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See the "Register Map" section for details.

As the default, the KSZ8081MNX/RNB supports unique PHY addresses 1 to 7, and broadcast PHY address 0. The latter is defined in the IEEE 802.3 Specification, and can be used to read/write to a single KSZ8081MNX/RNB device, or write to multiple KSZ8081MNX/RNB devices simultaneously.

PHY address 0 can optionally be disabled as the broadcast address by either hardware pin strapping (B-CAST_OFF, Pin 19) or software (Register 16h, Bit [9]), and assigned as a unique PHY address.

The PHYAD[2:0] strapping pins are used to assign a unique PHY address between 0 and 7 to each KSZ8081MNX/RNB device.

The MIIM interface can operates up to a maximum clock speed of 10 MHz MAC clock.

Table 3-4 shows the MII management frame format for the KSZ8081MNX/RNB.

TABLE 3-4: MII MANAGEMENT FRAME FORMAT FOR THE KSZ8081MNX/RNB

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.6 Interrupt (INTRP)

INTRP (Pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8081MNX/RNB PHY register. Bits [15:8] of Register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of Register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [9] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8081MNX/RNB control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

3.7 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8081MNX/RNB and its link partner. This feature allows the KSZ8081MNX/RNB to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs to the KSZ8081MNX/RNB accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a '1' to Register 1Fh, Bit [13]. MDI and MDI-X mode is selected by Register 1Fh, Bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 3-5 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

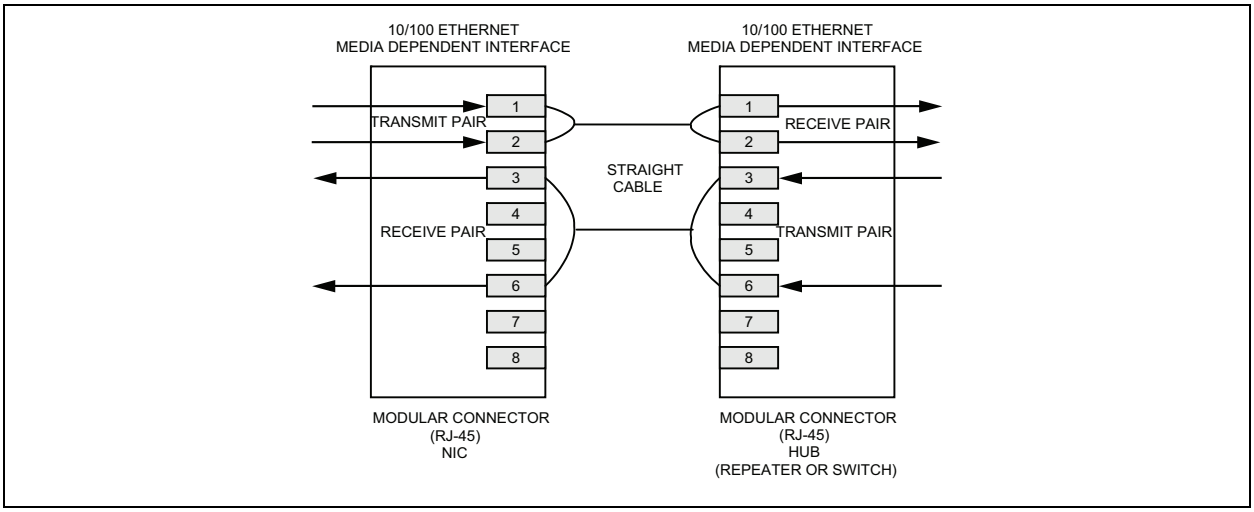
TABLE 3-5: MDI/MDI-X PIN DEFINITION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TX+	1	RX+
2	TX–	2	RX–
3	RX+	3	TX+
6	RX–	6	TX–

3.7.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-6 shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).

FIGURE 3-6: TYPICAL STRAIGHT CABLE CONNECTION



3.7.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-7 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).