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# KSZ8081RNA/RND

## 10BASE-T/100BASE-TX PHY with RMII Support

### Features

- Single-Chip 10BASE-T/100BASE-TX IEEE 802.3 Compliant Ethernet Transceiver
- RMII v1.2 Interface Support with a 50 MHz Reference Clock Output to MAC, and an Option to Input a 50 MHz Reference Clock
- RMII Back-to-Back Mode Support for a 100 Mbps Copper Repeater
- MDC/MDIO Management Interface for PHY Register Configuration
- Programmable Interrupt Output
- LED Outputs for Link and Activity Status Indication
- On-Chip Termination Resistors for the Differential Pairs
- Baseline Wander Correction
- HP Auto MDI/MDI-X to Reliably Detect and Correct Straight-Through and Crossover Cable Connections with Disable and Enable Option
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100 Mbps) and Duplex (Half/Full)
- Power-Down and Power-Saving Modes
- LinkMD® TDR-Based Cable Diagnostics to Identify Faulty Copper Cabling
- Parametric NAND Tree Support for Fault Detection Between Chip I/Os and the Board
- HBM ESD Rating (6 kV)
- Loopback Modes for Diagnostics
- Single 3.3V Power Supply with $V_{DD}$ I/O Options for 1.8V, 2.5V, or 3.3V
- Built-In 1.2V Regulator for Core
- Available in 24-pin 4 mm x 4 mm QFN Package

### Target Applications

- Game Consoles
- IP Phones
- IP Set-Top Boxes
- IP TVs
- LOM
- Printers

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## Table of Contents

# 1.0 INTRODUCTION

## 1.1 General Description

The KSZ8081RNA/RND is a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNA/RND is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core, and by offering 1.8/2.5/3.3V digital I/O interface support.

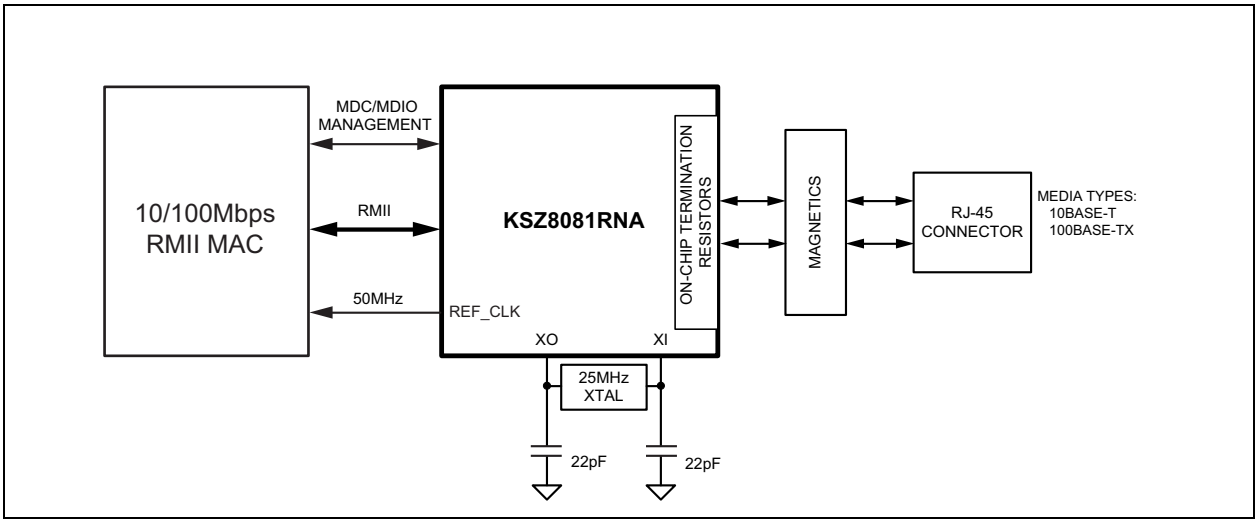
The KSZ8081RNA/RND offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors and switches.

As the power-up default, the KSZ8081RNA/RND uses a 25 MHz crystal to generate all required clocks, including the 50 MHz RMII reference clock output for the MAC. The KSZ8081RND is the version that takes in the 50 MHz RMII reference clock as the power-up default.

To facilitate system bring-up and debugging in production testing and in product deployment, parametric NAND tree support enables fault detection between KSZ8081RNA/RND I/Os and the board. LinkMD® TDR-based cable diagnostics identify faulty copper cabling.

The KSZ8081RNA and KSZ8081RND are available in 24-pin, lead-free QFN packages.

**FIGURE 1-1: SYSTEM BLOCK DIAGRAM**





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## 2.0 PIN DESCRIPTION AND CONFIGURATION

**FIGURE 2-1: 24-QFN PIN ASSIGNMENT (TOP VIEW)**

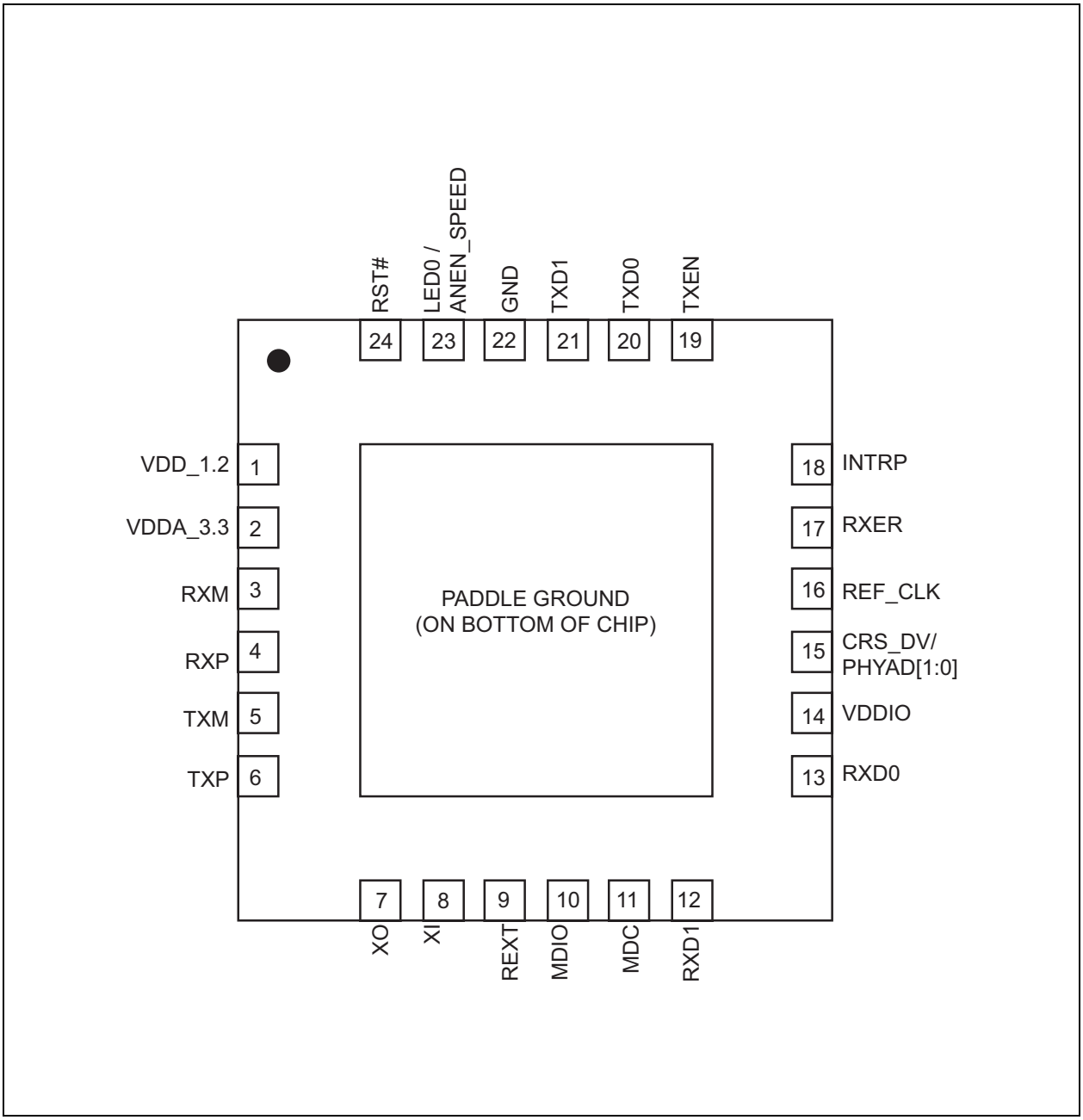

**TABLE 2-1: SIGNALS - KSZ8081RNA/RND**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 1 | VDD_1.2 | P | 1.2V Core $V_{DD}$ (power supplied by KSZ8081RNA/KSZ8081RND). Decouple with 2.2 µF and 0.1 µF capacitors to ground. |
| 2 | VDDA_3.3 | P | 3.3V Analog $V_{DD}$. |
| 3 | RXM | I/O | Physical Receive or Transmit Signal (– differential). |
| 4 | RXP | I/O | Physical Receive or Transmit Signal (+ differential). |
| 5 | TXM | I/O | Physical Transmit or Receive Signal (– differential). |
| 6 | TXP | I/O | Physical Transmit or Receive Signal (+ differential). |
| 7 | XO | O | Crystal Feedback for 25 MHz Crystal. This pin is a no connect if an oscillator or external clock source is used. |
| 8 | XI | I | RMII – 25 MHz Mode: 25 MHz ±50 ppm Crystal/Oscillator/External Clock Input<br>RMII – 50 MHz Mode: 50 MHz ±50 ppm Oscillator/External Clock Input<br>For unmanaged mode (power-up default setting):<br>– KSZ8081RNA takes in the 25 MHz crystal/clock on this pin.<br>– KSZ8081RND takes in the 50 MHz clock on this pin.<br><br>After power-up, both the KSZ8081RNA and KSZ8081RND can be programmed to either the 25 MHz mode or 50 MHz mode using PHY Register 1Fh Bit [7].<br>See also REF_CLK (Pin 16). |
| 9 | REXT | I | Set PHY Transmit Output Current. Connect a 6.49 kΩ resistor to ground on this pin. |
| 10 | MDIO | Ipu/ Opu | Management Interface (MII) Data I/O. This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor. |
| 11 | MDC | Ipu | Management Interface (MII) Clock Input. This clock pin is synchronous to the MDIO data pin. |
| 12 | RXD1 | Ipd/O | RMII Receive Data Output[1] (Note 2-2). |
| 13 | RXD0 | Ipu/O | RMII Receive Data Output[0] (Note 2-2). |
| 14 | VDDIO | P | 3.3V, 2.5V, or 1.8V Digital $V_{DD}$. |
| 15 | CRS_DV/ PHYAD[1:0] | Ipd/O | RMII Mode: Carrier Sense/Receive Data Valid Output.<br>Config. Mode: The pull-up/pull-down value is latched as PHYAD[1:0] at the de-assertion of reset.<br>See the Strapping Options section for details. |


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**TABLE 2-1: SIGNALS - KSZ8081RNA/RND (CONTINUED)**

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td>16</td><td>REF_CLK</td><td>Ipd/O</td><td>RMII – 25 MHz Mode: This pin provides the 50 MHz RMII reference clock output to the MAC.<br>RMII – 50 MHz Mode: This pin is a no connect.<br>For unmanaged mode (power-up default setting),<br>– KSZ8081RNA is in RMII – 25 MHz mode and outputs the 50 MHz RMII reference clock on this pin.<br>– KSZ8081RND is in RMII – 50 MHz mode and does not use this pin.<br><br>After power-up, both KSZ8081RNA and KSZ8081RND can be programmed to either 25 MHz mode or 50 MHz mode using PHY Register 1Fh Bit [7].<br>See also XI (Pin 8).</td></tr>
<tr><td>17</td><td>RXER</td><td>Ipd/O</td><td>RMII Receive Error Output.<br>At the de-assertion of reset, this pin needs to latch in a pull-down value for normal operation. If MAC side pulls this pin high, see Register 16h, Bit [15] for solution. It is better having an external pull-down resistor to avoid MAC side pulls this pin high.</td></tr>
<tr><td>18</td><td>INTRP</td><td>Ipu/ Opu</td><td>Interrupt Output: Programmable interrupt output. This pin has a weak pull-up, is open drain, and requires an external 1.0 kΩ pull-up resistor.</td></tr>
<tr><td>19</td><td>TXEN</td><td>I</td><td>RMII Transmit Enable Input.</td></tr>
<tr><td>20</td><td>TXD0</td><td>I</td><td>RMII Transmit Data Input [0] (Note 2-3).</td></tr>
<tr><td>21</td><td>TXD1</td><td>I/O</td><td>RMII Transmit Data Input [1] (Note 2-3).<br>NAND Tree Mode: NAND Tree output pin.</td></tr>
<tr><td>22</td><td>GND</td><td>GND</td><td>Ground.</td></tr>
<tr><td rowspan="11">23</td><td rowspan="11">LED0/ ANEN_SPEED</td><td rowspan="11">Ipu/O</td><td>LED Output: Programmable LED0 Output.<br>Config. Mode: Latched as auto-negotiation enable (Register 0h, Bit [12]) and Speed (Register 0h, Bit [13]) at the de-assertion of reset. See the Strapping Options section for details.<br>The LED0 pin is programmable using Register 1Fh bits [5:4], and is defined as follows:</td></tr>
<tr><td>LED Mode = [00]</td></tr>
<tr><td>Link/Activity | Pin State | LED Definition<br>No Link | High | OFF<br>Link | Low | ON<br>Activity | Toggle | Blinking</td></tr>
<tr><td>LED Mode = [01]</td></tr>
<tr><td>Link | Pin State | LED Definition<br>No Link | High | OFF<br>Link | Low | ON</td></tr>
<tr><td>LED Mode = [10], [11]: Reserved</td></tr>
<tr><td>24</td><td>RST#</td><td>Ipu</td><td>Chip Reset (active-low).</td></tr>
</table>

**TABLE 2-1: SIGNALS - KSZ8081RNA/RND (CONTINUED)**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| Paddle | GND | GND | Ground. |

**Note 2-1** P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value).
Ipu/O = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value).

**Note 2-2** RMII RX Mode: The RXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.

**Note 2-3** RMII TX Mode: The TXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.


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The PHYAD[1:0] strap-in pin is latched at the de-assertion of reset. In some systems, the RMII MAC receive input pins may drive high/low during power-up or reset, and consequently cause the PHYAD[1:0] strap-in pin, a shared pin with the RMII CRS_DV signal, to be latched to the unintended high/low state. In this case an external pull-up (4.7 kΩ) or pull-down (1.0 kΩ) should be added on the PHYAD[1:0] strap-in pin to ensure that the intended value is strapped-in correctly.

**TABLE 2-2: STRAP-IN OPTIONS - KSZ8081RNA/RND**

| Pin Number | Pin Name | Type Note 2-4 | Description |
|---|---|---|---|
| 15 | PHYAD[1:0] | Ipd/O | The PHY Address is latched at the de-assertion of reset and is configurable to either one of the following two values:<br>Pull-up = PHY Address is set to 00011b (0x3h)<br>Pull-down (default) = PHY Address is set to 00000b (0x0h)<br><br>PHY Address Bits [4:2] are set to 000 by default. |
| 23 | ANEN_SPEED | Ipu/O | Auto-Negotiation Enable and SPEED Mode<br>Pull-up (default) = Enable Auto-Negotiation and set 100 Mbps Speed<br>Pull-down = Disable Auto-Negotiation and set 10 Mbps Speed<br><br>At the de-assertion of reset, this pin value is latched into Register 0h Bit [12] for Auto-negotiation enable/disable, Register 0h Bit [13] for the speed select, and Register 4h (Auto-Negotiation Advertisement) for the speed capability support. |

**Note 2-4** Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.

## 3.0 FUNCTIONAL DESCRIPTION

The KSZ8081RNA is an integrated, single 3.3V supply, fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8081RNA supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8081RNA offers the Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches

The MII management bus option gives the MAC processor complete access to the KSZ8081RNA control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

As the power-up default, the KSZ8081RNA uses a 25 MHz crystal to generate all required clocks, including the 50 MHz RMII reference clock output for the MAC. The KSZ8081RND version uses the 50 MHz RMII reference clock as the power-up default.

The KSZ8081RNA/RND is used to refer to both KSZ8081RNA and KSZ8081RND versions in this data sheet.

### 3.1 10BASE-T/100BASE-TX Transceiver

#### 3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

#### 3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal to NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII format and provided as the input data to the MAC.

#### 3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

#### 3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10BASE-T signals with typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.


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### 3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV, or with short pulse widths, to prevent noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8081RNA/RND decodes a data frame. The receive clock is kept active during idle periods between data receptions.

### 3.1.6 PLL CLOCK SYNTHESIZER

The KSZ8081RNA/RND in RMII – 25 MHz Clock mode generates all internal clocks and all external clocks for system timing from an external 25 MHz crystal, oscillator, or reference clock. For the KSZ8081RNA/RND in RMII – 50 MHz clock mode, these clocks are generated from an external 50 MHz oscillator or system clock.

### 3.1.7 AUTO-NEGOTIATION

The KSZ8081RNA/RND conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

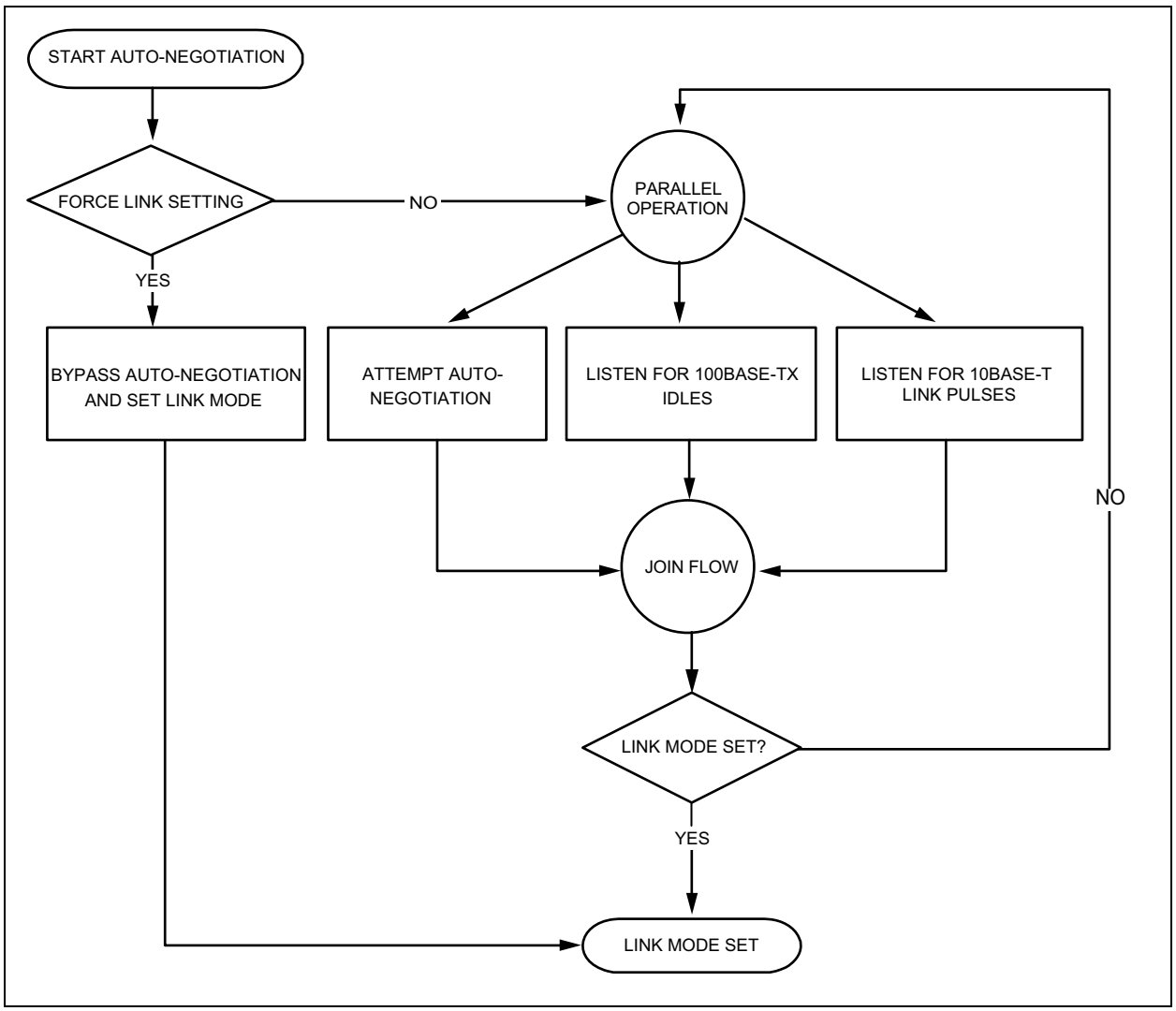
If auto-negotiation is not supported or the KSZ8081RNA/RND link partner is forced to bypass auto-negotiation, then the KSZ8081RNA/RND sets its operating mode by observing the signal at its receiver. This is known as parallel detection, which allows the KSZ8081RNA/RND to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (ANEN_SPEED, Pin 23) or software (Register 0h, Bit [12]).

By default, auto-negotiation is enabled after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled by Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bit [13], and the duplex is set by Register 0h, Bit [8].

The auto-negotiation link-up process is shown in Figure 3-1.

**FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART**




## 3.2 RMII Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, and 1 pin for the 50 MHz reference clock).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2 bits wide, a dibit.

### 3.2.1 RMII SIGNAL DEFINITION

Table 3-1 describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.


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**TABLE 3-1: RMII SIGNAL DEFINITION**

| RMII Signal Name | Direction with Respect to PHY, KSZ8081 Signal | Direction with Respect to MAC | Description |
|---|---|---|---|
| REF_CLK | Output (25 MHz Clock Mode)/ No Connect (50 MHz Clock Mode) | Input/ Input or No Connect | Synchronous 50 MHz reference clock for receive, transmit, and control interface |
| TXEN | Input | Output | Transmit Enable |
| TXD[1:0] | Input | Output | Transmit Data[1:0] |
| CRS_DV | Output | Input | Carrier Sense/Receive Data Valid |
| RXD[1:0] | Output | Input | Receive Data[1:0] |
| RXER | Output | Input or Not Required | Receive Error |

#### 3.2.1.1 Reference Clock (REF_CLK)

REF_CLK is a continuous 50 MHz clock that provides the timing reference for TXEN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For RMII – 25 MHz Clock Mode, the KSZ8081RNA/RND generates and outputs the 50 MHz RMII REF_CLK to the MAC at REF_CLK (Pin 16).

For RMII – 50 MHz Clock Mode, the KSZ8081RNA/RND takes in the 50 MHz RMII REF_CLK from the MAC or system board at XI (Pin 8) and leaves the REF_CLK (Pin 16) as no connect.

#### 3.2.1.2 Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII. It is negated before the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

#### 3.2.1.3 Transmit Data[1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TXEN is asserted, the PHY accepts TXD[1:0] for transmission.

TXD[1:0] is 00 to indicate idle when TXEN is de-asserted. The PHY ignores values other than 00 on TXD[1:0] while TXEN is de-asserted.

#### 3.2.1.4 Carrier Sense/Receive Data Valid (CRS_DV)

The PHY asserts CRS_DV when the receive medium is non-idle. It is asserted asynchronously when a carrier is detected. This happens when squelch is passed in 10 Mbps mode, and when two non-contiguous 0s in 10 bits are detected in 100 Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

While carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit. It is negated before the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid after CRS_DV is asserted. However, because the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is 00 until receive signals are properly decoded.

#### 3.2.1.5 Receive Data[1:0] (RXD[1:0])

RXD[1:0] transitions synchronously with respect to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] is 00 to indicate idle when CRS_DV is de-asserted. The MAC ignores values other than 00 on RXD[1:0] while CRS_DV is de-asserted.

#### 3.2.1.6 Receive Error (RXER)

RXER is asserted for one or more REF_CLK periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RXER has no effect on the MAC.

#### 3.2.1.7 Collision Detection (COL)

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

### 3.2.2 RMII SIGNAL DIAGRAM – 25/50 MHZ CLOCK MODE

The KSZ8081RNA/RND RMII pin connections to the MAC for 25 MHz clock mode are shown in Figure 3-2. The connections for 50 MHz clock mode are shown in Figure 3-3.

#### 3.2.2.1 RMII – 25 MHz Clock Mode

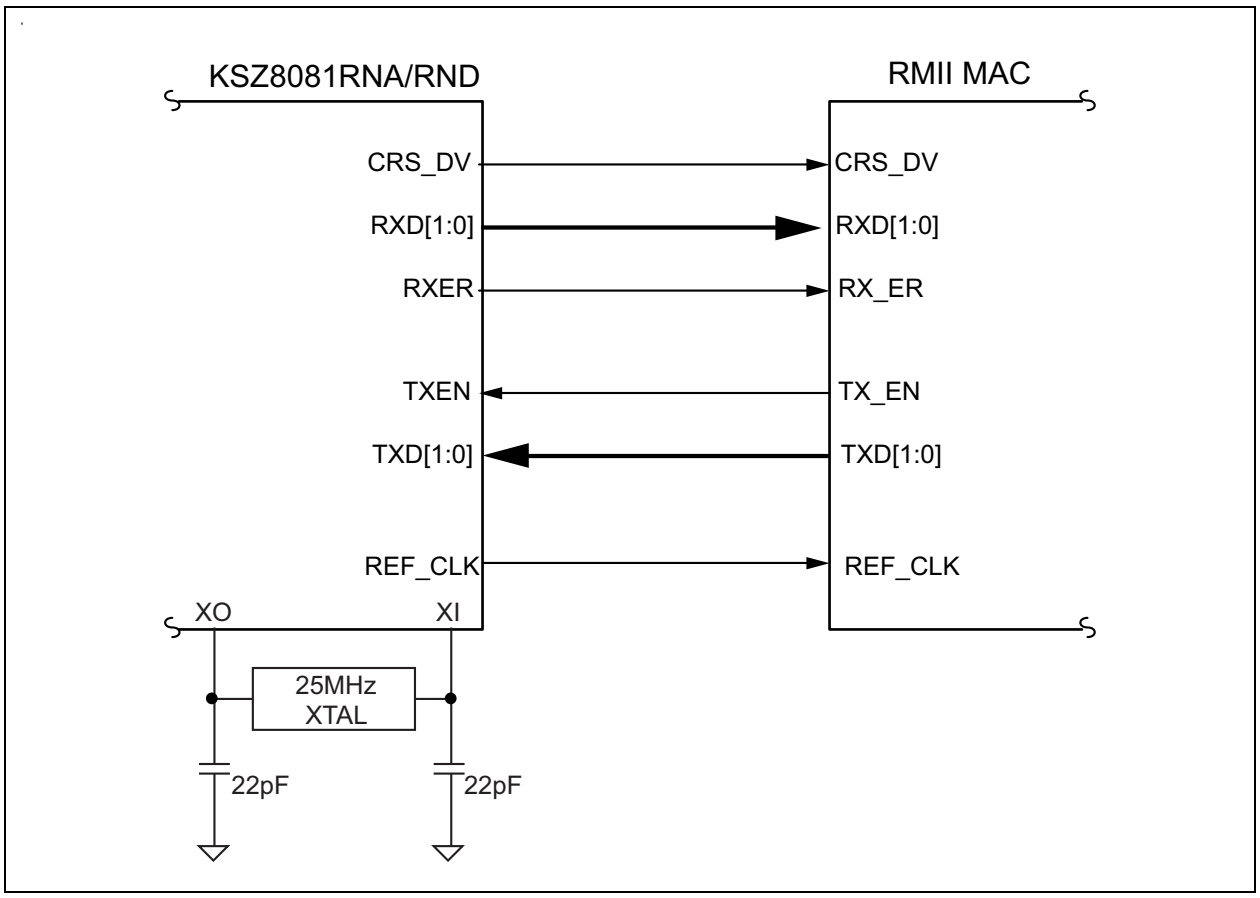
The KSZ8081RNA is configured to RMII – 25 MHz clock mode after it is powered up or hardware reset with the following:

- A 25 MHz crystal connected to XI, XO (Pins 8, 7), or an external 25 MHz clock source (oscillator) connected to XI

The KSZ8081RND can optionally be configured to RMII – 25 MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- A 25 MHz crystal connected to XI, XO (Pins 8, 7), or an external 25 MHz clock source (oscillator) connected to XI
- Register 1Fh, Bit [7] programmed to ‘1’ to select RMII – 25 MHz clock mode

**FIGURE 3-2: KSZ8081RNA/RND RMII INTERFACE (RMII - 25 MHZ CLOCK MODE)**





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#### 3.2.2.2 RMII – 50 MHz Clock Mode

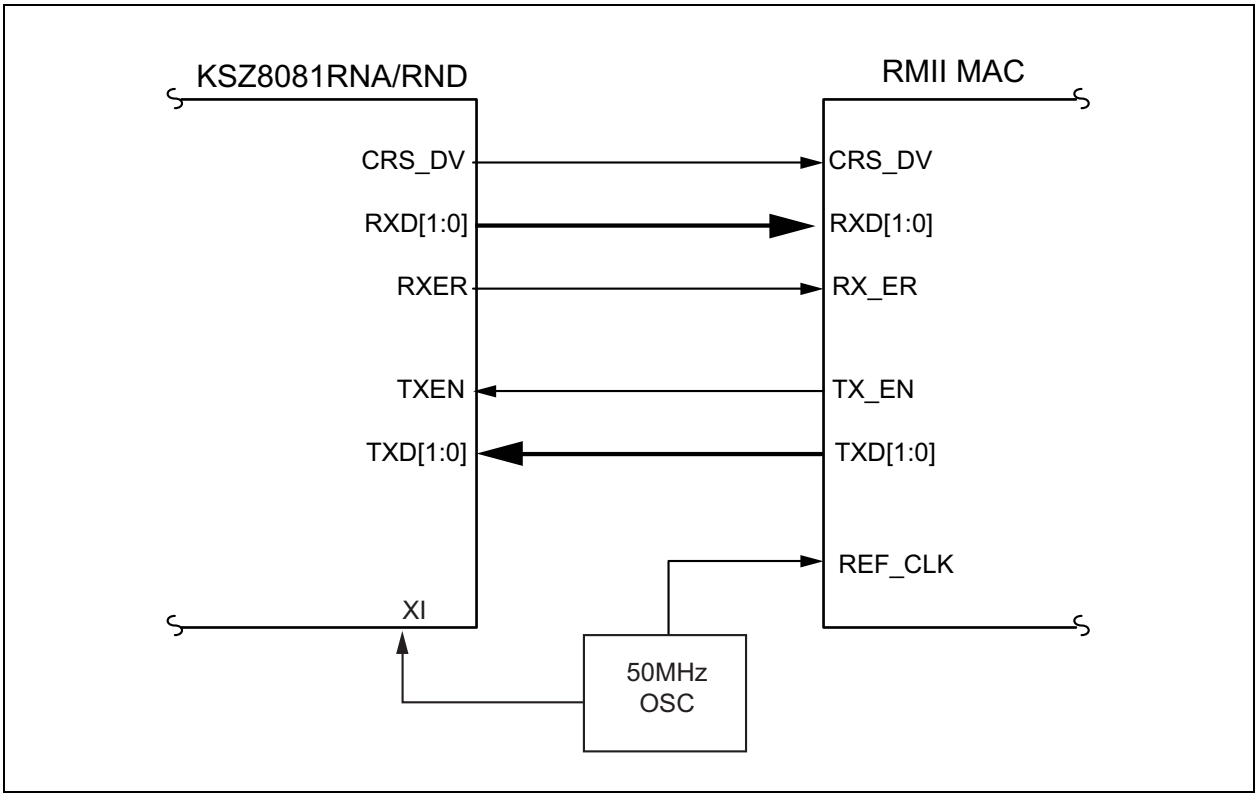
The KSZ8081RND is configured to RMII – 50 MHz clock mode after it is powered up or hardware reset with the following:

- An external 50 MHz clock source (oscillator) connected to XI (Pin 8)

The KSZ8081RNA can optionally be configured to RMII – 50 MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- An external 50 MHz clock source (oscillator) connected to XI (Pin 8)
- Register 1Fh, Bit [7] programmed to '1' to select RMII – 50 MHz clock mode

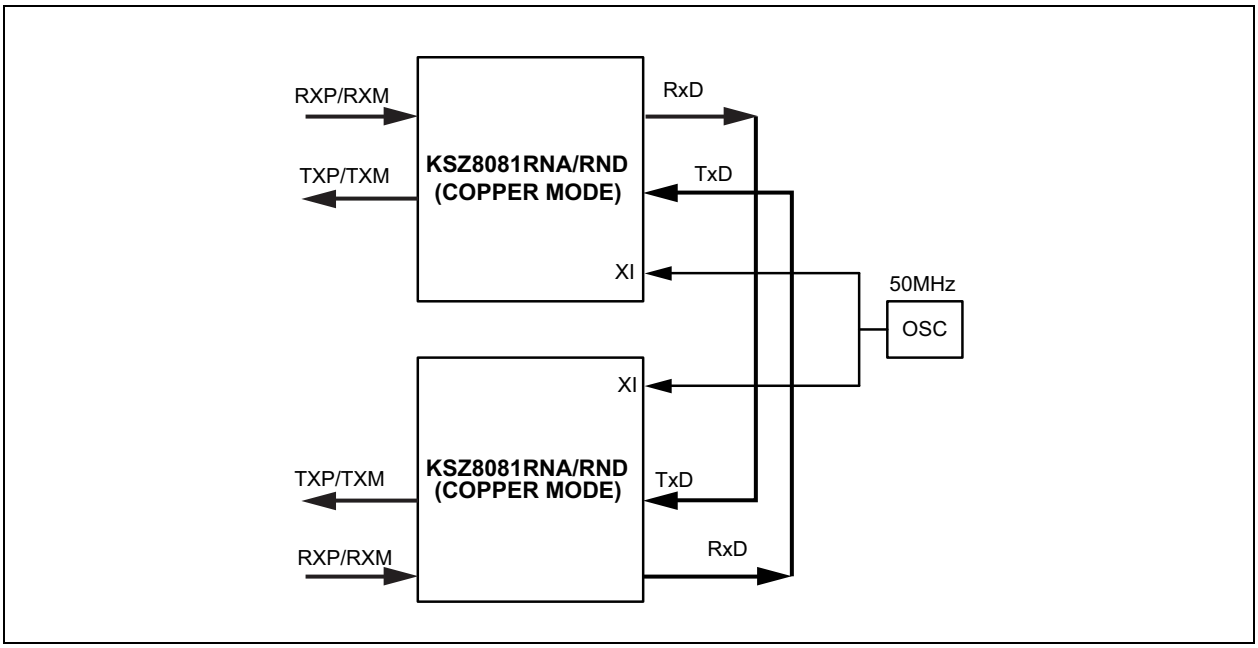
**FIGURE 3-3: KSZ8081RNA/RND RMII INTERFACE (RMII - 50 MHZ CLOCK MODE)**



## 3.3 Back-to-Back Mode – 100 Mbps Copper Repeater

Two KSZ8081RNA/RND devices can be connected back-to-back to form a managed 100BASE-TX copper repeater.

**FIGURE 3-4: KSZ8081RNA/RND AND KSZ8081RNA/RND RMII BACK-TO-BACK COPPER REPEATER**




### 3.3.1 RMII BACK-TO-BACK MODE

In RMII back-to-back mode, a KSZ8081RNA/RND interfaces with another KSZ8081RNA/RND to provide a 100 Mbps copper repeater solution.

The KSZ8081RNA/RND devices are configured to RMII back-to-back mode after power-up or reset, and software programming, with the following:

- A common 50 MHz reference clock connected to XI (Pin 8)
- Register 1Fh, Bit [7] programmed to '1' to select RMII – 50 MHz clock mode for KSZ8081RNA

KSZ8081RND is set to RMII – 50 MHz clock mode as the default after power up or hardware reset.

- Register 16h, Bits [6] and [1] programmed to '1' and '1', respectively, to enable RMII back-to-back mode.
- RMII signals connected as shown in Table 3-2.

**TABLE 3-2: RMII SIGNAL CONNECTION FOR RMII BACK-TO-BACK MODE (100BASE-TX COPPER REPEATER)**

| KSZ8081RNA/RND (100BASE-TX Copper) [Device 1] | | | KSZ8081RNA/RND (100BASE-TX Copper) [Device 2] | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin Number** | **Pin Type** | **Pin Name** | **Pin Number** | **Pin Type** |
| CRS_DV | 15 | Output | TXEN | 19 | Input |
| RXD1 | 12 | Output | TXD1 | 21 | Input |
| RXD0 | 13 | Output | TXD0 | 20 | Input |
| TXEN | 19 | Input | CRS_DV | 15 | Output |
| TXD1 | 21 | Input | RXD1 | 12 | Output |
| TXD0 | 20 | Input | RXD0 | 13 | Output |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## 3.4 MII Management (MIIM) Interface

The KSZ8081RNA/RND supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8081RNA/RND. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Registers [0:8] are standard registers, and their functions are defined in the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See the Register Map section for details.

The KSZ8081RNA/RND supports only two unique PHY addresses. The PHYAD[1:0] strapping pin is used to select either 0h or 3h as the unique PHY address for the KSZ8081RNA/RND device.

PHY address 0h is defined as the broadcast PHY address according to the IEEE 802.3 Specification, and can be used to read/write to a single PHY device, or write to multiple PHY devices simultaneously. For the KSZ8081RNA/RND, PHY address 0h defaults to the broadcast PHY address after power-up, but PHY address 0h can be disabled as the broadcast PHY address using software to assign it as a unique PHY address.

For applications that require two KSZ8081RNA/RND PHYs to share the same MDIO interface with one PHY set to address 0h and the other PHY set to address 3h, use PHY address 0h (defaults to broadcast after power-up) to set both PHYs' Register 16h, Bit [9] to '1' to assign PHY address 0h as a unique (non-broadcast) PHY address.

Table 3-3 shows the MII management frame format for the KSZ8081RNA/RND.

**TABLE 3-3: MII MANAGEMENT FRAME FORMAT FOR THE KSZ8081RNA/RND**

| | Preamble | Start of Frame | Read/ Write OP Code | PHY Address Bits[4:0] | REG Address Bits[4:0] | TA | Data Bits[15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 10 | 000AA | RRRRR | Z0 | DDDDDDDD_DDDDDDDD | Z |
| **Write** | 32 1's | 01 | 01 | 000AA | RRRRR | 10 | DDDDDDDD_DDDDDDDD | Z |

## 3.5 Interrupt (INTRP)

INTRP (Pin 18) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8081RNA/RND PHY register. Bits [15:8] of Register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of Register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [9] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8081RNA/RND control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

## 3.6 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8081RNA/RND and its link partner. This feature allows the KSZ8081RNA/RND to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs to the KSZ8081RNA/RND accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a '1' to Register 1Fh, Bit [13]. MDI and MDI-X mode is selected by Register 1Fh, Bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 3-4 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

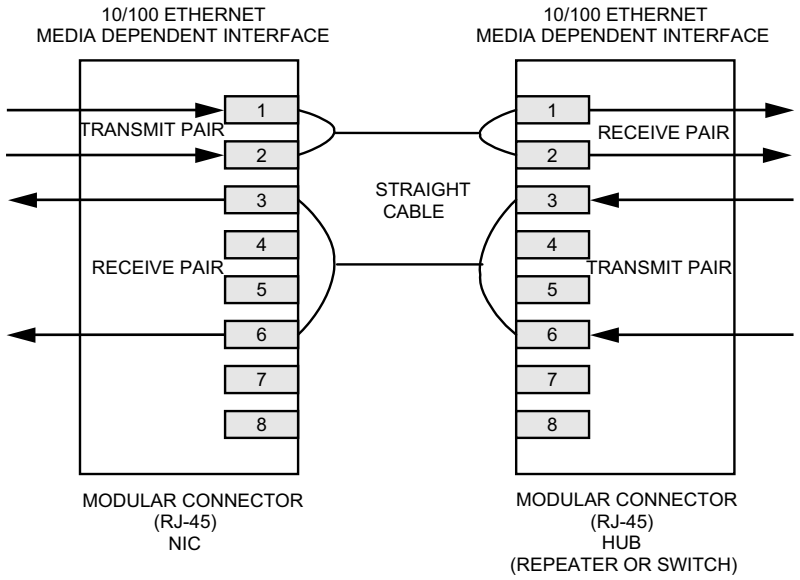
**TABLE 3-4: MDI/MDI-X PIN DESCRIPTION**

| MDI | | MDI-X | |
|---|---|---|---|
| **RJ-45 Pin** | **Signal** | **RJ-45 Pin** | **Signal** |
| 1 | TX+ | 1 | RX+ |
| 2 | TX– | 2 | RX– |
| 3 | RX+ | 3 | TX+ |
| 6 | RX– | 6 | TX– |

### 3.6.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-5 shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).

**FIGURE 3-5: TYPICAL STRAIGHT CABLE CONNECTION**




### 3.6.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-6 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).


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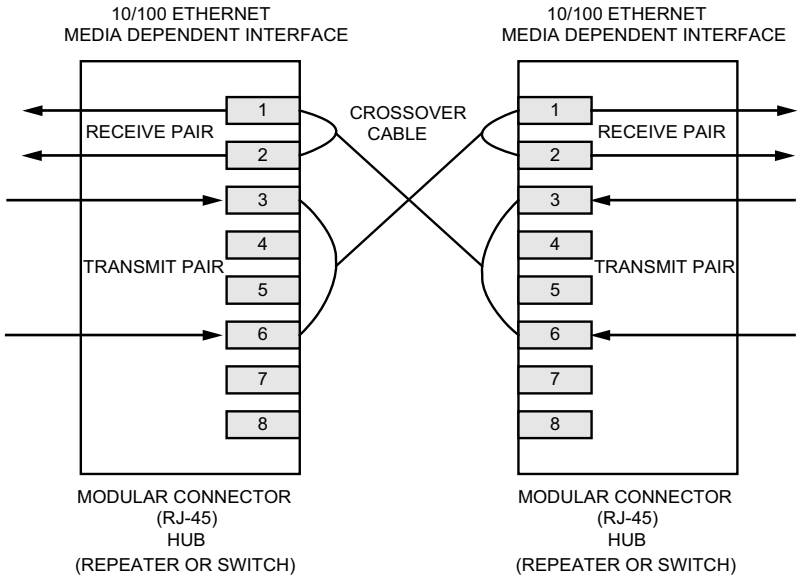
**FIGURE 3-6: TYPICAL CROSSOVER CABLE CONNECTION**




## 3.7 Loopback Mode

The KSZ8081RNA/RND supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

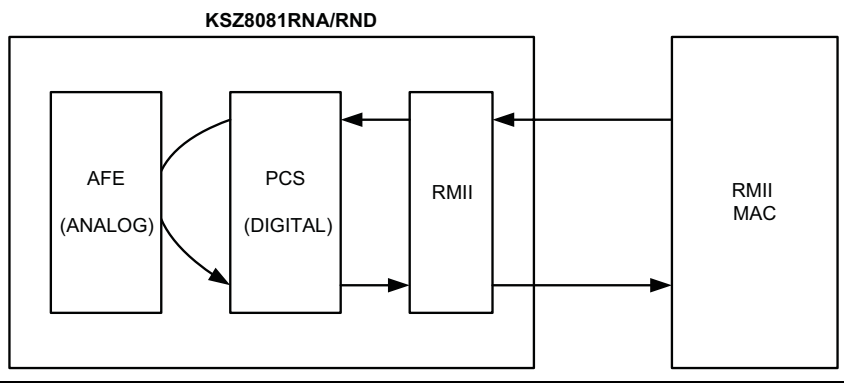
### 3.7.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the RMII transmit and receive data paths between the KSZ8081RNA/RND and the external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-7.

1. The RMII MAC transmits frames to the KSZ8081RNA/RND.
2. Frames are wrapped around inside the KSZ8081RNA/RND.
3. The KSZ8081RNA/RND transmits frames back to the RMII MAC.
4. Except the frames back to the RMII MAC, the transmit frames also go out from the copper port.

**FIGURE 3-7: LOCAL (DIGITAL) LOOPBACK**



The following programming action and register settings are used for local loopback mode:

For 10/100 Mbps loopback:

Set Register 0h,

Bit [14] = 1 // Enable local loopback mode

Bit [13] = 0/1 // Select 10 Mbps/100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

Follow the steps below if you don't want the frames go out from the copper port in the local loopback.

1. Set register 1Fh bit [3] to '1' to disable the transmitter.
2. Run local loopback test as above.
3. Set register 1Fh bit [3] to '0' to enable the transmitter.

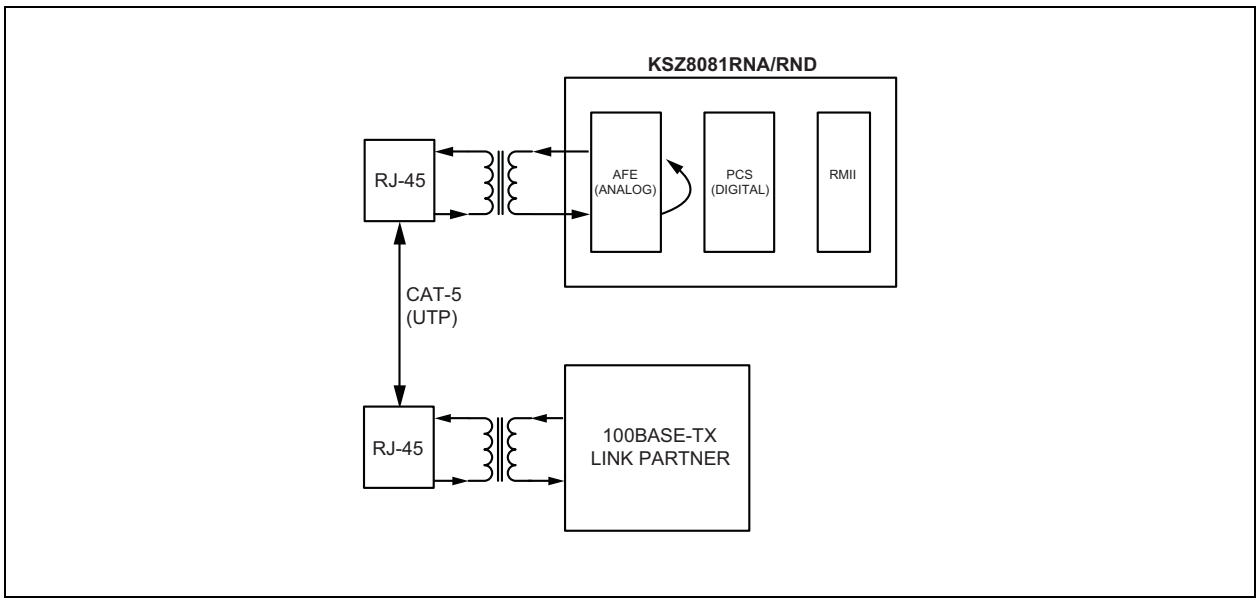
### 3.7.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8081RNA/RND and its link partner, and is supported for 100BASE-TX full-duplex mode only.

The loopback data path is shown in Figure 3-8.

1. The Fast Ethernet (100BASE-TX) PHY link partner transmits frames to the KSZ8081RNA/RND.
2. Frames are wrapped around inside the KSZ8081RNA/RND.
3. The KSZ8081RNA/RND transmits frames back to the Fast Ethernet (100BASE-TX) PHY link partner.

**FIGURE 3-8: REMOTE (ANALOG) LOOPBACK**




The following programming steps and register settings are used for remote loopback mode:

1. Set Register 0h,

Bits [13] = 1 // Select 100Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

Or just auto-negotiate and link up at 100BASE-TX full-duplex mode with the link partner.

2. Set Register 1Fh,

Bit [2] = 1 // Enable remote loopback mode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## 3.8 LinkMD® Cable Diagnostic

The LinkMD function uses time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems. These include open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing Register 1Dh, the LinkMD Control/Status register, in conjunction with Register 1Fh, the PHY Control 2 register. The latter register is used to disable Auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

### 3.8.1 USAGE

The following is a sample procedure for using LinkMD with Registers 1Dh and 1Fh:

1. Disable auto MDI/MDI-X by writing a ‘1’ to Register 1Fh, bit [13].
2. Start cable diagnostic test by writing a ‘1’ to Register 1Dh, bit [15]. This enable bit is self-clearing.
3. Wait (poll) for Register 1Dh, bit [15] to return a ‘0’, and indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 1Dh, bits [14:13]. The results are as follows:

   00 = normal condition (valid test)

   01 = open condition detected in cable (valid test)

   10 = short condition detected in cable (valid test)

   11 = cable diagnostic test failed (invalid test)

The ‘11’ case, invalid test, occurs when the device is unable to shut down the link partner. In this instance, the test is not run, since it would be impossible for the device to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating Register 1Dh, bits [8:0] and multiplying the result by a constant of 0.38. The distance to the cable fault can be determined by the following formula:

**EQUATION 3-1:**

$$D(Distance \text{ to cable fault in meters}) = 0.38 \times (Register \text{ 1Dh, bits[8:0]})$$

Concatenated value of Registers 1Dh bits [8:0] should be converted to decimal before multiplying by 0.38.

The constant (0.38) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

## 3.9 NAND Tree Support

The KSZ8081RNA/RND provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8081RNA/RND digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the TXD1 pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving each NAND tree input pin low, sequentially, according to the NAND tree pin order
- Checking the NAND tree output to make sure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 3-5 lists the NAND tree pin order.

**TABLE 3-5: NAND TREE TEST PIN ORDER FOR KSZ8081RNA/RND**

| Pin Number | Pin Name | NAND Tree Description |
|---|---|---|
| 10 | MDIO | Input |
| 11 | MDC | Input |
| 12 | RXD1 | Input |
| 13 | RXD0 | Input |
| 15 | CRS_DV | Input |
| 16 | REF_CLK | Input |
| 18 | INTRP | Input |
| 19 | TXEN | Input |
| 23 | LED0 | Input |
| 20 | TXD0 | Input |
| 21 | TXD1 | Output |

### 3.9.1 NAND TREE I/O TESTING

Use the following procedure to check for faults on the KSZ8081RNA/RND digital I/O pin connections to the board:

1. Enable NAND tree mode by setting Register 16h, Bit [5] to '1'.
2. Use board logic to drive all KSZ8081RNA/RND NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, in KSZ8081RNA/RND tree pin order, as follows:
   a) Toggle the first pin (MDIO) from high to low, and verify that the TDX1 pin switches from high to low to indicate that the first pin is connected properly.
   b) Leave the first pin (MDIO) low.
   c) Toggle the second pin (MDC) from high to low, and verify that the TXD1 pin switches from low to high to indicate that the second pin is connected properly.
   d) Leave the first pin (MDIO) and the second pin (MDC) low.
   e) Toggle the third pin from high to low, and verify that the TXD1 pin switches from high-to-low to indicate that the third pin is connected properly.
   f) Continue with this sequence until all KSZ8081RNA/RND NAND tree input pins have been toggled.

Each KSZ8081RNA/RND NAND tree input pin must cause the TXD1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the TXD1 pin fails to toggle when the KSZ8081RNA/RND input pin toggles from high to low, the input pin has a fault.

## 3.10 Power Management

The KSZ8081RNA/RND incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

### 3.10.1 POWER-SAVING MODE

Power-saving mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a '1' to Register 1Fh, Bit [10], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ8081RNA/RND shuts down all transceiver blocks except the transmitter, energy detect, and PLL circuits.

By default, power-saving mode is disabled after power-up.

### 3.10.2 ENERGY-DETECT POWER-DOWN MODE

Energy-detect power-down (EDPD) mode is used to further reduce transceiver power consumption when the cable is unplugged. It is enabled by writing a '0' to Register 18h, Bit [11], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

EDPD mode works with the PLL off (set by writing a '1' to Register 10h, Bit [4] to automatically turn the PLL off in EDPD mode) to turn off all KSZ8081RNA/RND transceiver blocks except the transmitter and energy-detect circuits.


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Power can be reduced further by extending the time interval between transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure two link partners in the same low power state and with auto MDI/MDI-X disabled can wake up when the cable is connected between them.

By default, energy-detect power-down mode is disabled after power-up.

### 3.10.3 POWER-DOWN MODE

Power-down mode is used to power down the KSZ8081RNA/RND device when it is not in use after power-up. It is enabled by writing a '1' to Register 0h, Bit [11].

In this mode, the KSZ8081RNA/RND disables all internal functions except the MII management interface. The KSZ8081RNA/RND exits (disables) power-down mode after Register 0h, Bit [11] is set back to '0'.

### 3.10.4 SLOW-OSCILLATOR MODE

Slow-oscillator mode is used to disconnect the input reference crystal/clock on XI (Pin 8) and select the on-chip slow oscillator when the KSZ8081RNA/RND device is not in use after power-up. It is enabled by writing a '1' to Register 11h, Bit[5].

Slow-oscillator mode works in conjunction with power-down mode to put the KSZ8081RNA/RND device in the lowest power state, with all internal functions disabled except the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable slow-oscillator mode by writing a '0' to Register 11h, Bit [5].
2. Disable power-down mode by writing a '0' to Register 0h, Bit [11].
3. Initiate software reset by writing a '1' to Register 0h, Bit [15].

## 3.11 Reference Circuit for Power and Ground Connections

The KSZ8081RNA/RND is a single 3.3V supply device with a built-in regulator to supply the 1.2V core. The power and ground connections are shown in Figure 3-9 and Table 3-6 for 3.3V VDDIO.

**FIGURE 3-9: KSZ8081RNA/RND POWER AND GROUND CONNECTIONS**

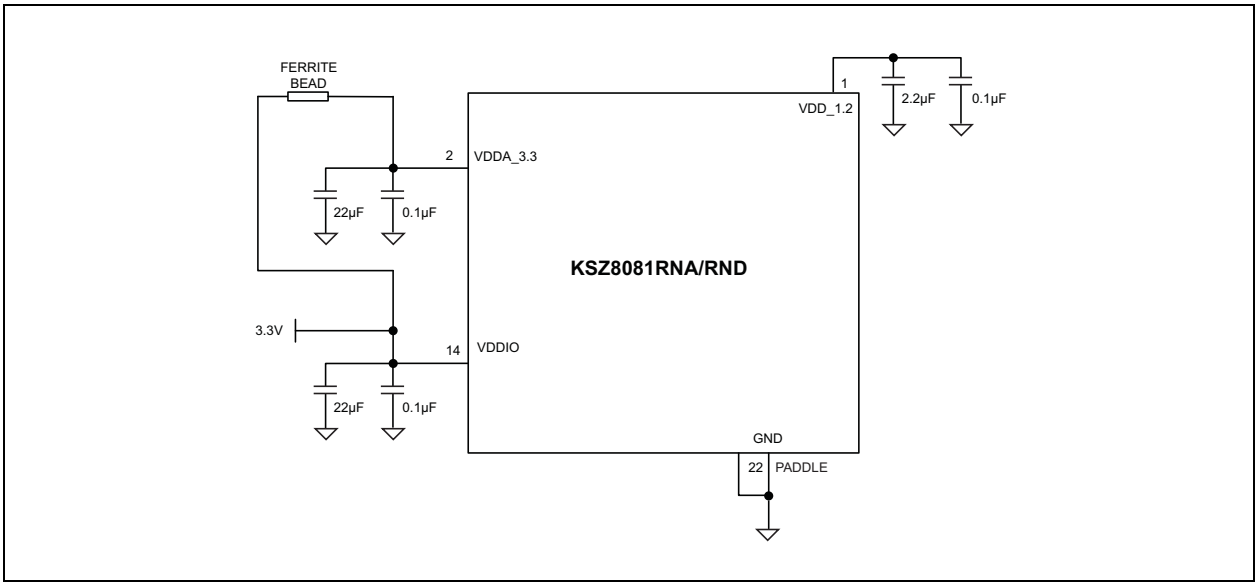

**TABLE 3-6: KSZ8081RNA/RND POWER PIN DESCRIPTION**

| Power Pin | Pin Number | Description |
|---|---|---|
| VDD_1.2 | 1 | Decouple with 2.2 µF and 0.1 µF capacitors to ground. |
| VDDA_3.3 | 2 | Connect to board's 3.3V supply through a ferrite bead. Decouple with 22 µF and 0.1 µF capacitors to ground. |
| VDDIO | 14 | Connect to board's 3.3V supply for 3.3V VDDIO. Decouple with 22 µF and 0.1 µF capacitors to ground. |

## 3.12 Typical Current/Power Consumption

Table 3-7, Table 3-8, and Table 3-9 show typical values for current consumption by the transceiver (VDDA_3.3) and digital I/O (VDDIO) power pins and typical values for power consumption by the KSZ8081RNA/RND device for the indicated nominal operating voltage combinations. These current and power consumption values include the transmit driver current and on-chip regulator current for the 1.2V core.

**TABLE 3-7: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 3.3V)**

| Condition | 3.3V Transceiver (VDDA_3.3) | 3.3V Digital I/Os (VDDIO) | Total Chip Power |
|---|---|---|---|
| 100BASE-TX Link-up (no traffic) | 34 mA | 12 mA | 152 mW |
| 100BASE-TX Full-duplex @ 100% utilization | 34 mA | 13 mA | 155 mW |
| 10BASE-T Link-up (no traffic) | 14 mA | 11 mA | 82.5 mW |
| 10BASE-T Full-duplex @ 100% utilization | 30 mA | 11 mA | 135 mW |
| Power-saving mode (Reg. 1Fh, Bit [10] = 1) | 14 mA | 10 mA | 79.2 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) | 10 mA | 10 mA | 66 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1) | 3.77 mA | 1.54 mA | 1.75 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) | 2.59 mA | 1.51 mA | 13.5 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1) | 1.36 mA | 0.45 mA | 5.97 mW |

**TABLE 3-8: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 2.5V)**

| Condition | 3.3V Transceiver (VDDA_3.3) | 2.5V Digital I/Os (VDDIO) | Total Chip Power |
|---|---|---|---|
| 100BASE-TX Link-up (no traffic) | 34 mA | 12 mA | 142 mW |
| 100BASE-TX Full-duplex @ 100% utilization | 34 mA | 13 mA | 145 mW |
| 10BASE-T Link-up (no traffic) | 15 mA | 11 mA | 77 mW |
| 10BASE-T Full-duplex @ 100% utilization | 27 mA | 11 mA | 117 mW |
| Power-saving mode (Reg. 1Fh, Bit [10] = 1) | 15 mA | 10 mA | 74.5 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) | 11 mA | 10 mA | 61.3 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1) | 3.55 mA | 1.35 mA | 15.1 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) | 2.29 mA | 1.34 mA | 10.9 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1) | 1.15 mA | 0.29 mA | 4.52 mW |


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**TABLE 3-9: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 1.8V)**

| Condition | 3.3V Transceiver (VDDA_3.3) | 1.8V Digital I/Os (VDDIO) | Total Chip Power |
|---|---|---|---|
| 100BASE-TX Link-up (no traffic) | 34 mA | 11 mA | 132 mW |
| 100BASE-TX Full-duplex @ 100% utilization | 34 mA | 12 mA | 134 mW |
| 10BASE-T Link-up (no traffic) | 15 mA | 10 mA | 67.5 mW |
| 10BASE-T Full-duplex @ 100% utilization | 27 mA | 10 mA | 107 mW |
| Power-saving mode (Reg. 1Fh, Bit [10] = 1) | 15 mA | 9 mA | 65.7 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) | 11 mA | 9 mA | 52.5 mW |
| EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1) | 4.05 mA | 1.21 mA | 15.5 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) | 2.79 mA | 1.21 mA | 11.4 mW |
| Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1) | 1.65 mA | 0.19 mA | 5.79 mW |